Design Workbook

MVPX2DW/D
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MVP X2 Multiprocessor Evaluation System Design Workbook

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1 Introduction

This document describes the design information on the MVP reference platform. MVP, short for Multiprocessing Verification Platform, is a dual-processor MPC7450-based platform which allows evaluation of the 60X or MPX bus interfaces. It provides all necessary computing platform devices needed to boot Linux, QNX, VxWorks, or other OSes.

This version of the design document describes the “X2” version, which has slight architectural changes over the first X1 version.

1.1 Features

The MVP includes the following features:

- Two MPC745X Processors (MPC7450 or MPC7451 “V’ger” or compatible)
  - 2MB pipelined-burst (PB) L3 Cache
- GD64260 System Controller (“Discovery”)
  - Dual Processor (60X bus mode) or Single-processor (MPX bus mode) interface
  - SDRAM controller
  - Dual PCI Interfaces
  - Dual 10/100base-T Ethernet interfaces
  - Dual serial ports
- SDRAM Modules
  - 2 PC133 SDRAM DIMM sockets
  - 2GB maximum memory (256MB standard)
- PCI Interface #1
  - Two slots, 32 or 64 bit, 66 MHz, 3V
- PCI Interface #2
  - Two slots, 32 bit, 33 MHz, 5V
- Super IO
  - Dual USB 1.0/UHCI v1.1 interface
  - Dual UltraDMA 33 IDE Disk interface
  - PS/2 keyboard and mouse interfaces
- Flash/ROM Interface
  - 32-bit Boot ROM (1-16 MB, 8 MB standard)
  - 32-bit OS/User ROM (1-16 MB, 8 MB standard)
- Ethernet
  - Dual 10/100baseT Ethernet
- Dual UART
  - Standard 9-pin serial port, baud rates up to ~500kpbs
- Power Supplies
  - Individual 18A 1.3 to 2.5V switching power supplies for each MPC7450
  - Adjustable 10A 1.8V and 2.5V switching power supplies for L3 cache, Discovery, etc.
- ATX Motherboard Form-factor

1.2 Overview

Figure 1 shows a block diagram of the MVP, for reference purposes.

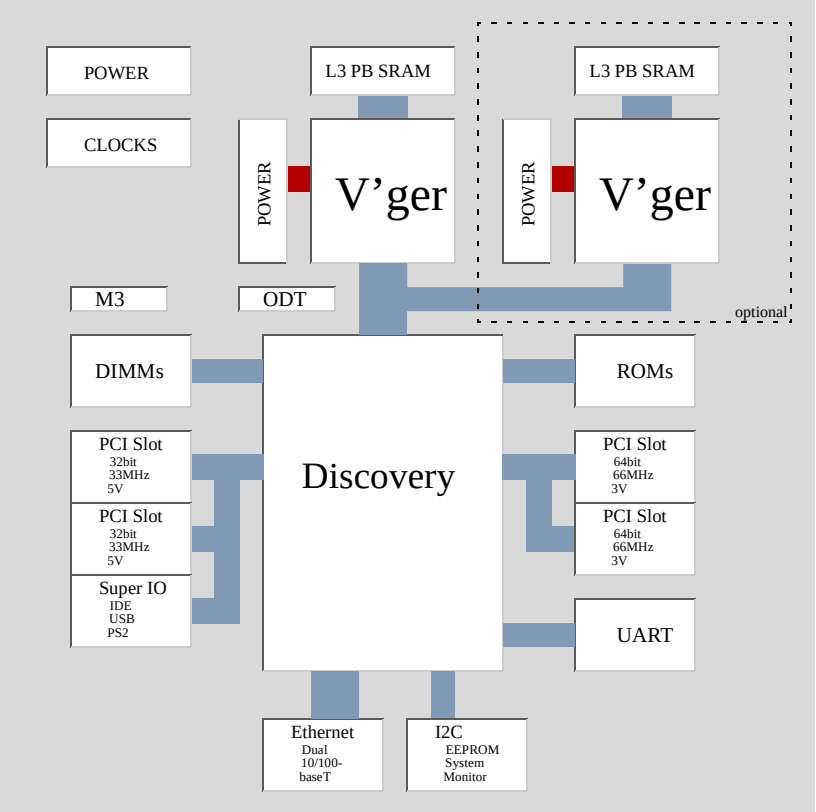


Figure 1. MVP Block Diagram

1.3 Difference between X1 and X2

This version of the MVP Design Document has been adjusted to accomodate revisions between X1 and X2. The board is architecturally similar, but numerous changes and enhancements were made, as described in Table 2.

Table 1. MVP X1 to X2 Changes

Category	Version	Change
Memory	X1	Cannot detect registered DIMMs Bank selects are interleaved: CS0/2 for DIMM #1, CS1/3 for DIMM #2.
	X2	Can detect registered DIMMs via GPIO bit. Bank selects are linear: CS0/1 for DIMM #1, CS2/3 for DIMM #2.
Serial Port	X1	UART baud rate generator must be clocked from bus clock. Serial port speed changes with bus speed.
	X2	Baud rate generator can be clocked from constant 14.318MHz clock. Serial port speed settings are invariant against bus speed.

Table 1. MVP X1 to X2 Changes

Category	Version	Change
ARB	X1	Requires external arbiter for MP-60X systems. Second CPU enabled via MPP port bit.
	X2	Uses internal arbiter for MP-60X systems. Second CPU enabled via internal GT64260 register bit.
Config	X1	Uses pullup/pulldown resistors to configure all GT64260 bits.
	X2	Most options fixed to defaults, others have switch settings.
Clock	X1	Uses SDCLK_OUT from Galileo to drive SDRAM.
	X2	Uses TCLK from main clock to drive SDRAM.
GT64260	X1	Uses ‘rev 0’.
	X2	Uses ‘rev A’.
	X1	Default register base: 0x1400_0000
	X2	Default register base: 0xF100_0000

2 Architecture

The following sections cover the MVP design in more detail. To describe the MVP system details, it is (perhaps) useful to track what devices are present on particular buses. The buses described in Table 2 are present on the MVP system.

Table 2. MVP Bus Architecture

Bus	Connections	Size	Max. Speed	Description	Notes
Processor	CPU #1 CPU #2 Discovery Mictor Debug Headers	32-bit address 4-bit address parity 64-bit data 8-bit data parity	133 MHz	60X or MPX bus	
Cache	CPU #1 CPU #2 PB SRAM	22-bit address 64-bit data 8-bit data parity	200 MHz	Cache data bus	
Memory	SDRAM DIMM #1 SDRAM DIMM #2	64 bits 8 parity/ECC bits	133 MHz	SDRAM bus	
Device	Boot ROM #1 Aux ROM #2	32-bits	100 MHz	IO bus	
Fast PCI	PCI Slot #1 PCI Slot #2	64-bits	66 MHz	Primary PCI bus	
Slow PCI	PCI Slot #3 PCI Slot #4 SuperIO	32-bits	33 MHz	Secondary PCI bus	
I2C	DIMM #1 SPD EEPROM DIMM #2 SPD EEPROM Info EEPROM System Monitor	2 bits	1 MHz	I^2C bus	
MII	PHY #1 PHY #2	15 bits	25 MHz	Interface to Ethernet PHYs	
Serial	Serial #1 Serial #2	5 bits	500 kbps	Serial ports	
USB	USB #1 USB #2	4 bits	1.5 Mbps	USB 1.1 Host Port	
PS/2	PS/2 Keyboard PS/2 Mouse	4 bits	~100 kbps	PS/2 Peripheral Port	

2.1 Processors

The MVP platform supports two MPC7450 “V’ger” processors. The system bus interface connects between the two V’ger processors and the “Discovery” system controller, using either the MPX bus protocol or the 60X bus protocol.

2.1.1 BVSEL/L2VSEL

In addition to bus mode configuration, the V’ger processor must be configured for bus I/O voltage (BVSEL) and L3 I/O voltage (L3VSEL). MVP only supports 2.5V I/O on the system bus (for Discovery

compatibility) and 2.5V I/O on the L3 bus (for PB2 compatibility), so these options are not switch/resistors selectable on MVP.

2.1.2 BMODE

The V'ger BMODE pins are controlled to select both the bus mode (MPX or 60X) and the processor ID. Processor ID is controlled with hardware, but bus mode is switch-selectable (however, changing bus mode requires changing two separate switches - see section 3 for details).

Table 3. V'Ger Bus Mode/ID Selection

Processor	BMODE0	BMODE1	Bus Mode	Processor ID
V'ger #1	0 (ON)	OVDD	MPX Bus	0
V'ger #1	1 (OFF)	OVDD	60X Bus	0
V'ger #2	0 (ON)	not $\overline{\text{HRESET}}$	MPX Bus	1
V'ger #2	1 (OFF)	not $\overline{\text{HRESET}}$	60X Bus	1

Each processor detects its own ID by examining bit 26 (CPUID) of the MSSCR0 register.

2.1.3 L3 Cache

Each V'ger processor has a 2MB back-side L3 cache, implemented with two (2) 8Mbit PB SRAM devices operating in the range of 133-200 MHz. The maximum speed of the L3 on MVP will depend upon parts used and may vary subject to availability.

The L3 SRAMs require a 3.3V core power supply and use 2.5V I/O signalling, compatible with V'ger. No other voltage options are provided for.

2.2 System Controller

The system controller is the Galileo GT64260 "Discovery", which provides the following features:

- Multiprocessing 60X bus OR Single-processor MPX bus
- SDRAM memory controller, 133 MHz
- Dual 10/100-base-T Ethernet ports
- Dual serial ports
- I2C interface
- Interrupt Controller
- PCI Bus arbiters

The GT64260 does not support two processors in MPX bus protocol, so the Discovery must be configured to single-processor mode when MPX bus mode is configured (section 3).

2.2.1 Discovery MPP Configuration

Discovery provides many more features than pins. To use particular functions, the MPP (Multi-Purpose Port) must be programmed to provide one of 16 selectable functions per port pin. MVP relies on each MPP

port being set to the proper configuration option as described in Table 4; otherwise, the system may not operate properly.

Table 4. MVP MPP Usage

MPP Bit	MPP Definition	MPP Programming	Usage	Notes
0	GNT0[0]*	MPPCTL0[3:0]	pPCI slot 1 GNT#	
1	REQ0[0]*	MPPCTL0[7:4]	pPCI slot 1 REQ#	
2	GNT0[1]*	MPPCTL0[11:8]	pPCI slot 2 GNT#	
3	REQ0[1]*	MPPCTL0[15:12]	pPCI slot 2 REQ#	
4	GPP[4]	MPPCTL0[19:16]	Cross-processor 1->0 interrupt	
5	GPP[5]	MPPCTL0[23:20]	Cross-processor 0->1 output drive	
6	GPP[6]	MPPCTL0[27:24]	pPCI INT 0 (Slot 1 INTA#, Slot 2 INTD#)	
7	GPP[7]	MPPCTL0[31:28]	pPCI INT 1 (Slot 1 INTB#, Slot 2 INTA#)	
8	GPP[8]	MPPCTL1[3:0]	pPCI INT 2 (Slot 1 INTC#, Slot 2 INTB#)	
9	GPP[9]	MPPCTL1[7:4]	pPCI INT 3 (Slot 1 INTD#, Slot 2 INTC#)	
10	GPP[10]	MPPCTL1[11:8]	sPCI INT 0 (Slot 3 INTA#, Slot 4 INTD#)	
11	GPP[11]	MPPCTL1[15:12]	sPCI INT 1 (Slot 3 INTB#, Slot 4 INTA#)	
12	GPP[12]	MPPCTL1[19:16]	sPCI INT 2 (Slot 3 INTC#, Slot 4 INTB#)	
13	GPP[13]	MPPCTL1[23:20]	sPCI INT 3 (Slot 3 INTD#, Slot 4 INTC#)	
14	GPP[14]	MPPCTL1[27:24]	PHY1 INT*	
15	GPP[15]	MPPCTL1[31:28]	PHY2 INT*	
16	GNT1[0]*	MPPCTL2[3:0]	sPCI slot 3 GNT#	
17	REQ1[0]*	MPPCTL2[7:4]	sPCI slot 3 REQ#	
18	GNT1[1]*	MPPCTL2[11:8]	sPCI slot 4 GNT#	
19	REQ1[1]*	MPPCTL2[15:12]	sPCI slot 4 REQ#	
20	GNT2[1]*	MPPCTL2[19:16]	sPCI SIO GNT#	
21	REQ2[1]*	MPPCTL2[23:20]	sPCI SIO REQ#	
22	GPP[22]	MPPCTL2[27:24]	SIOINT	1
23	GPP[23]	MPPCTL2[31:28]	BG1_EN	2
24	GPP[24]	MPPCTL3[3:0]	SYSSTAT	3
25	GPP[25]	MPPCTL3[7:4]	REGE	5
26	GPP[26]	MPPCTL3[11:8]	*reserved*	4
27	GPP[27]	MPPCTL3[15:12]	*reserved*	4
28	GPP[28]	MPPCTL3[19:16]	*reserved*	4
29	GPP[29]	MPPCTL3[23:20]	*reserved*	
30	GPP[30]	MPPCTL3[27:24]	Cross-processor 0->1 interrupt	
31	GPP[31]	MPPCTL3[31:28]	Cross-processor 1->0 output drive	

NOTES:
1 Active high interrupt.
2 GPIO signal set to output; active high enables secondary processor if external arbiter option is used.
3 LED drive output; set to active low output.
4 Reserved pin; set to input.
5 Registered mode DIMM detect (common to both slots). 1 = registered; 0 = normal.

2.3 MVP FPGAs

The MVP motherboard has two FPGAs (or more precisely, CPLDs) which implement various functions, as described in Table 5.

Table 5. MVP FPGA Functions

FPGA	Function
ARB	External Arbiter
	ODT generation
M^3	Reset Controller
	COP Interface Levels
	Configuration Logic
	ROM Mode Selection

The first FPGA, ARB, implements the external arbiter needed for multiprocessing in the 60X bus mode when used with the Rev 0 GT64260. This function is not needed with the Rev A device, and may be depopulated. Provisions to implement the external arbiter are retained on the MVP X2 board, and can support the re-installation and evaluation of the external arbiter.

Alternately, the ARB FPGA can be installed and provided with a different design database to implement ODT debugging assistance. ODT assists logic analyzers in recovering trace flow of overlapping/pipelined address and data buses such as the Motorola MPC7450 uses.

The second FPGA, M^3, provides general support logic for MVP. In addition to the reset controller, which is discussed in Section 2.14, M^3 also collects various logic and provides translation between 3.3V environments and the 2.5V V'ger/Discovery system logic, and provides activity monitors with appropriate pulse-width stretching.

2.4 Clocking

MVP must generate many clocks for various devices, as summarized in Table 6.

Table 6. System Clocks

Destination	Signal	Frequency	Quantity	VIO
V'ger processors	pCPUCLK sCPUCLK	66-133 MHz	2	2.5V
Discovery core	SYSCLK	66-133 MHz	1	2.5V
Discovery arbiter	MODCLK	66-133 MHz	1	2.5V
SDRAM modules (2 DIMMs @ 4 clocks ea.)	SDCLK(0:7)	66-133 MHz	8	3.3V
PHY interface clock	CLK_25MHZ	25 MHz	1	3.3V

Table 6. System Clocks

Destination	Signal	Frequency	Quantity	VIO
Fast PCI clocks	pPCICLK(0:3) pPCICLK0 = slot1 pPCICLK1 = slot2 pPCICLK2 = rsv pPCICLK3 = pPCI	33-100 MHz	4	3.3V
Slow PCI clocks	sPCICLK(0:3) sPCICLK0 = slot3 sPCICLK1 = slot4 sPCICLK2 = SIO sPCICLK3 = PCI	25-66 MHz	4	3.3V
USB Clock	CLK_48MHZ	48 MHz	1	5V
SIO Clock	CLK_14MHZ	14.318 MHz	1	5V

Since several of these clocks are completely independent of other clocks, they are generated by simple oscillator components where possible. This has the additional advantage of minimizing the amount of clock traces running over the MVP board, but it is not necessarily the most cost-effective solution. Integrated clock synthesizers can also provide such clocks where board space or cost is at a premium.

The overall clock architecture is shown in Figure 2.

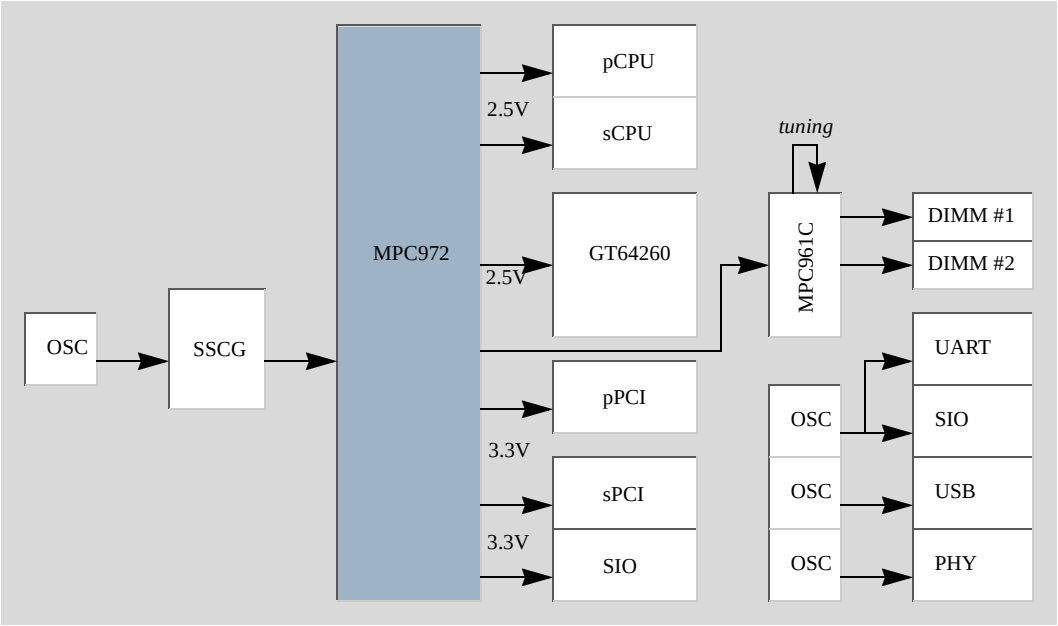


Figure 2. MVP Clock Architecture

The main clocks are generated by the Motorola MPC972, a PLL-based clock multiplier that meets all Motorola MPC7450X restrictions (in particular, low jitter and fast rise/fall time). MVP uses a Motorola MPC961 clock regenerator to drive the SDRAM clocks (up to four per module), which provides the system with the ability to adjust the skew between the Discovery and the SDRAM with configurable path delays; this may be required to operate at high speeds with large memory arrays.

A complication of using the MPC972 or many common clock synthesizers is that the V'ger and Discovery require 2.5V clocks. Instead of buffering the clocks, which would cause unacceptable phase delay, MVP uses resistor dividers which reduce the voltage at the destination to 2.5V in a manner compatible with a 55 ohm impedance board. The divider network is shown in Figure 3.

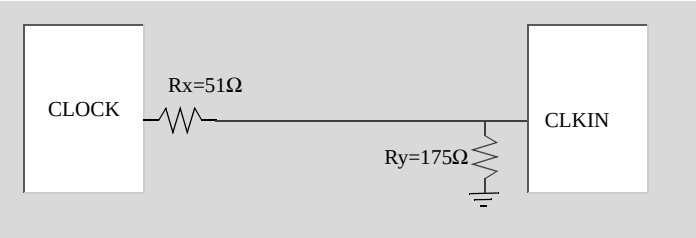


Figure 3. MVP Clock Resistor Dividers

The MPC972 uses programmable divider options to synthesize clocks using divisions of a high-frequency internal VCO. Consequently, there are literally hundreds of combinations, though many are not usable. The table shown in Table 7 lists some of the more useful combinations; other combinations can be derived from the MPC972 hardware specification if custom frequencies are needed.

Table 7. System Clock Selection

CPU & Memory Bus Speed	Fast/3V PCI Bus Speed	Slow/5V PCI Bus Speed	SW7 Settings
133 MHz	66 MHz	33 MHz	0100 0010
100 MHz	66 MHz	33 MHz	1111 1010
100 MHz	33 MHz	33 MHz	1010 1000
83 MHz	55 MHz	41 MHz	0111 1101
66 MHz	66 MHz	33 MHz	0101 0101
66 MHz	33 MHz	33 MHz	0000 0001

NOTES:
0 = ON = UP (viewed with I/O connectors at top of board)
1 = OFF = DOWN

2.4.1 Spread-Spectrum Clock

MVP includes a spread-spectrum modulated clock which dynamically alters the base frequency of the CPU, system memory and PCI bus clocks (other clocks are unaffected). This option is useful for attaining FCC/VDE compliance with radiated emissions. Only the minimum spread range, +/- 0.625%, is guaranteed to meet the MPC745X clock input jitter requirements, though higher spreads are possible if the maximum system frequency is not selected.

2.5 Memory

The MVP system provides memory resources described in Table 8.

Table 8. .MVP Memory Resources

Type	Size	Speed	Address Range	Memory Range	Notes
SDRAM	0 .. 2GB	33 ... 133 MHz	Direct	0000_0000 ... 3FFF_FFFF	1
Flash	32 MB	33 ... 133 MHz	Direct	FF00_0000 ... FF7F_FFFF FF80_0000 ... FFFF_FFFF	2
NVRAM	256 B	33 MHz	Indirect	XX00_0072 ... XX00_0073	3
EEPROM	256 B	1 MHz	Serial	00 ... FF	

NOTES:
1 The maximum speed of SDRAM may be dependant on availablility of particular revisions of silicon; refer to the system configuration sheet for details).
2 There are two separate 16MB flash devices at the addresses shown; the total size is 32MB.
3 Access to NVRAM is via an address/data register in the real-time-clock component of the VIA SuperIO.

2.5.1 SDRAM

MVP supports one or two standard PC-100/PC-133, 3.3 Volt, single-data-rate SDRAM DIMM sockets. Each socket connects to two separate bank enables on the Discovery system controller, and each bank may be up to 1GB in size, so a total of up to 4GB may be supported. Figure 4 shows a block diagram of the SDRAM memory architecture.

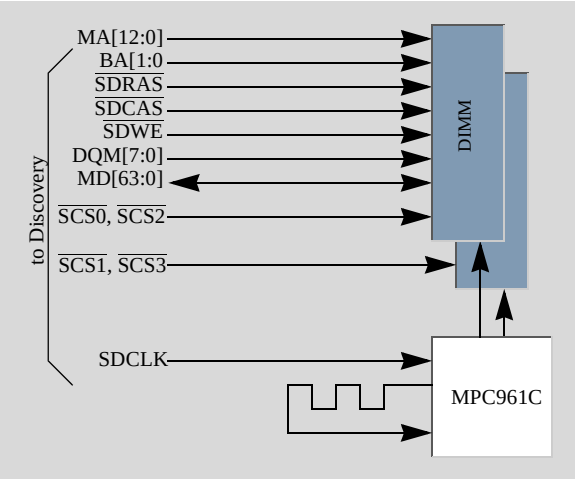


Figure 4. SDRAM Architecture

The connections between Discovery and the SDRAM sockets are fairly straightforward. Except for the databus, most SDRAM signals are output only and may be routed in a daisy-chain from Discovery to each DIMM socket, keeping overall trace lengths short, paired and separated by at least 6-12 mils. Signals are source-series-terminated with impedance matching resistors; no other termination is used.

The DIMM clocks are generated by an MPC961, which generates in-phase copies of the SDCLK (SDRAM clock) that is matched to the Discovery system clock (SYSCLK).

Registered mode SDRAM DIMMs are supported and can be enabled with an external configuration switch. Since Discovery does not support low-power modes, CKE is not supported and is simply tied high for each module.

Since DIMMs are available in one- or two-physical bank configurations, MVP interleaves the chip selects provided to the sockets so that either type may be supported. No matter how the multiple DIMM chip selects are connected, software must be aware to the possibility of mixed single- and dual-bank DIMMs and manage chip selects accordingly, as shown in Table 9.

Table 9. MVP Memory Resources

DIMM Type #1	DIMM Type #2	SCS0 Used	SCS1 Used	SCS2 Used	SCS3 Used	Notes
Single	Single	Yes	No	Yes	No	1
Single	Dual	Yes	Yes	No	Yes	
Dual	Single	Yes	Yes	Yes	No	
Dual	Dual	Yes	Yes	Yes	Yes	

NOTES:
1 Single-bank DIMMs are generally preferred for higher-speed operation, especially at 133 MHz.

2.6 Flash Memory

MVP supports two banks of 32-bit flash memory for startup code (“boot flash”) and other purposes, typically OS firmware storage. Each flash bank may be populated with 1, 2, 4, or 8MB TSSOP48W flash devices, supporting a maximum total of 32MB. Figure 5 shows a block diagram of the MVP flash memory architecture.

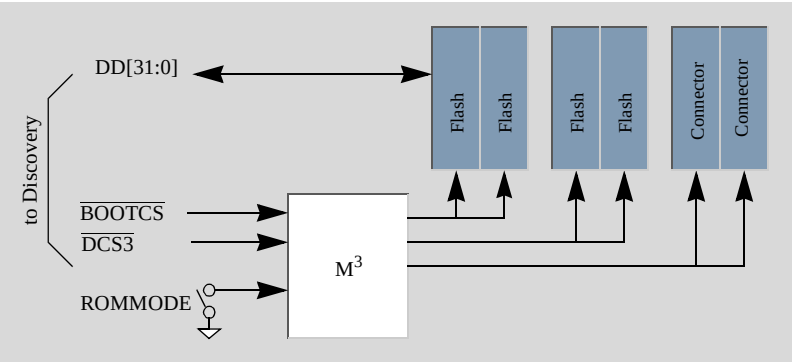


Figure 5. MVP Flash Architecture

Socketable flash devices, no matter how attractive during the code development process, are no longer reasonable to use on systems due to limited size and power options. To support code development, a popular method to circumvent this is to desolder the flash devices and replace them with special cables to flash emulators; however this is difficult for many end users to accomplish.

MVP instead adds two dedicated high-density connectors which are parallel to the flash memory bus. Dedicated cables may be used to connect the flash emulators to the MVP board, without removing the original devices. The M^3 FPGA contains ROM selection mode which disables one of the on-board flash

banks and redirects accesses to the flash emulator, for transparent switching between on-board and off-board flash.

To allow the emulator to intercept the standard flash controls, the M^3 FPGA alters the definition of the BOOTCS and DCS3 chip selects from Discovery. Typically these signals are routed directly to the component, but on MVP M^3 alters them according to Table 10.

Table 10. Flash ROM Modes

ROMMODE(0:1)	Mode	Controls
00	Standard Boot	$\overline{\text{BOOTCS}}$ controls U14, U15 DCS3 controls U16, U13
01	Aux Boot	$\overline{\text{DCS3}}$ controls U14, U15 $\overline{\text{BOOTCS}}$ controls U16, U13
10	Emulate Standard Boot	$\overline{\text{BOOTCS}}$ controls J1, J2 DCS3 controls U16, U13
11	Emulate Aux Boot	$\overline{\text{BOOTCS}}$ controls U14, U15 DCS3 controls J1, J2

Using the ROMMODE option switches, startup code can be swapped among the flash memory banks, and each bank can be redirected to the ROM emulator sockets for quick download. Note that both banks cannot be emulated at the same time.

The flash may be sector-protected by applying +12V to the “SECPR” test pad and running appropriate software. Neither DINK nor other software make any use of this facility at this time.

2.7 PCI

The Discovery supports two independant PCI buses, each configurable for 32 or 64-bit operation, and at 33 or 66 MHz operation (among other frequencies). MVP separates the two buses into a high-speed 3.3V/64-bit/66 MHz PCI bus and a slower 5V/32-bit/33 MHz bus, as shown in Figure 6. The latter bus allows connection of the PCI-based VIA SuperIO, which only operates at 33 MHz.

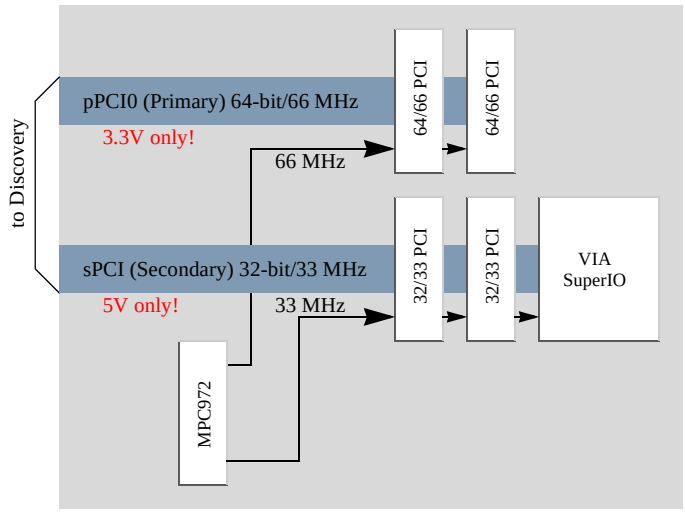


Figure 6. MVP PCI Architecture

All PCI signals are handled by the Discovery with the exception of clocks. Interrupts and bus arbitration are available through the Discovery MPP port (and optionally in the case of the secondary PCI bus, the VIA PCI interrupt controller), and will require proper and careful initialization to be setup properly.

To simplify PCI clock generation, the secondary PCI buses is fixed at 33 MHz only; the primary PCI may be set to 33, 50 or 66 MHz operation. MVP does not automatically switch between 66 and 33 MHz if a “33 MHz only” card is inserted in a 66 MHz slot.

2.7.1 PCI Configuration

Each PCI device accessible as a target has an associated device number, implemented by connected the devices IDSEL pin to the corresponding PCI AD[31:0] bus. PCI device numbers start at 13 (for marginal compatibility reasons, with previous Motorola evaluation platforms) and increment.

Table 11. PCI Configuration Addresses

Component	Device Number	Notes
Slot 1 (J25)	13	2
Slot 2 (J26)	14	2
reserved	15	2
Secondary PCI Interface	16	1, 2
Slot 3 (J23)	17	2
Slot 4 (J24)	18	2
Primary PCI Interface	19	1, 2
SuperIO	20	2

NOTES:
1 IDSEL for PCI interface provided for PCI test card probing only; performing PCI configuration cycles to self may or may not be valid.
2 The primary and secondary PCI domains have different IDSEL/configurations accesses, and so it is possible to have (for example) IDSEL=AD15 on both PCI buses. Separate devices numbers are therefore not a requirement, but having globally unique device numbers may aid software management.

2.8 Ethernet

MVP supports two 10-/100-baseT ethernet ports. The ports are connected directly to two 3.3V LevelOne LXT971 PHYs, using the standard MII interface. The physical signals are then connected through standard

isolation transformers (Pulse Engineering NPI-6120-30) into a dual-RJ45 jack. Figure 7 shows the general arrangement.

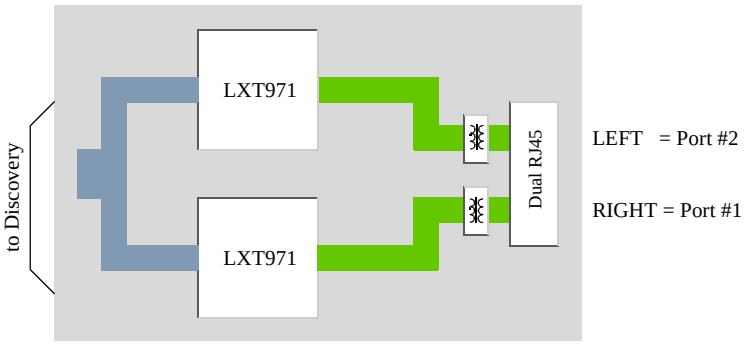


Figure 7. MVP Ethernet Architecture

The Ethernet ports are connected to a dual RJ45 header block which includes two LEDs. Each pair of LEDs is driven by the corresponding LED outputs of the PHY interface (LXT971). The PHY can automatically control the LEDs with various functions such as link active, activity, speed, etc. Refer to the LXT971 specification for LED programming.

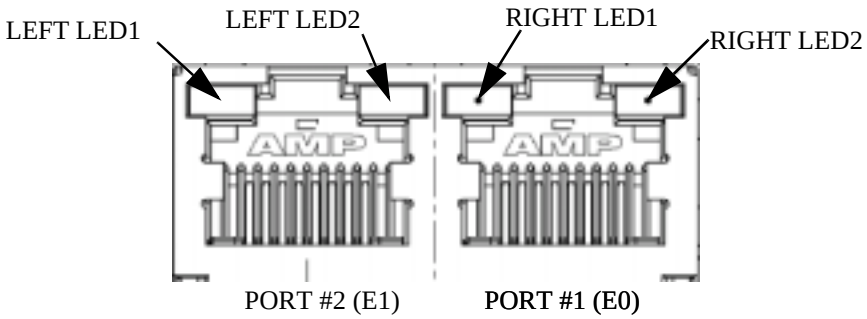


Figure 8. MVP Ethernet Ports with LEDs

The LEDs are by default initialized to the functions shown in Table 12 (though software can select other options).

Table 12. Ethernet Connector LED Functions

LED	Default Function
Left LED1	Speed Status: ON = 100 Mbps OFF=10 Mbps
Left LED2	Link Status: ON=Active OFF=Inactive
Right LED1	Speed Status: ON = 100 Mbps OFF=10 Mbps
Right LED 2	Link Status: ON=Active OFF=Inactive

2.9 UART

The Discovery supports two serial devices. MVP drives the UART to standard RS-232 levels and a dual DB9 male connector (also PC standard). The UART signals are driven to RS232 levels by two Maxim

MAX211CAI chips, which also provide ESD protection to the ports with no additional circuitry. Table 13. shows the location and use of each port.

Table 13. UART Information

UART	Location	Function
0	Top	DINK Console
1	Bottom	DINK Host

These serial ports are standard DTE (Data Terminal Equipment) ports, so to connect MVP to another computer (for terminal emulator purposes) requires a “null-modem” cable. Refer to the DINK User’s Manual for details on such a cable, if needed.

2.10 I^2C

MVP uses an I^2C bus to communicate with various on-board peripherals. The I^2C controller is provided in the Discovery device. Table 14 describes the address at which each device may be found.

Table 14. I2C Addresses

Address	Device	Description
0x4D	LM87	System Monitor
0x50	SDRAM DIMM #1	DIMM SPD Information
0x51	SDRAM DIMM #2	DIMM SPD Information
0x57	EEPROM	256 bytes of general-purpose storage

For details on the internal registers of the LM87, or on the format of DIMM SPD data, refer to the corresponding document in Table 36..

2.11 PIPC

The PCI Integrated Peripheral Controller (PIPC), also referred to as SIO on MVP, contains numerous I/O and control facilities needed for modern computer systems or embedded OS support, including:

- Dual UltraDMA-33 IDE disk interface
- Dual USB interface
- PS2 Keyboard and Mouse interface
- NVRAM
- APC power controller
- Secondary PCI interrupt controller

The SIO used on MVP is the Via Technologies VT82C586B. This SIO is used on many PC motherboard, so OS support should be relatively straightforward and many drivers may already exist for SIO functions. The SIO also includes an PCI interrupt controller which may be used to re-architect the interrupt hierarchies of MVP. Refer to the interrupt architecture section for more detail on the use of the VIA SIO PCI interrupt in this manner.

2.11.1 IDE

The SIO has a PC-compatible dual-channel UltraDMA-33 IDE disk controller. Interrupts flow through the VIA PCI interrupt controller (which must be used whether the VIA PCI interrupt controller is used for other purposes or not) into the dedicated SIOINT interrupt pin to the Discovery.

2.11.2 PS/2

The SIO has a dual PS/2 driver which can be used to connect PS/2-style keyboard and mice.

Table 15. PS/2 Port Location

Location	Function
Top	PS/2 Mouse
Bottom	PS/2 Keyboard

The interface is identical to that used on PCs; once the VIA has been programmed as a valid PCI target for I/O accesses, the PS/2 interface may be controlled at standard PC addresses (i.e. XX00_0060/XX00_0064, where “XX” is software-determined).

2.11.3 USB

The SIO includes two USB 1.0/UHCI-1.1 compatible ports for connecting to keyboards, mice, scanners, printers, and other peripherals. MVP has an internal power supply capable of supplying up to 500mA to each USB device, and short-circuit protection at 1.25A.

2.11.4 NVRAM

The SIO has 256 bytes of battery-backed (NV) RAM. The SIO maintains the state of the NVRAM using either the VSTBY power available from the ATX power supply when it is plugged in (but not necessarily “ON”), or from the lithium coin cell on the motherboard.

2.11.5 APC

The SIO contains an APC power controller which allows “soft” power supply on-off via front-panel switches, by timers in the APC, or by software. The APC also manages transitions between standby power and the 3V coin-cell battery in maintaining the contents of the RTC and NVRAM.

2.12 Power

Assuming that each component and each PCI slot draws the maximum amount of power, the total requirements of the MVP board are shown in Table 16.

Table 16. MVP Power Requirements

Symbol	Voltage	Tolerance	Used By	Amount	Total	Power, Maximum	Notes
pVCORE	+1.8V	± 10%	V'GER:	20 A	20 A	40 W	2, 4
sVCORE	+1.8V	± 10%	V'GER:	20 A	20 A	40 W	2, 4
VCC_1.8	+1.8V	± 10%	DISCOVERY:	950 mA	950 mA	1.8 W	4, 5
VCC_2.5 OVDD VCACHEIO	+2.5V	± 10%	V'GER: DISCOVERY: SRAM_IO: FPGA:	(2) @ 1.5A 500 mA (4) @ 72*1mA 200 mA	3.9 A	10 W	1, 4
VCC	+5V	± 5%	PCI: RS232: SIO: USBPWR: ATPWR: PWR_CORE: PWR_1.8 PWR_2.5	(4) @ 5A (2) @ (20mA+5*20mA) 80 mA 2.5 A 1 A (2) @ 9.2A 460 mA 2.3 A	45 A	225 W	1
VCC_3.3 VCACHE	+3.3V	± 10%	SRAM: PCI: FPGA: DISCOVERY: SDRAM: MPC961: FLASH: PHY:	(4) @ 640 mA (4) @ 7.6A 300 mA 1.4 A (3) @ 1.5A 40 mA 12 mA (2) @ 110 mA	39.5 A	132 W	1
VSTDBY	+5V	± 5%	SIO-APC	1 uA	1 mA	5 mW	
VBAT	+3V	± 20%	SIO-APC	1 uA	1 uA	3 uW	
VCC_12	+12V	± 5%	PCI:	(4) @ 500 mA	2000 mA	24 W	
VCC_12N	-12V	± 10%	PCI	(4) @ 100 mA	400 mA	4.8 W	
					Total	385 W	4

NOTES:
1 Assumes 85% conversion efficiency.
2 Voltage may vary; 2.0VDC assumed for worst-case power calculations.
3 The previous standard that IO power is 10-15% of core power is no longer reasonable. Instead, equivalent 100 MHz bus for current G4 processors are assumed, rated w/CVVF.
4 Only input supplies are considered in the total; shaded totals are derived from other input supplies and are not included in the total power requirements.
5 The VCC1_8 power supply is overrated because MVP will switch from PBSRAM to DDR or PCDDR at the next revision.

Note that the table uses only worst-case numbers; few if any PCI cards use 500mA of 12V power. Nonetheless, to insure adequate power, MVP will require at bare minimum a 400W ATX power supply, with 500-600 W generally recommended. This is particularly true since the above table does not include power for external equipment such as disk drives.

Standard ATX power supplies are available in this range. Table 17. lists some compatible power supplies.

Table 17. MVP Power Supply Vendors

Manufacturer	Part Number	Power	Contact
Sparkle Power	FSP400-60PFN(12V)	400W	www.sparklepower.com

2.13 Interrupts

MVP uses the Discovery as a the primary interrupt handler, and optionally can relegate some interrupts to the Via SuperIO. Discovery has an extensive interrupt flexibilities, but it is somewhat limited in the number of discrete interrupts supported. Furthermore, the interrupt controller is quite different from that of the MPC107/MPC8240 EPIC or PC PIC, so software may require some careful thought in this area.

The MVP interrupt architecture is shown in Figure 9.

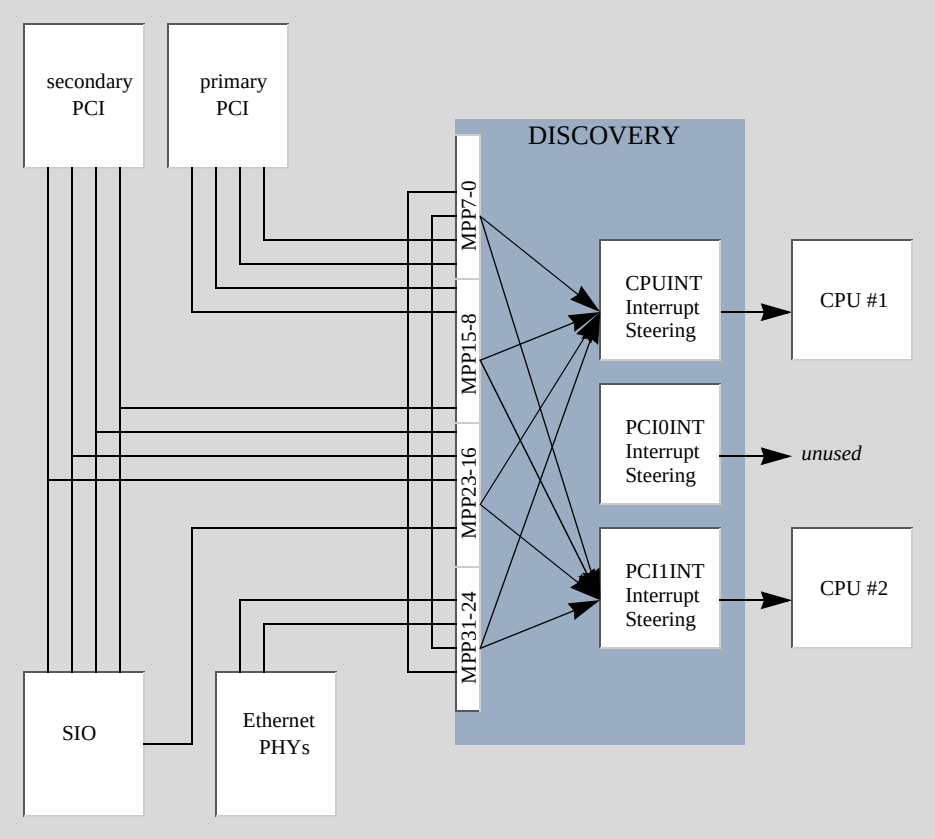


Figure 9. MVP Interrupt Architecture

There are many external interrupt sources possible on an MVP platform, in addition to the numerous ones available inside Discovery (including but not limited to ethernet, serial, DMA, PCI handling, and memory errors). Since Discovery has a limited number of directly triggerable interrupt input pins (basically interrupts are triggered on one of the four MPP byte lanes), interrupt handlers will have to essentially share

interrupts. The SuperIO PIC can be used to handle the secondary PCI bus interrupt for a reduction in interrupt sharing, though an additional level of interrupt processing hierarchy is introduced.

Discovery has one primary $\overline{\text{CPUINT}}$ signal, which is used to signal CPU #1 (Primary). For the second CPU, the secondary PCI interrupt output $\overline{\text{PCI1INT}}$ is used. Despite the name, these interrupts have the same capabilities as the $\overline{\text{CPUINT}}$ signal, so once any of the interrupt sources have been routed as shown in Table 18, it may be further routed to a particular processor.

Table 18. MVP Interrupt Resources

Interrupt	Connection	MPP Byte Lane	Driving Resource(s)	Notes
PCI Error	(internal)	N/A	(internal)	
		N/A		
Cross-processor 1->0	MPP bit #4	0	MPP[31]	
Primary PCI Int0	MPP bit #6	0	pSLOT_INT(1)-INTA# pSLOT_INT(2)-INTD#	1, 2
Primary PCI Int1	MPP bit #7	0	pSLOT_INT(1)-INTB# pSLOT_INT(2)-INTA#	1, 2
Primary PCI Int2	MPP bit #8	1	pSLOT_INT(1)-INTC# pSLOT_INT(2)-INTB#	1, 2
Primary PCI Int3	MPP bit #9	1	pSLOT_INT(1)-INTD# pSLOT_INT(2)-INTC#	1, 2
Secondary PCI Int0	MPP bit #10	1	sSLOT_INT(1)-INTA# sSLOT_INT(2)-INTD#	1, 2
Secondary PCI Int1	MPP bit #11	1	sSLOT_INT(1)-INTB# sSLOT_INT(2)-INTA#	1, 2
Secondary PCI Int2	MPP bit #12	1	sSLOT_INT(1)-INTC# sSLOT_INT(2)-INTB#	1, 2
Secondary PCI Int3	MPP bit #13	1	sSLOT_INT(1)-INTD# sSLOT_INT(2)-INTC#	1, 2
ENet PHY #1 Interrupt	MPP bit #14	1	LXT971A #1(L) MDINT*	
ENet PHY #2 Interrupt	MPP bit #15	1	LXT971A #2(R) MDINT*	
SuperIO Interrupt	MPP bit #22	2	SIOINT	3
Cross-processor 0->1	MPP bit #30	3	MPP[5]	

NOTES:
1 Requires MPP setup.
2 Interrupts are shared in a rotating fashion among PCI domains to handle multi-interrupt-capable boards.
3 An active-high/edge-triggered interrupt, unlike PCI interrupt drivers (active-low/level-sensitive).

Note that all of the external interrupt resources are connected through the MPP port, so MPP setup is required for any interrupts.

Since the Discovery cannot trigger a distinct interrupt on the change of one MPP pin, as noted above interrupt handling software must be prepared to poll or otherwise handle the possibility that one or all of the devices on a single MPP byte lane are asserting interrupts. For example, an interrupt from MPP byte lane 1 could be caused by:

- primary PCI slot 1 INTC#/INTD# pins (fairly rare)
- primary PCI slot 2 INTB#/INTC# pins (fairly rare)
- secondary PCI slot 1 INT(A:D)# pins (fairly likely)

- secondary PCI slot 2 INT(A:D)# pins (fairly likely)
- ethernet PHY interrupts (1 and 2) (possible)

2.13.1 Cross-Processor Interrupts

A common requirement for multiprocessing systems is to allow one CPU to interrupt another, referred to as a cross-processor interrupt. This facility may be used to allow one CPU to hand off interrupt processing to another, or to perform dynamic load balancing of processes.

Since the Discovery does not include a special path for cross-processor interrupts, MVP uses a combination of general-purpose software controlled outputs (GPIO ports), and general-purpose interrupt inputs. These functions are all available through the MPP port of Discovery with appropriate programming.

The cross-processor interrupt architecture is shown in Figure 10.

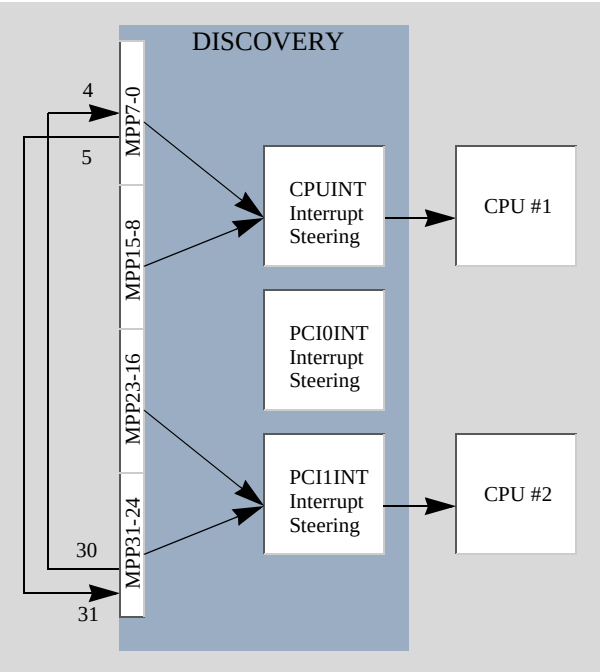


Figure 10. Cross-Processor Interrupts

To use the cross-processor facility, the initialization software must set and use the MPP ports as described in see “MVP Cross-Processor Interrupts” on page 21..

Table 19. MVP Cross-Processor Interrupts

Action	Intiialization Actor	Output Setup	Interrupt Setup	Assert Action	Interrupt Action	Byte Lane
CPU 1 -> CPU 2	CPU #1	Set MPP bit 5 to output.		Set MPP bit 5 = 0, Set MPP bit 5 = 1.		0
	CPU #2		Set MPP bit 30 to: active-low edge-triggered interrupt.		OS-dependant	3

Table 19. MVP Cross-Processor Interrupts

Action	Intiialization Actor	Output Setup	Interrupt Setup	Assert Action	Interrupt Action	Byte Lane
CPU 2 -> CPU 1	CPU #2	Set MPP bit 31 to output.		Set MPP bit 31 = 0, Set MPP bit 31 = 1.		3
	CPU #1		Set MPP bit 4 to: active-low edge-triggered interrupt.		OS-dependant	0

Notice that in the table, CPU1 only uses byte lane 0 (aligned at 0xF100_XXX0) while CPU2 uses only byte lane 3 (aligned at 0xF100_XXX3). Since Discovery allows byte-access to the MPP control/status bits, processors can read from or write to the associated byte portion of the 32-bit MPP ports without requiring locks or semaphores for shared arbitration, as is otherwise often needed.

2.13.2 PCI Secondary PCI Interrupt Handling

As noted in Section 2.2.1 earlier, the VIA PIPC can serve as a secondary PCI interrupt handler, merging the interrupt sources from the two secondary PCI slots with its own interrupt capabilities (IDE, USB, serial, PS/2) to the standard SIOINT pin. This allows modelling software which requires the presence of an 8259 PIC.

2.14 Reset

The reset architecture of MVP is fairly straightforward, as long as these reset requirements are followed:

- PCI resets must not be released before CPU or Discovery resets
- Configuration logic drive must not be released until one clock after Discovery reset release

In the M^3 FPGA, a simple sequencer provides the required sequence, as described in Table 20.

Table 20. MVP Reset Sequence

Time	Event	Outputs
t_{RH}	RESET input deasserted	$\overline{\text{pHRESET}}$ deasserted $\overline{\text{sHRESET}}$ deasserted $\overline{\text{SYSRST}}$ deasserted
t_{RH}+1	Configuration drive ends	$\overline{\text{CFGDRV}}$ deasserted
t_{RH}+2	PCI resets deasserted	$\overline{\text{pPCIRST}}$ deasserted $\overline{\text{sPCIRST}}$ deasserted

The general reset architecture is shown in Figure 11.

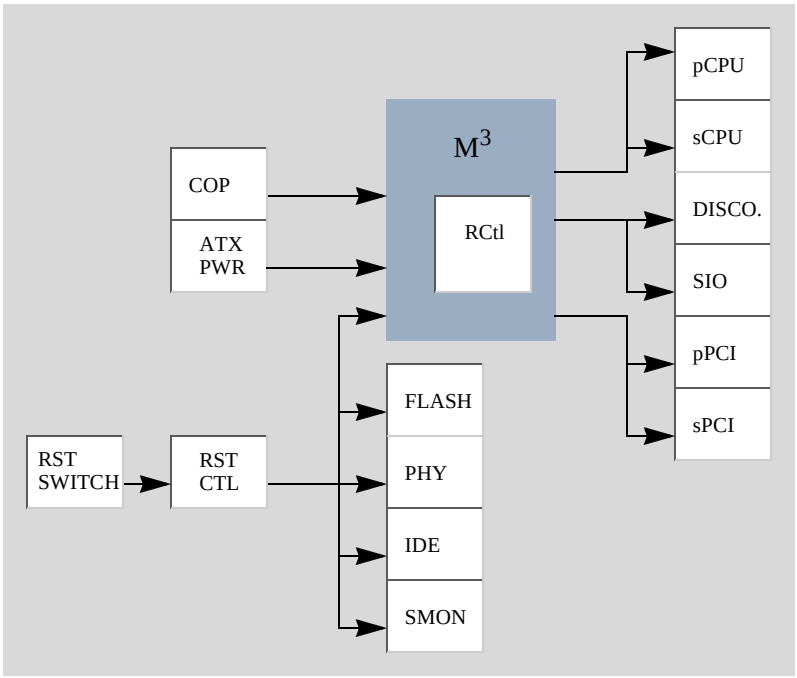


Figure 11. MVP Reset Architecture

In operation, the ATX power supply or either of the reset pushbutton switches may initiate a system reset and cause the reset controller to drive the global reset signal $\overline{\text{RESET}}$ low. The FPGA, in turn, derives the secondary reset signals and drives them at the appropriate time.

The reset controller keeps $\overline{\text{RESET}}$ asserted for approximately 350 milliseconds, which is sufficient to reset all Motorola MPC745X processors as well as others used on MVP. Upon release, the Discovery controller latches in configuration options, and then begins to process bus transaction.

2.14.1 Service Interrupt

MVP includes a debounced reset switch which can be configured to assert one of the signals in Table 21..

Table 21. Service Switch Definition

Definition	Asserted Signal	Install	Note
Primary CPU Soft-Reset	pSRESET	R271	1, 2
Secondary CPU Soft-Reset	$\overline{\text{sSRESET}}$	R265	2
Primary CPU Checkstop	$\overline{\text{pCKSTPI}}$	R266	2
Secondary CPU Checkstop	$\overline{\text{sCKSTPI}}$	R267	2
Primary Machine Check	pMCP	R268	2
Primary Service Management Interrupt	pSMI	R269	2

NOTES:
1 Default as shipped.
2 All other resistors should generally be removed except the signal of interest.

Note that changing the assertion selection requires moving a 0-Ω resistor.

3 Configuration

MVP contains several slide-switches used to configure the board, processors(s) and chipsets for the options shown in Table 22. Underlined entries are the defaults, as shipped. Since the switches operate by connecting a pulled-up signal to ground, setting a switch to “ON” is indicated as ‘0’ in the table.

All switches are oriented so that “ON”=”0”=“UP”, where “UP means toward the PCI and I/O connector back panel of the ATX chassis. If the chassis is standing up with the cover off, an alternate interpretation is “ON”=”0”=”LEFT”

Table 22. MVP Configuration Switches

Switch	No	Option	Default Setting	Description	Notes
SW5	1:5	Primary CPU PLL(0:4)	00010	See MPC745X HW spec	2
	6	SSCG Enable	1	0 = SS Enable 1 = SS Disable	1
	7	ARB Option	0	0 = Normal 1 = TBD	1
	8	Bus Mode	1	0 = MPX Bus Mode 1 = 60X Bus Mode	4
SW6	1:5	Secondary CPU PLL(0:4)	00010	See MPC745X HW spec	2
	6	Registered SDRAM Mode	0	0 = Normal DIMMs 1 = Registered DIMMs	
	7:8	ROM Mode	00	See Table 10.	
SW7	1:8	Clock Code		See Table 7.	
SW4	1	MMM Option	0	0 = Normal 1 = TBD	1
	2	Flash Write Protect	0	0 = Flash Writes Disabled 1 = Flash Writes Enabled	
	3	Discovery Serial Initialize	1	0 = Serial Init Enabled 1 =Serial Init Disabled	
	4	Discovery Bus Mode	0	0 = 60X Bus Mode 1 =MPX Bus Mode	4
	5	Discovery Arbiter Enable	1	0 = Arbiter Disabled 1 =Arbiter Enabled	
	6:8	Discovery PLL Tune	000	000 = Galileo Default	

NOTES:
1 For experimental purposes only; not guaranteed useful.
2 PLL_CFG(0:4) is the same as [PLL_EXT+PLL_CFG(0:3)] from the V’ger Hardware Specification. The bit order is the same as that shown in the PLL Encoding table and can be entered directly.
3 The remaining Discovery options are set with resistors and are not easily changable.
4 Must set both switches to corresponding bus mode.

3.1 Diagnostic Functions

MVP includes several features to assist in hardware/software debugging, which are discussed in the remaining sections.

3.1.1 Mictors

MVP (optionally) includes a set of 5 high-density Mictor headers, connected to the processors' 60X/MPX bus between the V'ger processors and the Discovery. This allows transactions on the bus to be monitored and captured on a standard logic analyzer. Since these headers are placed in a manner which may interfere with chassis insertion, they may or may not be present on the board; refer to the configuration checklist for details.

Two of the most popular analyzers are made by Agilent(HP) and Tektronics. There is no standard numbering scheme on Mictor connectors, and Agilent and Tektronics use differing numbers. There is no standard shroud, and each has a different insertion scheme. Fortunately, both use the predefined connections on the system bus in a consistent manner, so as long as the proper cable adapters and software are used, either analyzer may be used. For a variety of reasons, MVP uses the standards shown in Table 23.

Table 23. MVP Mictor Definitions

Uses	Company	Reason
Mictor Numbering Scheme	Tektronics	Historical
Mictor Shroud	Agilent Tektronics	Low-profile Better mechanical retention
Mictor Labelling	Agilent	Agilent definitions

The Mictor headers are grouped into logical functions. While each signal can be individually captured and examined with a proper logic analyzer setup, typically the signals are grouped into 32-bit quantities and given a label; the logic analyzer disassemblers generally prefer this approach. Thus "TS" becomes part of the capture group "STAT". Table 24 summarizes the connections.

Table 24. MVP Mictor Groups

Group	Definition	Includes	Table	Notes
STAT	Transfer status signals	AACK, DTI, ODT, TSIZ, TT, etc.	Table 25	
ADDR	Standard Address	$\overline{TS}$, A[4:36]	Table 26	1
DATA	Data Bus	D[0:31] (or DH[0:31])	Table 27	
DATA_B	Data Bus Lower	DL[32:63] (or DL[0:31])	Table 28	
STAT_B	Status Miscellaneous	$\overline{BR1}$, $\overline{BG1}$, $\overline{DBG1}$	Table 29	

NOTES:
1 The typical definition is "A0:31" for the MPC74xx family processors, where A0 is the MSB. On V'ger and newer processors, the MSB is still A0, but since the system operates in 32-bit-address mode by default, MVP A(4:35) are the corresponding lowest 32 address bits.

The the remaining tables describe the connections in detail.

Table 25. Mictor STAT Definition

Pin	Signal	
3	AACK	Even Clock
4	$\overline{pBR}$	Even D15 (MSB)
5	$\overline{pBG}$	Even D14
6	$\overline{pDBG}$	Even D13
7	*rsvd*	Even D12
8	*rsvd*	Even D11

Table 25. Mictor STAT Definition

Pin	Signal	
9	DTI[0]	Even D10
10	DTI[1]	Even D9
11	DTI[2]	Even D8
12	DTI[3]	Even D7
13	*rsvd*	Even D6
14	ODT[0]	Even D5
15	ODT[1]	Even D4
16	ODT[2]	Even D3
17	ODT[3]	Even D2
18	ODT[4]	Even D1
19	$\overline{\text{ARTRY}}$	Even D0 (LSB)
36	$\overline{\text{TA}}$	Odd Clock
35	$\overline{\text{TEA}}$	Odd D15 (MSB)
34	TSIZ[0]	Odd D14
33	TSIZ[1]	Odd D13
32	TSIZ[2]	Odd D12
31	*rsvd*	Odd D11
30	TT[0]	Odd D10
29	TT[1]	Odd D9
28	TT[2]	Odd D8
27	TT[3]	Odd D7
26	TT[4]	Odd D6
25	$\overline{\text{TBST}}$	Odd D5
24	$\overline{\text{WT}}$	Odd D4
23	A[0]	Odd D3
22	A[1]	Odd D2
21	A[2]	Odd D1
20	A[3]	Odd D0 (LSB)

Table 26. Mictor ADDR Definition

Pin	Signal	
3	TS	Even Clock
4	A[4]	Even D15 (MSB)
5	A[5]	Even D14
6	A[6]	Even D13
7	A[7]	Even D12
8	A[8]	Even D11
9	A[9]	Even D10
10	A[10]	Even D9
11	A[11]	Even D8
12	A[12]	Even D7

Table 26. Mictor ADDR Definition

Pin	Signal	
13	A[13]	Even D6
14	A[14]	Even D5
15	A[15]	Even D4
16	A[16]	Even D3
17	A[17]	Even D2
18	A[18]	Even D1
19	A[19]	Even D0 (LSB)
36	LACLK	Odd Clock
35	A[20]	Odd D15 (MSB)
34	A[21]	Odd D14
33	A[22]	Odd D13
32	A[23]	Odd D12
31	A[24]	Odd D11
30	A[25]	Odd D10
29	A[26]	Odd D9
28	A[27]	Odd D8
27	A[28]	Odd D7
26	A[29]	Odd D6
25	A[30]	Odd D5
24	A[31]	Odd D4
23	A[32]	Odd D3
22	A[33]	Odd D2
21	A[34]	Odd D1
20	A[35]	Odd D0 (LSB)

Table 27. Mictor DATA Definition

Pin	Signal	
3	*rsvd*	Even Clock
4	D[0]	Even D15 (MSB)
5	D[1]	Even D14
6	D[2]	Even D13
7	D[3]	Even D12
8	D[4]	Even D11
9	D[5]	Even D10
10	D[6]	Even D9
11	D[7]	Even D8
12	D[8]	Even D7
13	D[9]	Even D6
14	D[10]	Even D5
15	D[11]	Even D4
16	D[12]	Even D3

Table 27. Mictor DATA Definition

Pin	Signal	
17	D[13]	Even D2
18	D[14]	Even D1
19	D[15]	Even D0 (LSB)
36	*rsvd*	Odd Clock
35	D[16]	Odd D15 (MSB)
34	D[17]	Odd D14
33	D[18]	Odd D13
32	D[19]	Odd D12
31	D[20]	Odd D11
30	D[21]	Odd D10
29	D[22]	Odd D9
28	D[23]	Odd D8
27	D[24]	Odd D7
26	D[25]	Odd D6
25	D[26]	Odd D5
24	D[27]	Odd D4
23	D[28]	Odd D3
22	D[29]	Odd D2
21	D[30]	Odd D1
20	D[31]	Odd D0 (LSB)

Table 28. Mictor DATA_B Definition

Pin	Signal	
3	*rsvd*	Even Clock
4	D[32]	Even D15 (MSB)
5	D[33]	Even D14
6	D[34]	Even D13
7	D[35]	Even D12
8	D[36]	Even D11
9	D[37]	Even D10
10	D[38]	Even D9
11	D[39]	Even D8
12	D[40]	Even D7
13	D[41]	Even D6
14	D[42]	Even D5
15	D[43]	Even D4
16	D[44]	Even D3
17	D[45]	Even D2
18	D[46]	Even D1
19	D[47]	Even D0 (LSB)
36	*rsvd*	Odd Clock

Table 28. Mictor DATA_B Definition

Pin	Signal	
35	D[48]	Odd D15 (MSB)
34	D[49]	Odd D14
33	D[50]	Odd D13
32	D[51]	Odd D12
31	D[52]	Odd D11
30	D[53]	Odd D10
29	D[54]	Odd D9
28	D[55]	Odd D8
27	D[56]	Odd D7
26	D[57]	Odd D6
25	D[58]	Odd D5
24	D[59]	Odd D4
23	D[60]	Odd D3
22	D[61]	Odd D2
21	D[62]	Odd D1
20	D[63]	Odd D0 (LSB)

Table 29. Mictor STAT_B Definition

Pin	Signal	
3	*rsvd*	Even Clock
4	$\overline{\text{pINT}}$	Even D15 (MSB)
5	$\overline{\text{sINT}}$	Even D14
6	$\overline{\text{pCPU\_HRST}}$	Even D13
7	*rsvd*	Even D12
8	*rsvd*	Even D11
9	*rsvd*	Even D10
10	*rsvd*	Even D9
11	*rsvd*	Even D8
12	*rsvd*	Even D7
13	*rsvd*	Even D6
14	*rsvd*	Even D5
15	*rsvd*	Even D4
16	*rsvd*	Even D3
17	*rsvd*	Even D2
18	*rsvd*	Even D1
19	*rsvd*	Even D0 (LSB)
36	*rsvd*	Odd Clock
35	F1VIS	Odd D15 (MSB)
34	F2VIS	Odd D14
33	*rsvd*	Odd D13
32	*rsvd*	Odd D12

Table 29. Mictor STAT_B Definition

Pin	Signal	
31	*rsvd*	Odd D11
30	*rsvd*	Odd D10
29	sBR	Odd D9
28	sBG	Odd D8
27	sDBG	Odd D7
26	GTBR	Odd D6
25	pBR_GTBG	Odd D5
24	sBR_GTDBG	Odd D4
23	*rsvd*	Odd D3
22	*rsvd*	Odd D2
21	*rsvd*	Odd D1
20	*rsvd*	Odd D0 (LSB)

3.1.2 LEDs

Table 30 describes the diagnostic LEDs on the MVP motherboard.

Table 30. MVP Diagnostic LEDs

LED	PCB Label	Definition	Activation Method
pBEAT	CPU1	Activity on pBG, stretched to >10ms.	CPU #1 performs bus cycles.
sBEAT	CPU2	Activity on pBG, stretched to >10ms.	CPU #2 performs bus cycles.
M1	M1	User-defined.	Set VIA GPIO 0 bit 0 to ‘0’.
M2	M2	User-defined.	Set VIA GPIO 0 bit 1 to ‘0’.
SYSSTAT	STAT	User-defined.	Set MPP port pin 24 to ‘0’ to activate LED.
pPCILED	pPCI	None.	Control via cPCI hot-swap extended features register.
sPCILED	sPCI	Activity on secondary PCI bus.	Initiated traffic on sPCI bus.
CLKLED	CLK	Clock is running.	Properly set CLK options.
BOOTLED	ROM	Access to any flash device.	Access 0xFFXX_XXXX.
DISKLED	DISK	Disk activity	Access to IDE disk drives.
VSTDBY	VSTD	ATX power supply is plugged in (and rear-panel switch is on)	None (if plugged in)
VCC_2.5	V2_5	VCC_2.5 > 1.5V	Power activated.
VCACHEIO	VCIO	VCACHEIO > 1.5V	
pVCORE	pVCO	pVCORE > 1.5V	
sVCORE	sVCO	sVCORE > 1.5V	
ENET #1 Left		Speed: On when 100baseT; else 10baseT	Upon HRESET, or via LXT971 LED control register.
ENET #1 Right		Link Status: On when link is up.	
ENET #2 Left		Speed: On when 100baseT; else 10baseT	
ENET #2 Right		Link Status: On when link is up.	

3.1.3 System Monitor

MVP includes an LM87 system monitoring device, which provides the following features:

- Power Supply Monitoring (VCORE for primary and secondary, OVDD, +5V and 12V).
- Remote Temperature Sensing
- Fan Speed Sense (two)

The LM87 is accessed using the I^2C bus; reading various registers will return a sampling of the current power supply voltage, sense the thermistor cable, or sense the fan tachometer reading. MVP does not implement the extra circuitry needed to dynamically control fan speed.

Due to the slightly different system voltages as found on MVP, versus a typical PC, some of the LM87 voltage sensing pins have different definitions, as noted in Table 31.

Table 31. MVP Voltage Monitoring Definitions

LM87 Definition	MVP Definition	MVP Valid Range	Notes
V2.5VIN	OVDD	2.3V ... 2.7V	
V5V	VCC_5	4.5V ... 5.5V	
V12V	VCC_12	11V ... 13V	
Vp	VCC_3.3	3.0V ... 3.6V	
Vccp1	pVCORE	1.3V ... 1.8V	
Vccp2	sVCORE	1.3V ... 1.8V	
AIN1	Fan #1 Tachometer	0 ... 5V	1
AIN2	Fan #2 Tachometer	0 ... 5V	1

NOTES:
1 Fans with tachometer sensing may or may not be present.

3.1.4 Trace Characteristic Probes

MVP supports the ability to install a FET probe directly to two co-located signal/ground test pad, allowing easy connection of the FET probe tip and FET probe ground sleeve. Two pair of probes are provided for the $\overline{TS}$ and DH[0] signals, and are located at the center of the connections between the two CPUs, the Discovery and the Mictor headers. This allows a good connection to a scope for trace characteristic observations and to correlate actual signal performance versus simulations.

3.1.5 Power Consumption Measurement

MVP supports the ability to measure the current consumed by various subsystems by removing some high-current, 0-ohm resistors and replacing them with ammeters, or by measuring the voltage across

low-ohm resistors and calculating the corresponding current.. Table 32 shows some of the power measurements possible.

Table 32. MVP Power Measurement

Voltage	Sense Resistor	Used By	Measurement Method	Notes
pVCORE	R217	Primary CPU	I_{CORE} = V_across_R217 / 0.0028	
sVCORE	R218	Secondary CPU	I_{CORE} = V_across_R218 / 0.0028	
VCC_1.8	R25	GT64260 Core	$I_{VCC1.8}$ = V_across_R25 / 0.010	
OVDD	R235	CPU Bus IO FPGA IO	I_{OVDD} = V_across_R235 / 0.010	1
VCACHEIO	R9	CPU Cache IO SRAM IO	$I_{VCACHEIO}$ = V_across_R9 / 0.010	1
VCC_2.5	R26	GT64260 CPU Bus IO FPGA Core	$I_{VCC2.5}$ = (V_across_R26 / 0.010) - I_{OVDD} - $I_{VCACHEIO}$	2

NOTES:
1 Replace sense resistors with a 0.010Ω 2512 resistor.
2 VCC_2.5 also supplies derivative power supplies VCACHEIO and OVDD, so it can only determined by subtracting the latter two supplies.

The other power supplies (5V, 3.3V) can be measured through the ATX power supply.

4 Placement and Layout

The general placement of components on the MVP motherboard is shown in Figure 12.

Figure 12. MVP Placement

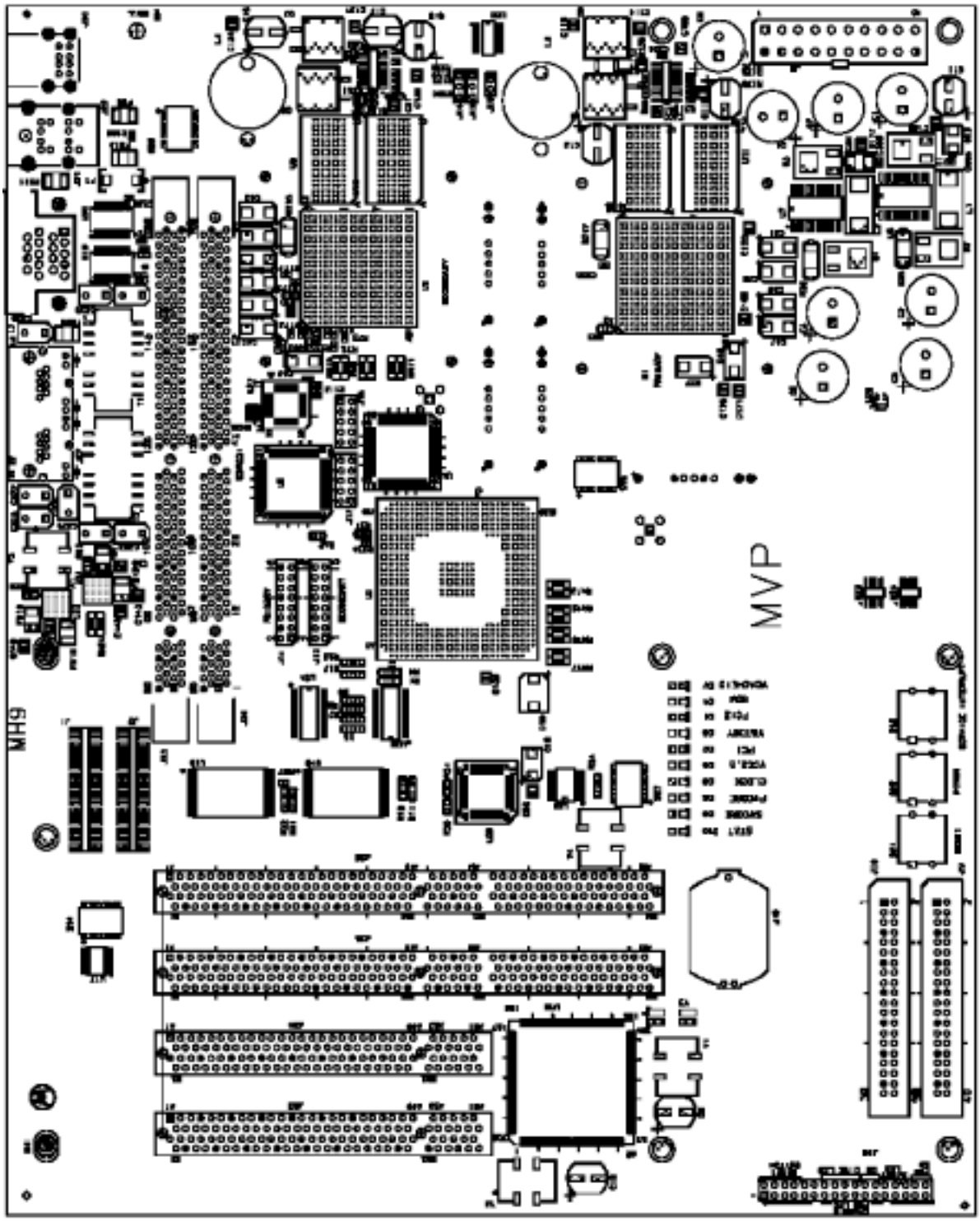
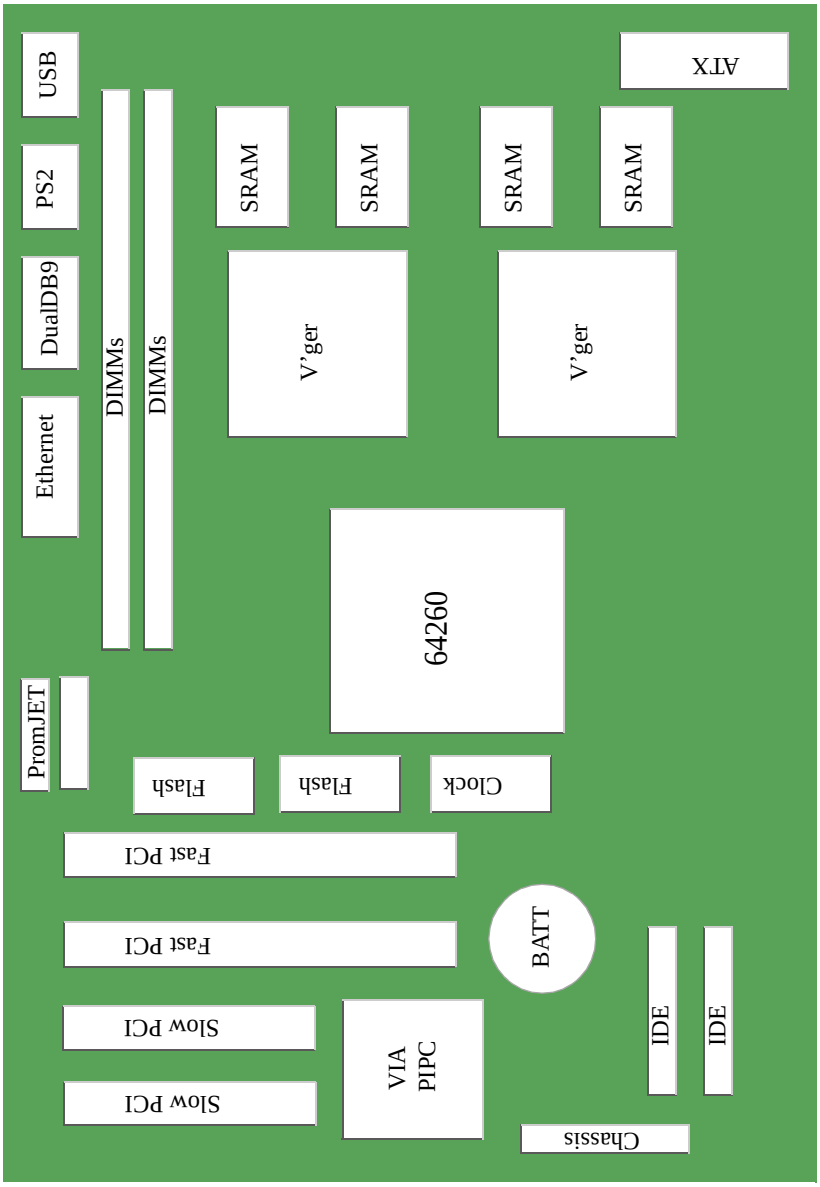


Figure 13. MVP Block Placement



5 Programmers Model

This section describes support information which may be useful to hardware or software designers who are using MVP.

5.1 Address Map

Table 33 shows the general address map of the MVP, while Table 34 shows the specific location of ISA/PCI I/O addresses.

Table 33. Global Address Map

START	END	Definition	Notes
0000_0000	0FFF_FFFF	SDRAM	1
1E00_0000	1EFF_FFFF	PCI/ISA I/O space	2
2000_XXXX	3FFF_FFFF	SDRAM	1
		PCI memory	7
		PCI/ISA memory	7
		PCI configuration address register	7
		PCI configuration data register	7
		Interrupt Acknowledge	7
F100_0000	F100_XXXX	Discovery Configuration Registers	2
FF00_0000	FF7F_FFFF	DCS3 ROM space (8MB)	3, 5, 6
FF80_0000	FFFF_FFFF	Boot ROM space (8MB)	5, 6

NOTES:
1. Requires SDRAM control registers to be properly programmed (TBD).
2. DINK 12.3 default; may be relocated.
3. Requires software setup (CS3 registers [CS3_ADDR_LO]).
4. Only software-enabled PCI/ISA I/O devices appear in this space.
5. Devices may be reassigned using the ROMMODE switches. See Section 3.
6. Devices default to an 8MB aperture, though 16MB is available. To get the full address range of each device, the BOOT/DCS3 address range registers must be reprogrammed.
7. Unassigned by DINK startup code; must be specified by user code.

The detailed address map in Table 34 assumes that the PnP devices have not been changed from the default locations.

Table 34. Detailed ISA I/O Address Map

Start	End	Mode	Register	Notes
1E00_0000	---	R/W	DMA Channel 0 Base/Current Address	
1E00_0001	---	R/W	DMA Channel 0 Base/Current Word	
1E00_0002	---	R/W	DMA Channel 1 Base/Current Address	
1E00_0003	---	R/W	DMA Channel 1 Base/Current Word	
1E00_0004	---	R/W	DMA Channel 2 Base/Current Address	
1E00_0005	---	R/W	DMA Channel 2 Base/Current Word	
1E00_0006	---	R/W	DMA Channel 3 Base/Current Address	
1E00_0007	---	R/W	DMA Channel 3 Base/Current Word	

Table 34. Detailed ISA I/O Address Map

Start	End	Mode	Register	Notes
1E00_0008	---	R	DMA Controller 1 Status	
		W	DMA Controller 1 Command	
1E00_0009	---	W	DMA Controller 1 Request	
1E00_000A	---	W	DMA Controller 1 Mask	
1E00_000B	---	W	DMA Controller 1 Mode	
1E00_000C	---	W	DMA Controller 1 Clear Byte Pointer	
1E00_000D	---	W	DMA Controller 1 Master Clear	
1E00_000E	---	W	DMA Controller 1 Clear Mask	
1E00_000F	---	W	DMA Controller 1 Write All Mask	
1E00_0010	1E00_001F		*unassigned*	
1E00_0020	---	R/W	PIC 1 Command	
1E00_0021	---	R/W	PIC 1 Command	
1E00_0022	1E00_003F		*unassigned*	
1E00_0040	---	R/W	Counter 0	
1E00_0041	---	R/W	Counter 1	
1E00_0042	---	R/W	Counter 2	
1E00_0043	---	W	Timer/Counter Control	
1E00_0044	1E00_005F		*unassigned*	
1E00_0060	---	R/W	Keyboard Controller Data	1
1E00_0061	---	R/W	NMI Status/Control	
1E00_0062	1E00_0063		*unassigned*	
1E00_0064	---	R/W	Keyboard Controller Command	1
1E00_0065	1E00_006F		*unassigned*	
1E00_0070	---	R/W	RTC/APC Index	1
	---	W	RTC Index (shadow)	
1E00_0072	---	R/W	NVRAM Address	
1E00_0073	---	R/W	NVRAM Data	
1E00_0074	1E00_0077		*unassigned*	
1E00_0078	1E00_007F		*unassigned*	
1E00_0080	---		*unassigned*	
1E00_0081	---	R/W	DMA Memory Page 2	
1E00_0082	---	R/W	DMA Memory Page 3	
1E00_0083	---	R/W	DMA Memory Page 1	
1E00_0084	FF80_0086	-	DMA Reserved Page	
1E00_0087	---	R/W	DMA Memory Page 0	
1E00_0088	---	-	DMA Reserved Page	
1E00_0089	---	R/W	DMA Memory Page 6	
1E00_008A	---	R/W	DMA Memory Page 7	
1E00_008B	---	R/W	DMA Memory Page 5	
1E00_008C	FF80_008E	-	DMA Reserved Page	
1E00_008F	1E00_0091		*unassigned*	

Table 34. Detailed ISA I/O Address Map

Start	End	Mode	Register	Notes
1E00_0092	---	R/W	Port 92: System Reset	
1E00_0093	1E00_009F		*unassigned*	
1E00_00A0	---	R/W	PIC 2 Command	
1E00_00A1	---	R/W	PIC 2 Command	
1E00_00A2	1E00_00BF		*unassigned*	
1E00_00C0	---	R/W	DMA Channel 4 Base/Current Address	
1E00_00C1	---	R/W	DMA Channel 4 Base/Current Word	
1E00_00C2	1E00_00C3		*unassigned*	
1E00_00C4	---	R/W	DMA Channel 5 Base/Current Address	
1E00_00C5			*unassigned*	
1E00_00C6	---	R/W	DMA Channel 5 Base/Current Word	
1E00_00C7			*unassigned*	
1E00_00C8	---	R/W	DMA Channel 6 Base/Current Address	
1E00_00C9			*unassigned*	
1E00_00CA	---	R/W	DMA Channel 6 Base/Current Word	
1E00_00CB			*unassigned*	
1E00_00CC	---	R/W	DMA Channel 7 Base/Current Address	
1E00_00CD			*unassigned*	
1E00_00CE	---	R/W	DMA Channel 7 Base/Current Word	
1E00_00CF			*unassigned*	
1E00_00D0		R	DMA Controller 2 Status	
		"W	DMA Controller 2 Command	
1E00_00D3			*unassigned*	
1E00_00D2	---	W	DMA Controller 2 Request	
1E00_00D3			*unassigned*	
1E00_00D4	---	W	DMA Controller 2 Mask	
1E00_00D5			*unassigned*	
1E00_00D6	---	W	DMA Controller 2 Mode W	
1E00_00D7			*unassigned*	
1E00_00D8	---	W	DMA Controller 2 Clear Byte Pointer	
1E00_00D9			*unassigned*	
1E00_00DA	---	W	DMA Controller 2 Master Clear	
1E00_00DB			*unassigned*	
1E00_00DC	---	W	DMA Controller 2 Clear Mask	
1E00_00DD			*unassigned*	
1E00_00DE	---	W	DMA Controller 2 Write All Mask	
1E00_00DF	1E00_00FF		*unassigned*	
1E00_0100	1E00_0CF7		*unassigned*	
1E00_0CF8	1E00_CFB	R/W	PCI Configuration Index Register	
1E00_0CFC	1E00_CFF	R/W	PCI Configuration Data Register	
1E00_0D00	1E00_FFFF		*unassigned*	

5.2 Memory Resources

The SIO has the following non-volatile RAM resources:

- 256 bytes of battery-backed RAM in the SIO
- 256 bytes of EEPROM in an I2C EEROM at address 0x57.

Unlike other Motorola reference design platforms such as Yellowknife or Sandpoint, MVP does not have a large amount of storage available for environment variables, so judicious use is recommended. It is also possible to use the flash devices with careful software management.

5.3 Initializing MVP

A typical multiprocessing start-up sequence is shown in Figure 14:

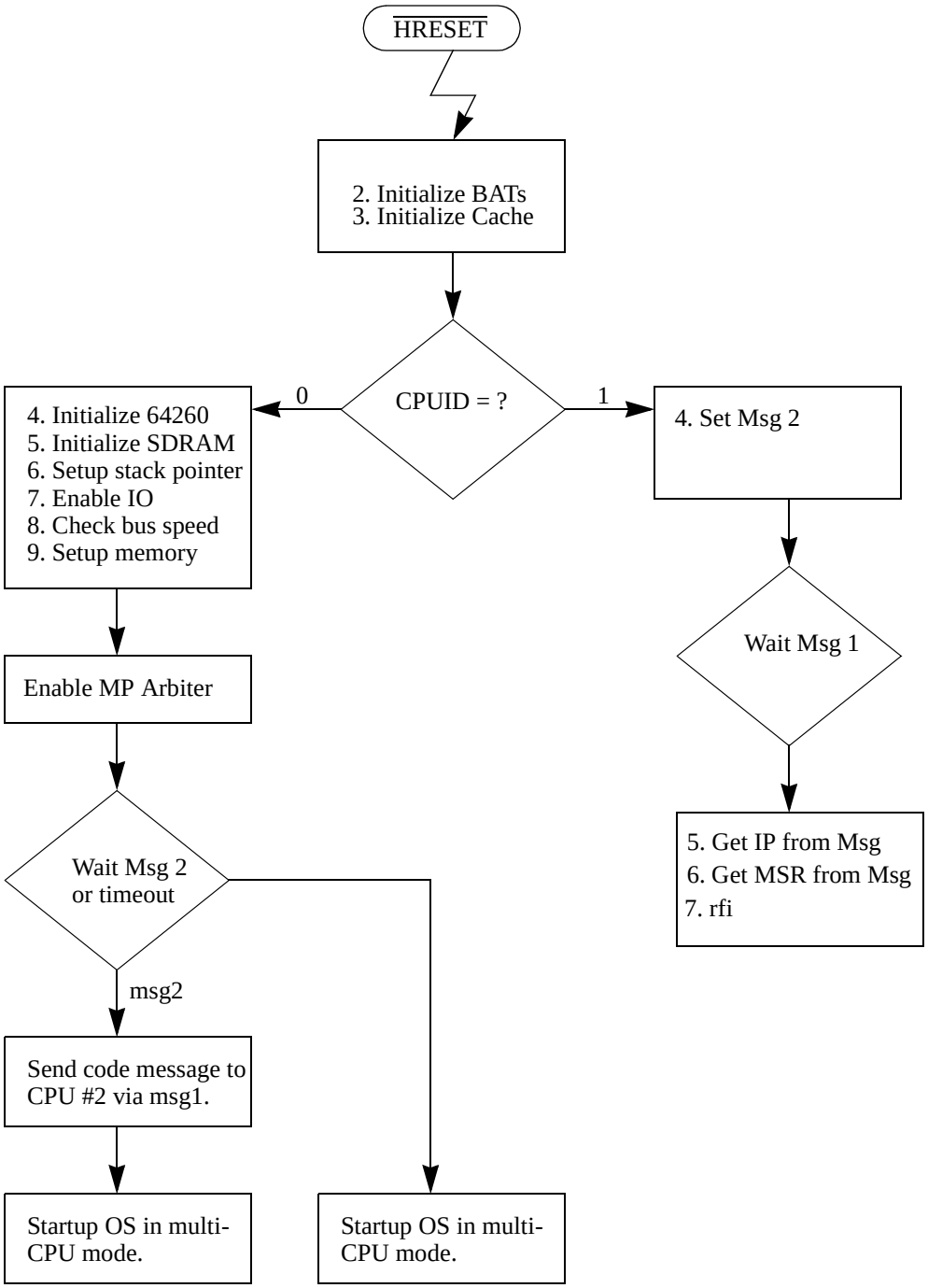


Figure 14. Multiprocessing Startup Sequence

6 Mechanical

The following sections discuss mechanical issues of the MVP board, including board layout, thermal/heatsink issues, and placement. Nothing in this section should be considered a substitute for mechanical drawings.

6.1 Motherboard Dimensions

MVP is a standard 12.0 x 9.6 inch (305 x 244 cm (the specification is written in inches)) motherboard, and follows standard ATX 2.01 clearance requirements. MVP implements the standard set of mounting holes for chassis attachment, with the addition of ATX 2.01 mounting hole “F”, located near the communications port adapter as shown in Figure 15.

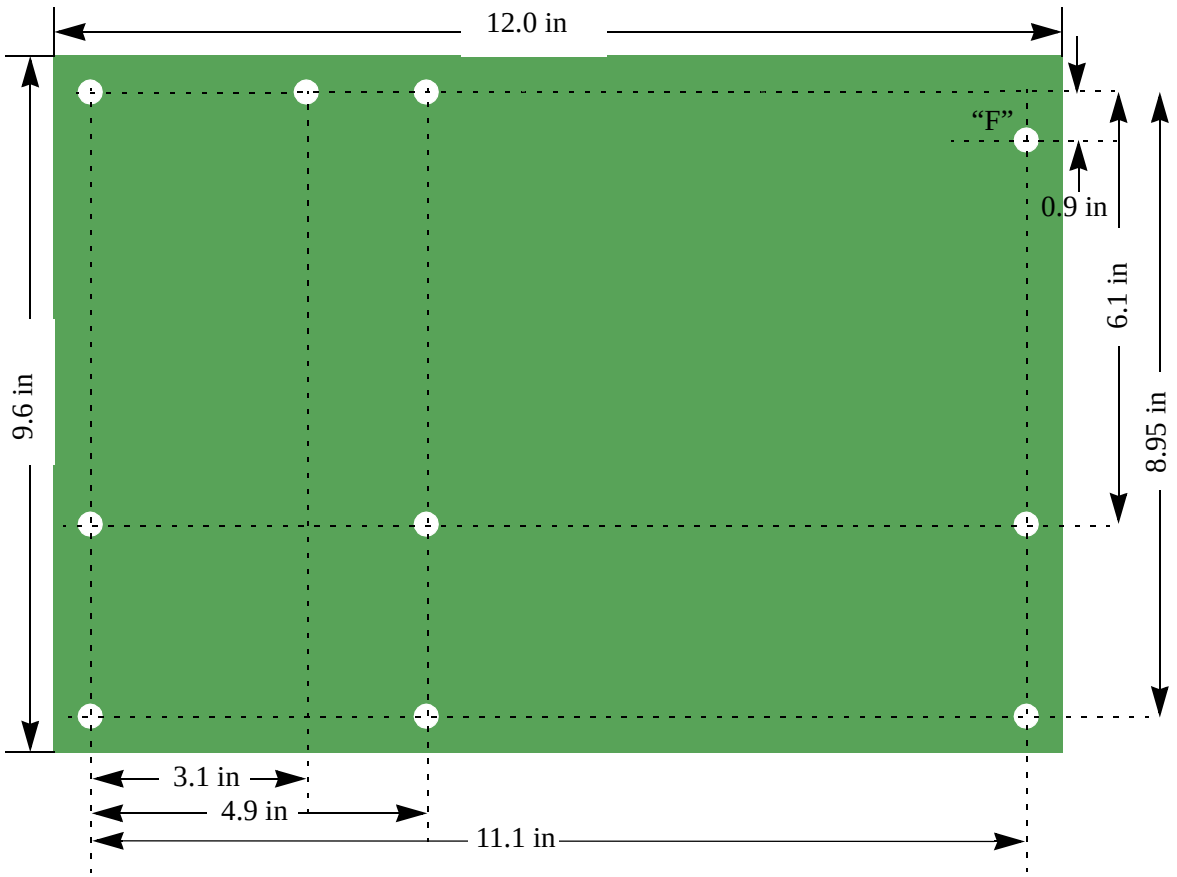


Figure 15. MVP ATX Chassis Mounting Holes.

This hole is required for ATX 2.01 standards and is needed for mechanical rigidity for MVP; most standard standard chassis punchouts implement the standard support area.

6.2 Mictor Clearance

If the MVP is assembled with the Mictor headers for debugging, the connectors will protrude into the ATX motherboard carrier frame. To install MVP in an ATX chassis, either the Mictors must be removed or the

motherboard carrier must have holes cut into the frame for clearance. Figure 16 shows the area which must be cut to install MVP with Mictors attached.

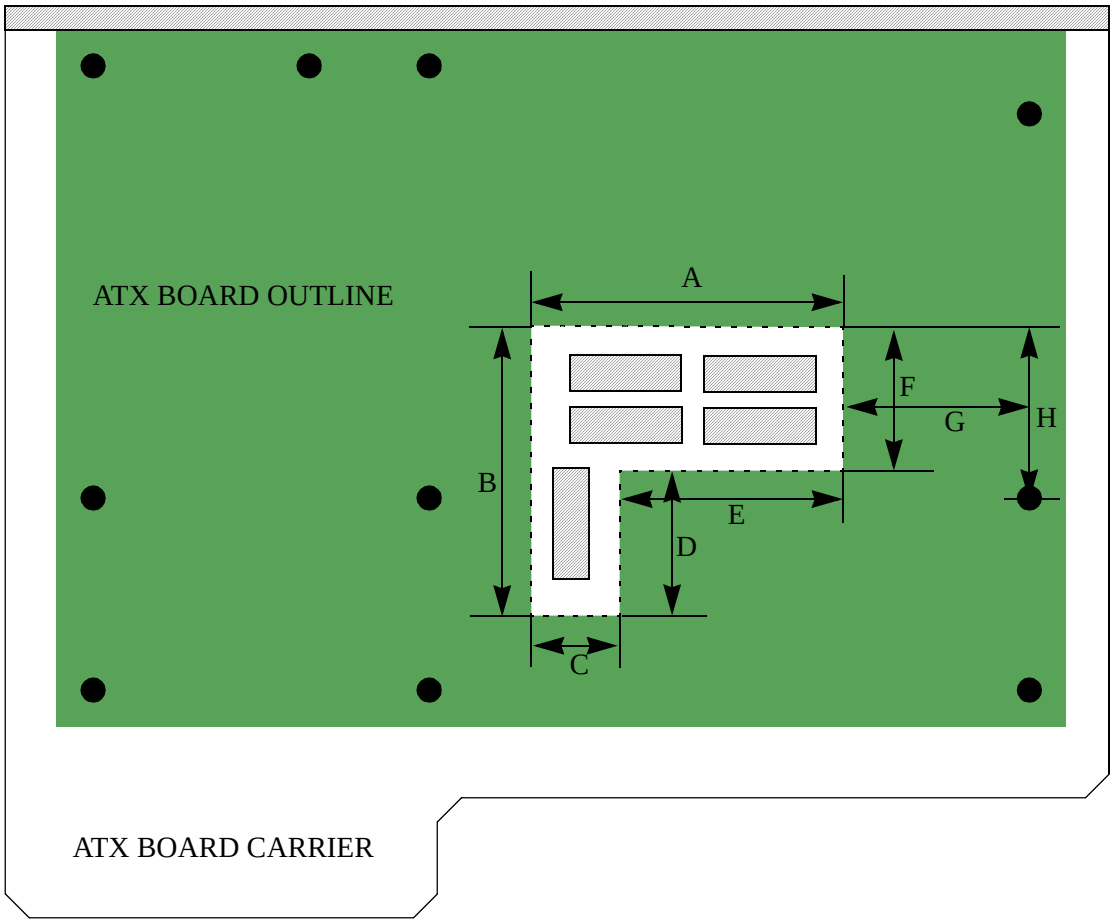


Figure 16. MVP ATX Chassis Carrier Frame Mictor Cutout.

The dimensions are shown in Table 35.

Table 35. Mictor Clearance Cutout Dimensions

Dimension	Value	Units
A		in
B		
C		
D		
E		
F		
G		
H		

Once the cutouts have been made, an MVP with Mictor headers (with or without Tektronix shrouds) can be installed in the carrier frame and also installed in the ATX chassis (no further clearance issues arise). This does not apply when the high-profile Agilent shrouds are used (MVP supports both styles).

6.3 ATX Chassis Gasket

The particular set of IO ports provided by MVP do not match any particular ATX “gasket” (the removable panel which fits between the motherboard and the chassis to provide EMI compliance. Because of this, the MVP will require a custom gasket, as shown in Figure 17.

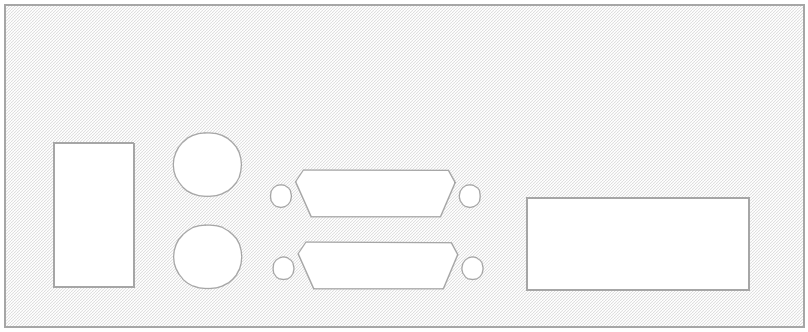


Figure 17. MVP ATX Chassis Gasket

7 Thermal Management

This section discusses some of the thermal issues related to MVP.

Do NOT operate MVP without the heatsinks and/or without the attached fan.

7.1 Heat Sinks

MVP uses heat sinks manufactured by Chip Coolers Inc. Refer to www.chipcoolers.com for further details.

7.2 Fan Sensing

In addition to the heat sink, cooling fans are attached. MVP supports standard PC-style fan-sink speed sensors. The fans connect into a tachometry sensor in the LM87. To sense the fan speed, read the corresponding register in the LM87 using the I^2C bus.

MVP does not implement fan speed control (neither on/off nor modulation).

8 Reference Documentation

Table 36 describes reference documentation which may be useful for understanding the operation of the MVP system.

Table 36. Reference Documentation

Document	Number/Reference
MPC7450 Hardware Specification	e-www.motorola.com/brdata/PDFDB/docs/MPC7450EC.pdf
MPC7450 User's Manual	e-www.motorola.com/brdata/PDFDB/docs/MPC7450UM.pdf
ODT	e-www.motorola.com/brdata/PDFDB/docs/AN2161.pdf (also in MPC7450 hardware specification)
GD64260 (Discovery) Data Sheet	www.GalileoT.com
DINK User's Manual and code updates	www.mot.com/SPS/RISC/smartnetworks/arch/
PCI 2.1 Specification	www.pcisig.com
VIA 82C586B Datasheet	www.via.com.tw/pdf/productinfo/586b.pdf
National LM87CIMT Datasheet	www.national.com/ds/LM/LM87.pdf
SPD Serial Presence Detect Standard	www.chips.ibm.com/products/memory/spddessd/spddessd.pdf
Emulations Technologies "PromJET"	www.emutec.com/pjetadpt.html
LXT971 Documentation Hardware Datasheet Programming Manual	www.level1.com
Heatsinks	www.chipcoolers.com

HOW TO REACH US:

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Motorola Japan Ltd.; SPS, Technical Information Center,
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81-3-3440-3569

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