VR249

VR249, HV system PMIC with low power for industrial safety

Rev. 1.0 — 24 March 2026 **Product brief**

1 Introduction

This product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant VR249 full data sheet, available via the NXP Secure Files content interface.

2 General description

Devices in the VR249 high voltage industrial safety PMIC family are designed to support entry and mid-range safety microcontrollers, like those in the MCX-E series. VR249 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting industrial safety applications. Possible VR249 applications include energy storage, power delivery, gateways and factory automation.

This family of devices consist of several versions that are pin to pin and software compatible. These versions support a wide range of applications with high Industrial Safety Integrity Level upto SIL 2 offering choices in number of output rails, output voltage settings, operating frequencies, power up sequencing, and integrated system level features.

The VR249 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs and communication interfaces. It offers a high precision reference voltage supply for the system, and for two independent tracking regulators. The VR249 also offers various functionality for system control and diagnostics, including an analog multiplexer, General purpose Input/Outputs (GPIOs), and selectable wakeup events from I/O, long duration timer or Serial-Peripheral Interface (SPI) communication.

The VR249 is developed in compliance with the IEC 61508 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on-demand self test, and can be part of a safety-oriented system partitioning scheme covering SIL2 safety integrity level.

3 Features and benefits

Operating range

- 40 V DC maximum input voltage.
- Supports operating voltage range down to 3.2 V with VBST in front-end.
- Supports operating voltage range down to 6 V without VBST in front-end.
- Low power LPOFF mode with 30 µA quiescent current.
- Low power Standby mode with 29 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for low power Standby mode operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: Asynchronous boost controller with external low-side switch, diode, and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Supports high-voltage protection for ECU off- board operation. Each tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness.
- Two programmable GPIO with wake-up capability or HS/LS driver.
- Programmable long duration timer (LDT) for system shutdown and wake-up control.
- Monitoring of system voltages (Including supply voltage monitoring) through the analog multiplexer.
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI activity.
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC).

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness sto support various industrial EMI test standards.

Functional safety

- Industrial safety level support up to SIL -2
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function.
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup.
- Analog built-in self-test (ABIST2) on demand.
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B).

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management.
- Permanent device customization via one time programmable (OTP) fuse memory.
- OTP Emulation mode for hardware development and evaluation.
- Debug mode for software development, MCU programming, and debugging.

4 Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

4.1 Part number definition

Figure 1 shows how the VR249xyz part number is used to describe the available feature set of each device.

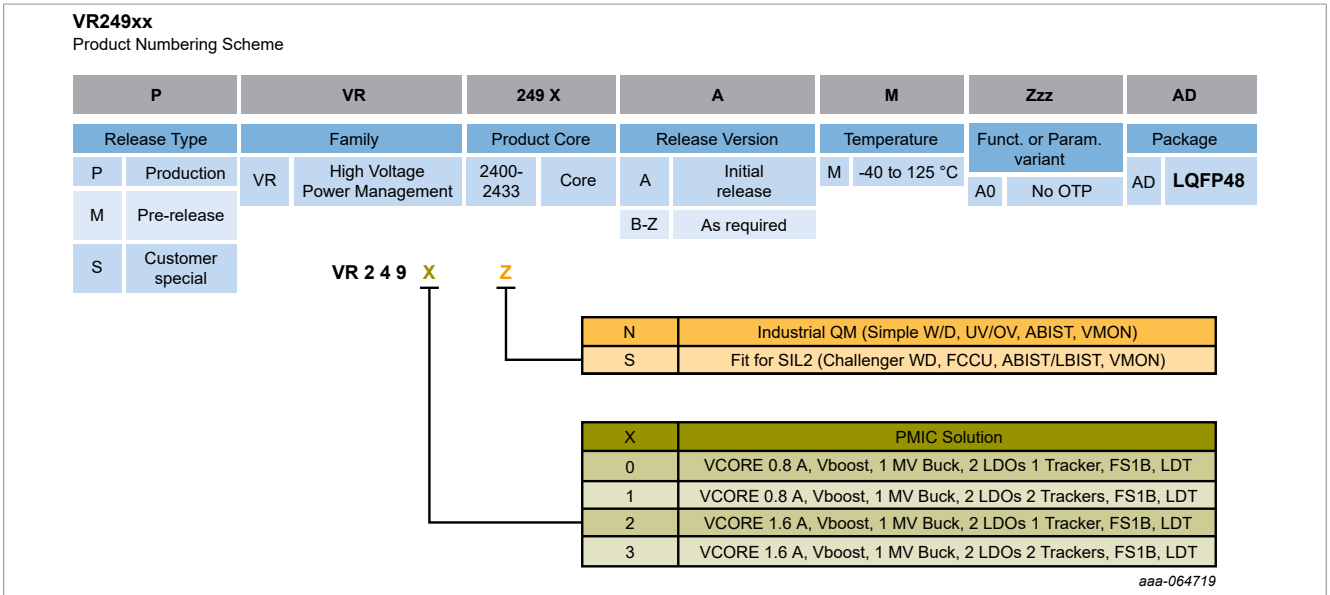

Figure 1. Part number breakdown

Figure 2 maps VR249 part numbers vs. product feature sets.

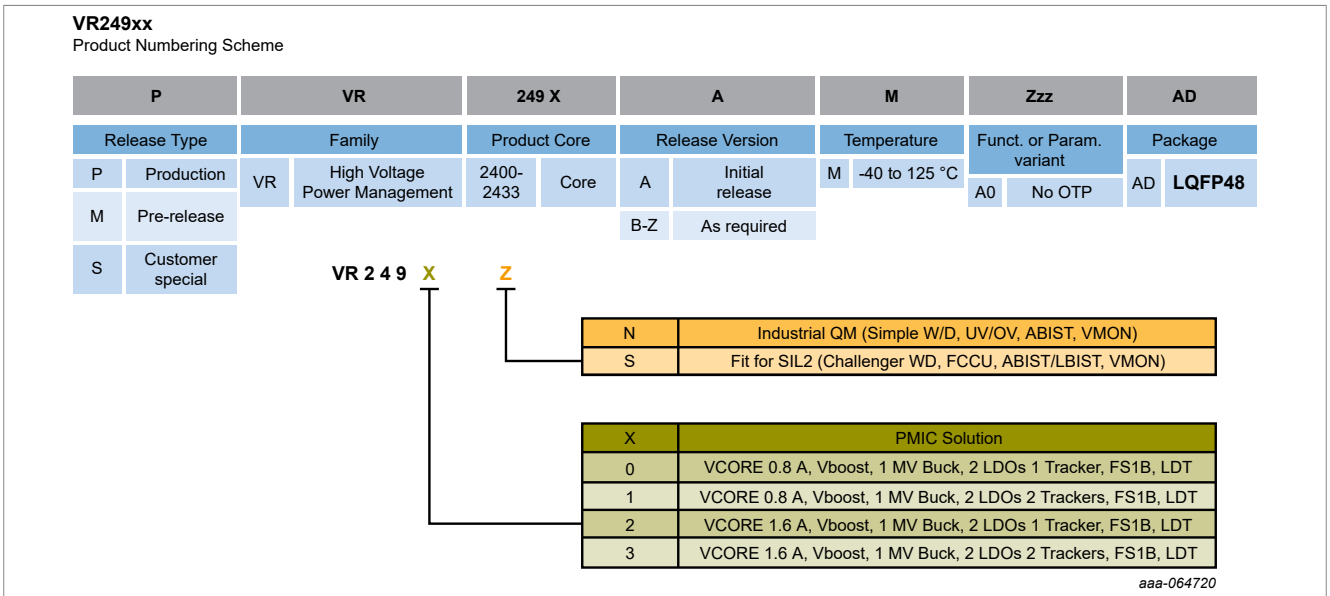

Figure 2. art number mapping versus features set

4.2 Part number list

Additional part numbers will exist with different features and parametric settings. Table 1 is an example of a part number list.

Table 1. Orderable parts example

Part No.	DEV_ID	Tracker 2	Core current capability	Long duration timer	Tracker 2 monitoring	FS1B	ABIST on demand	Watchdog type	Fault recovery	FCCU monitoring	LBIST
VR2490N	0x21	NO	0.8 A	YES	NO	YES	YES	Simple	NO	NO	NO
VR2490S	0x22	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
VR2491N	0x23	YES	0.8 A	YES	YES	YES	YES	Simple	NO	NO	NO
VR2491S	0x24	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
VR2492N	0x25	NO	1.65 A	YES	NO	YES	YES	Simple	NO	NO	NO
VR2492S	0x26	NO	1.65 A	YES	NO	YES	YES	Challenger	YES	YES	YES
VR2493N	0x27	YES	1.65 A	YES	YES	YES	YES	Simple	NO	NO	NO
VR2493S	0x28	YES	1.65 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Empty OTP samples can be ordered for engineering purposes using part number PVR2493AMSA0AD. Refer to the associated OTP configuration report in the website product page.

Table 2. Orderable part numbers

Part number	Description	Package
MVR2491AMSF2AD	MCX-E + VR249	LQPF48
MVR2493AMSAKAD	MCX-E HVBMS reference designs	
MVR2491AMSA4AD	S32K3 body control module reference design (white board)	
MVR2491AMSA6AD	S32K344 48 V MC development platform	
MVR2492AMSABAD	Aurix TC38, TC29	
MVR2491AMSF1AD	MCX-E315/317 + 24V input systems	
MVR2493AMSA0AD	Superset covering VR2493S devices	
MVR2493AMNA0AD	Superset covering VR2493N devices	
MVR2490AMNA0AD	Superset covering VR2490N devices	
MVR2490AMSA0AD	Superset covering VR2490S devices	
MVR2491AMNA0AD	Superset covering VR2491N devices	
MVR2491AMSA0AD	Superset covering VR2491S devices	
MVR2492AMNA0AD	Superset covering VR2492N devices	
MVR2492AMSA0AD	Superset covering VR2492S devices	
MVR2493AMNA0AD	Superset covering VR2493N devices	
MVR2493AMSA0AD	Superset covering VR2493S devices	

5 Applications

Energy storage

- Battery management system (BMS)
- Battery backup systems
- EV wall chargers

Factory automation

- Safety PLCs
- Industrial motor drivers
- Industrial networking

Industrial robotics

- Autonomous mobile robots
- Collaborative robots
- Humanoid robots

Safety and chassis

- Two wheeler body controller
- Smart junction box

MCU Attach

- MCX-E family / S32K3
- Infineon AURIX family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

6 Simplified application diagrams

Figure 3 shows a simplified block diagram of a typical VR249-based system, such as industrial vehicles, that uses the boost controller to support battery cold-crank events.

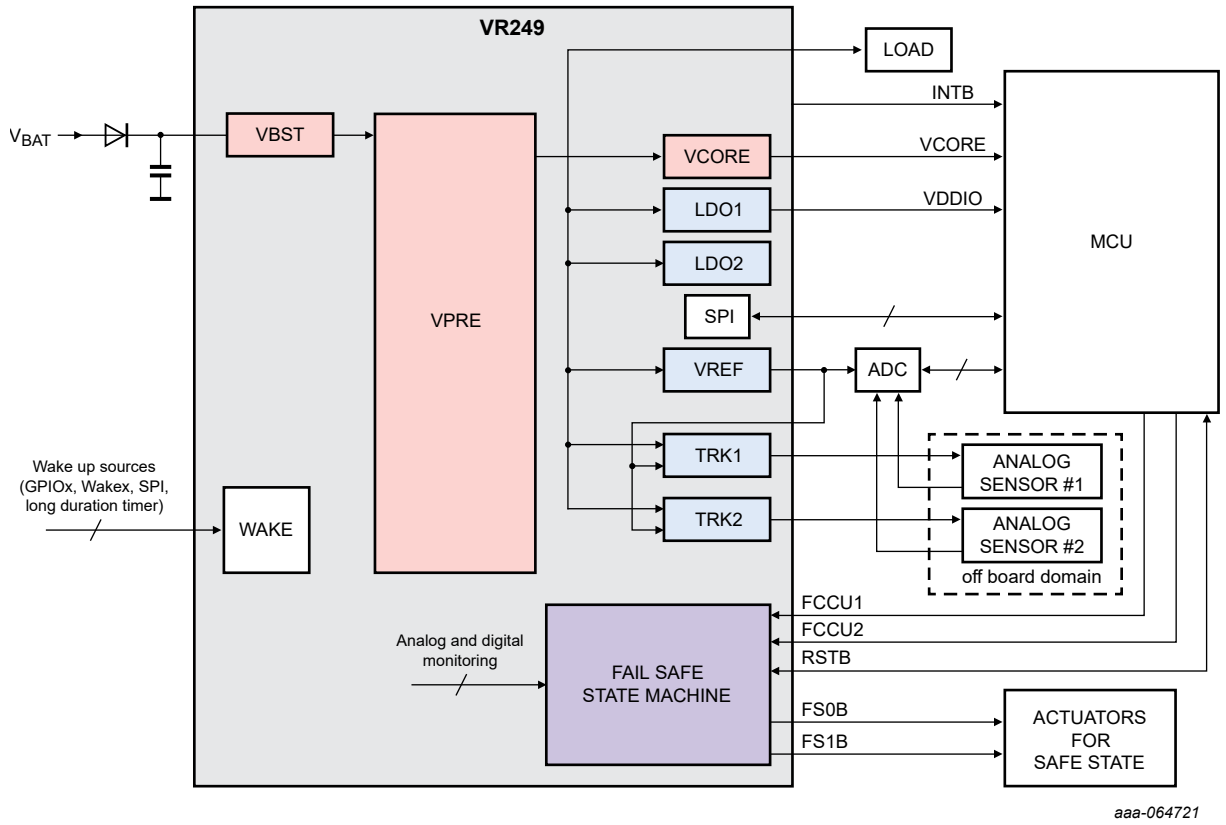

Figure 3. Example of application diagram with VBST as a front-end regulator

Figure 4 shows a simplified block diagram for a typical system with an VR249, using the boost controller to generate a voltage above the high-voltage buck output voltage.

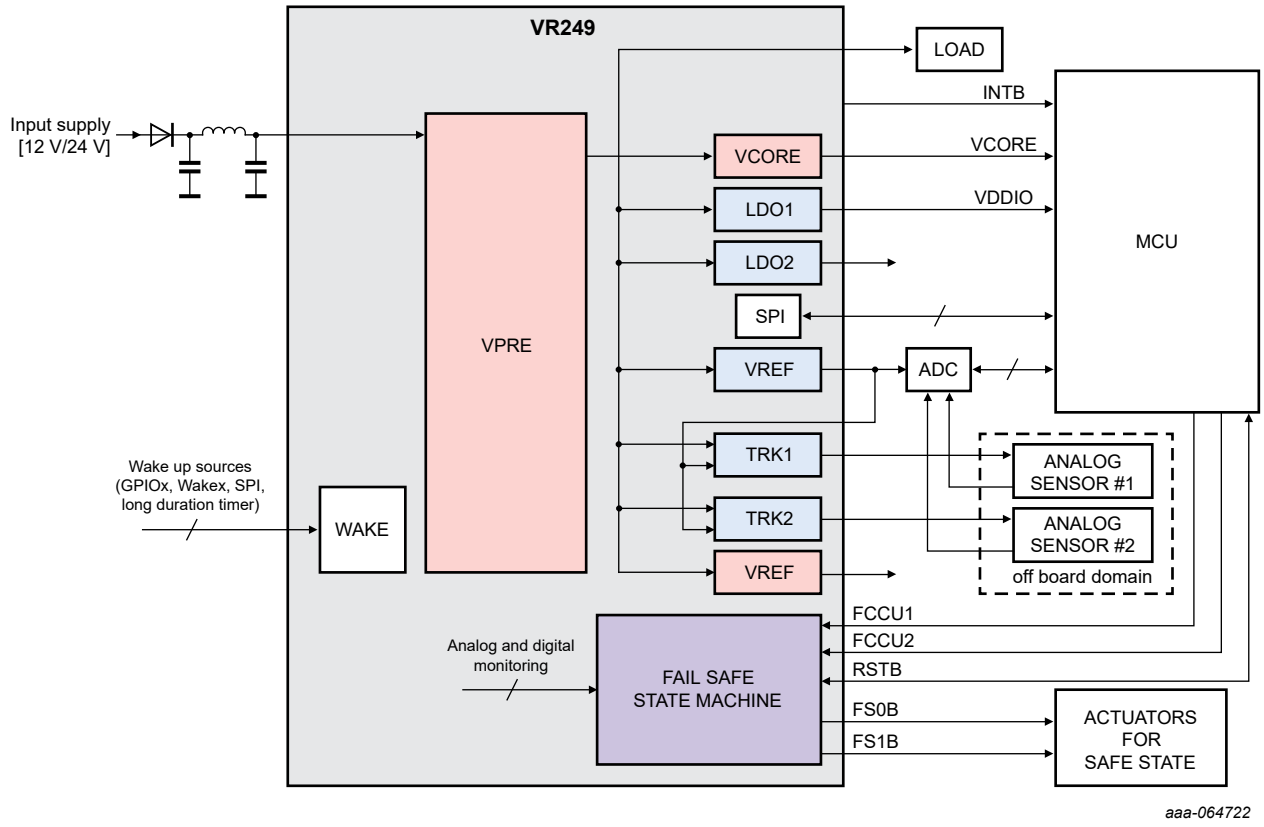

Figure 4. Example of application diagram with VBST as a back-end regulator

7 Block diagram

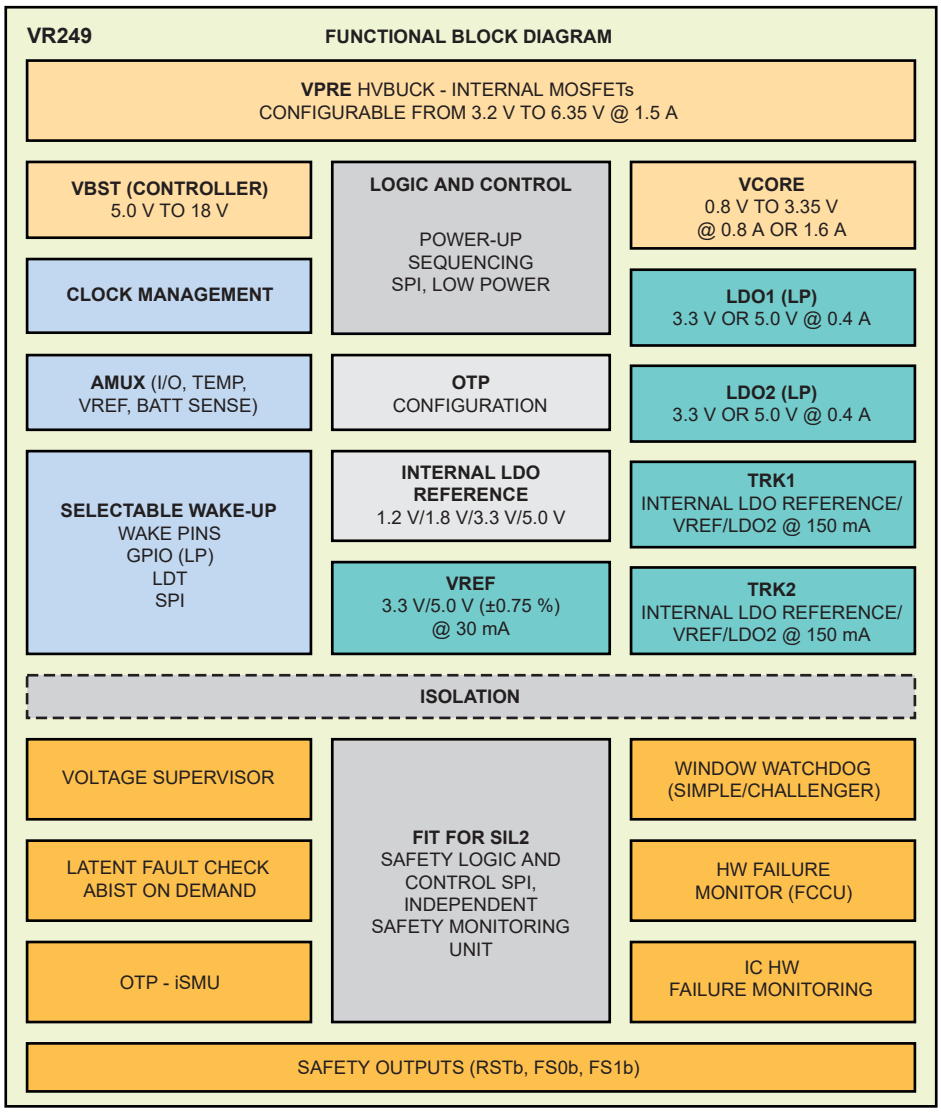

Figure 5. Functional block diagram

8 Pinning information

8.1 Pinning

8.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin Number	Type	Description
VBST_PG	1	Digital output	Power Good signal of VBST
WAKE2	2	Analog input	WAKE2 input pin or ERRMON input
GPIO1	3	Analog output / Digital Input	General Purpose I/O 1 (GPIO1)
TRK1	4	Analog output	TRK1 regulator output
TRK2	5	Analog output	TRK2 regulator output
GPIO2	6	Analog output / Digital Input	General Purpose I/O 2 (GPIO2)
TRKIN	7	Analog input	TRK1, TRK2 and VREF regulators input
VREF	8	Analog output	Voltage reference output (VREF)
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO1 and LDO2 regulator input voltage supply
LDO1OUT	11	Analog output	LDO1 regulator output
FS1B	12	Digital output	Safety output #1 (FS01)
FS0B	13	Digital output	Safety output #0 (FS02)
VMONEXT	14	Analog input	VMON_EXT voltage monitoring input
VMONCORE	15	Analog input	VMON_CORE voltage monitoring input
RSTB	16	Digital input/output	Reset input/output (RSTB)
FCCU1	17	Digital input	Fault Control Collection Unit (FCCU) pin 1
FCCU2	18	Digital input	Fault Control Collection Unit (FCCU) pin 2
GNDFS	19	Ground connection	Ground connection for fail-safe circuitry
GND	20	Ground connection	Ground connection for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI Primary In Secondary out
MOSI	26	Digital input	SPI Primary Out Secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog multiplexer (AMUX) output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin. Used to enter OTP and *debug mode*

Table 3. Pin descriptions*...continued*

Symbol	Pin Number	Type	Description
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best Of Supply (BOS) decoupling output
VMONPRE	36	Analog input	VMON_PRE voltage monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to ground)

9 Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Table 4. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	8.5	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_ FB, VBST_ISH, VBST_ ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EP	DC voltage at GNDFS, GND, GNDSUB pins, and exposed pad (EP)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

10 Electrostatic discharge

Exceeding these ratings may cause a malfunction or permanent damage to the device.

Table 5. Electrostatic discharge

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
VESD_HBM	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
VESD_CDM1	All pins	-500	500	V
VESD_CDM2	Corner pins	-750	750	V
Gun Test				
VESD_CDT1	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
VESD_CDT2	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
VESD_CDT3	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
VESD_CDT4	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
VESD_CDT5	Operating ESD- GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

11 Thermal ratings

Table 6. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
TSTG	Storage temperature	-55	—	150	°C
TWARN	Temperature warning threshold to set TWARN_S SPI bit	145	155	170	°C

Table 7. Thermal resistance (per JEDEC JESD51-2)

Table 7. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
RθJA	Thermal resistance Junction to Ambient[1]	25	°C/W
RθJCBOTTOM	Thermal resistance Junction to Case Bottom (with uniform power dissipation on the silicon die)[2][3]	1.7	°C/W
RθJCTOP	Thermal resistance Junction to Case Top[1][3]	13.5	°C/W
ΨJT	Thermal characterization parameter Junction to Top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

12 Packaging

12.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 8. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

12.2 Package outline

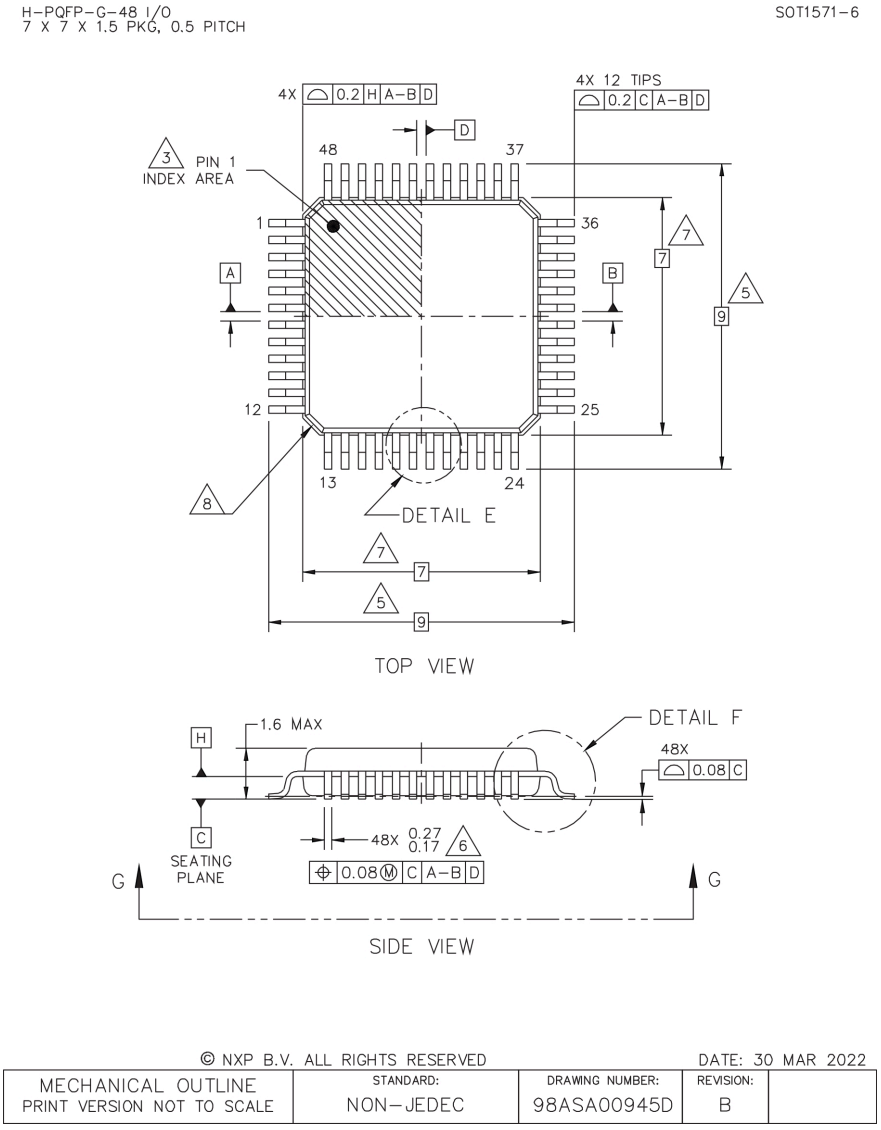

Figure 6. SOT1571-6

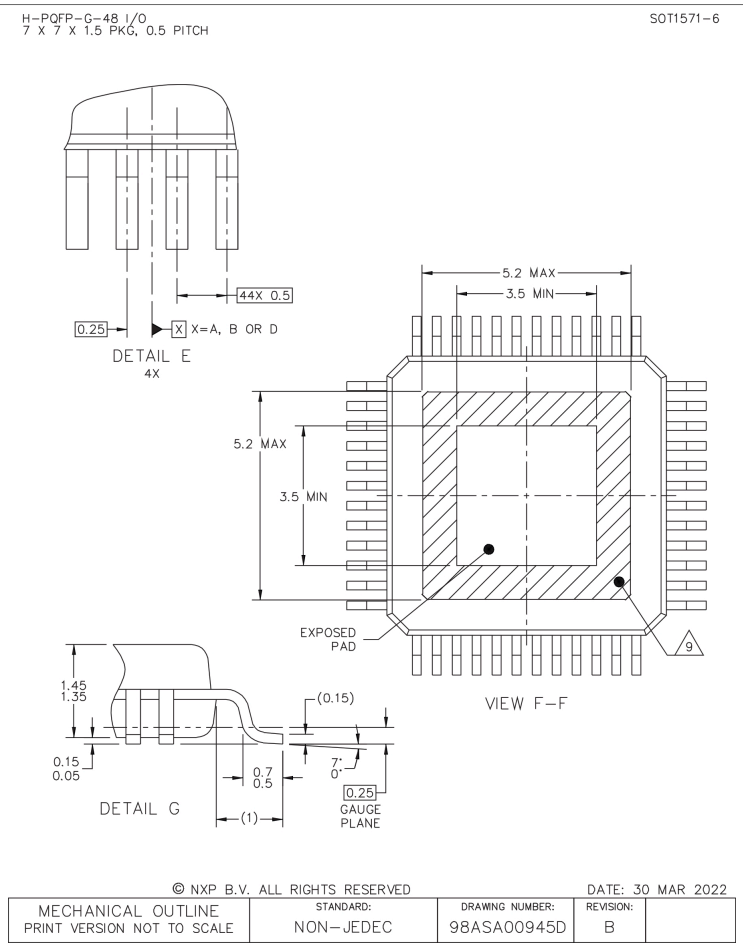

Figure 7. Package outline details (SOT1571-6)

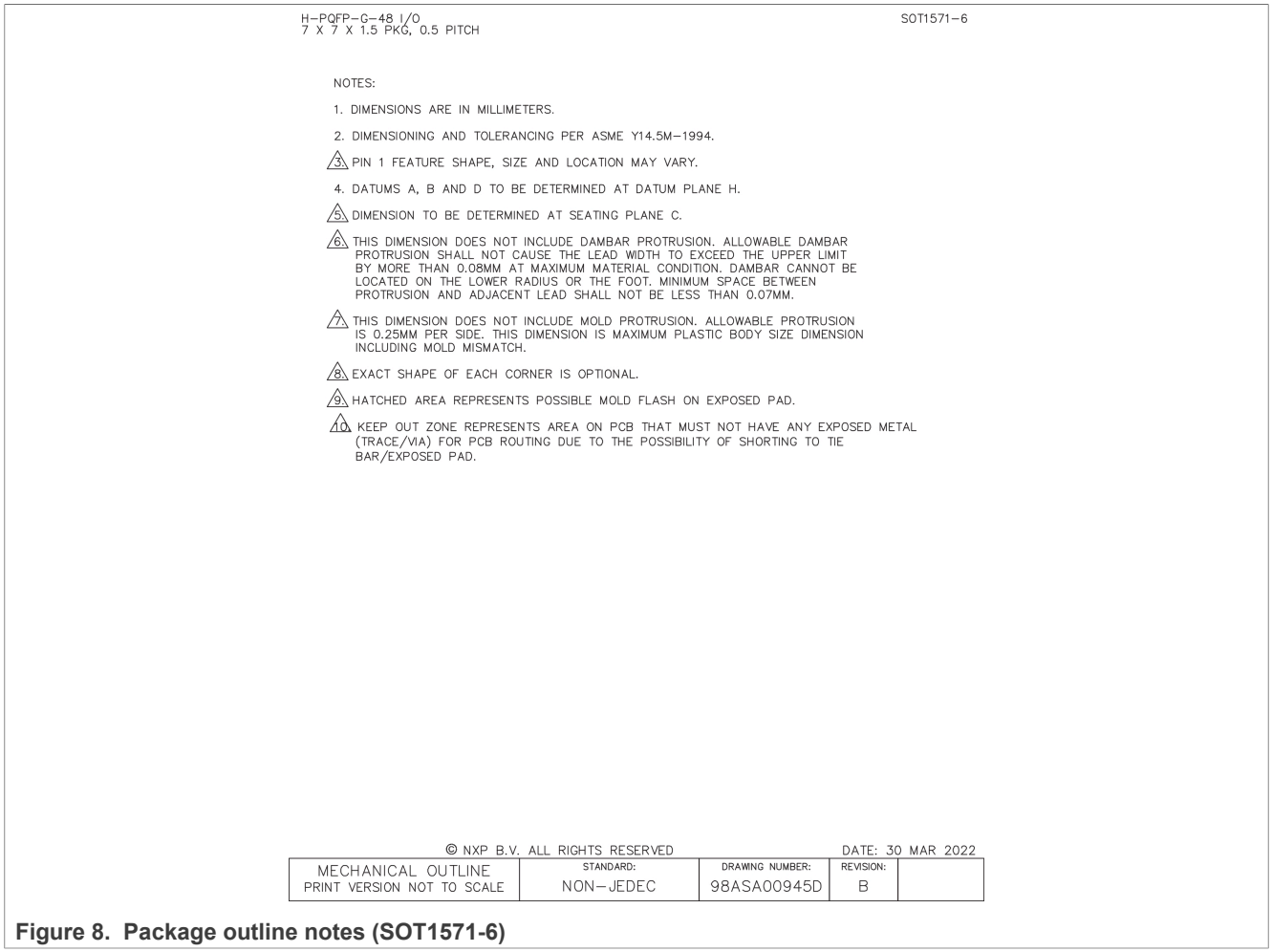

Figure 8. Package outline notes (SOT1571-6)

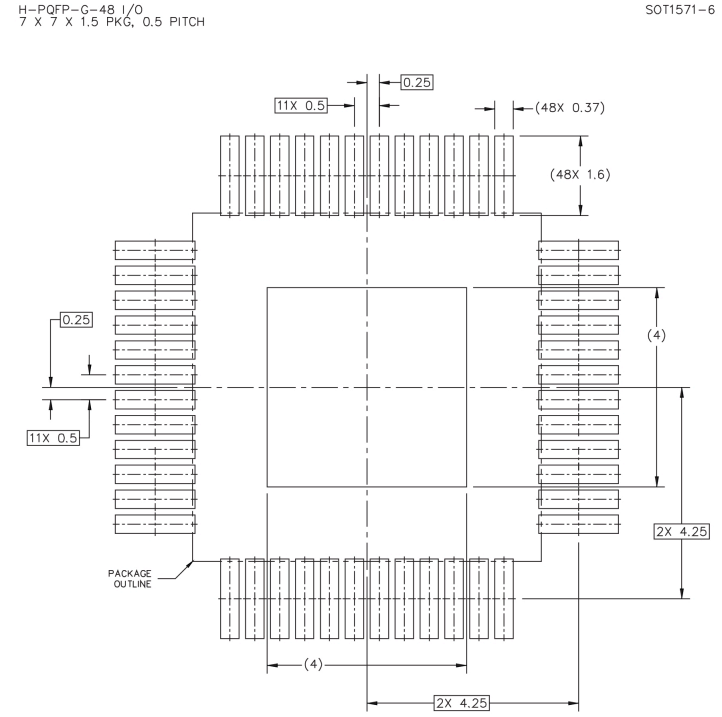

Figure 9. PCB design guidelines - solder mask opening pattern (SOT1571-6)

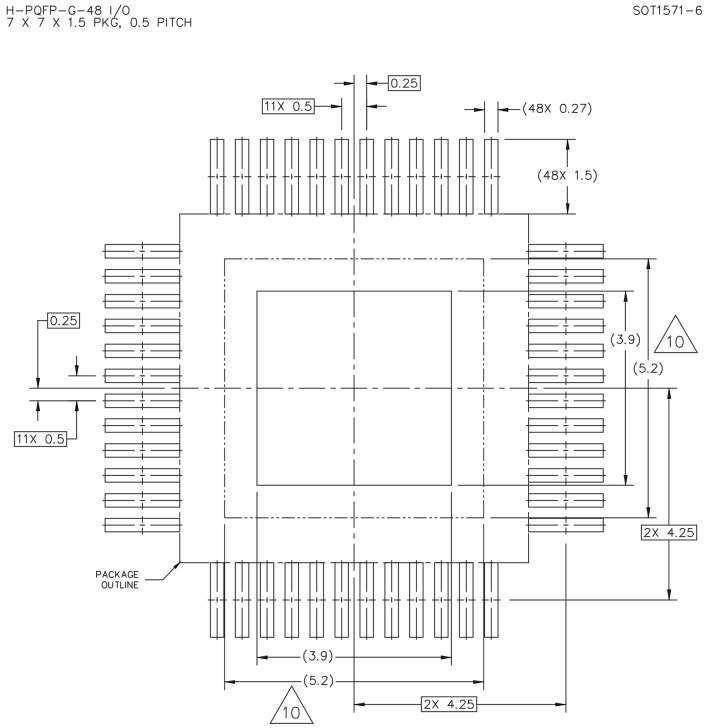

Figure 10. PCB design guidelines - I/O pads and solderable area (SOT1571-6)

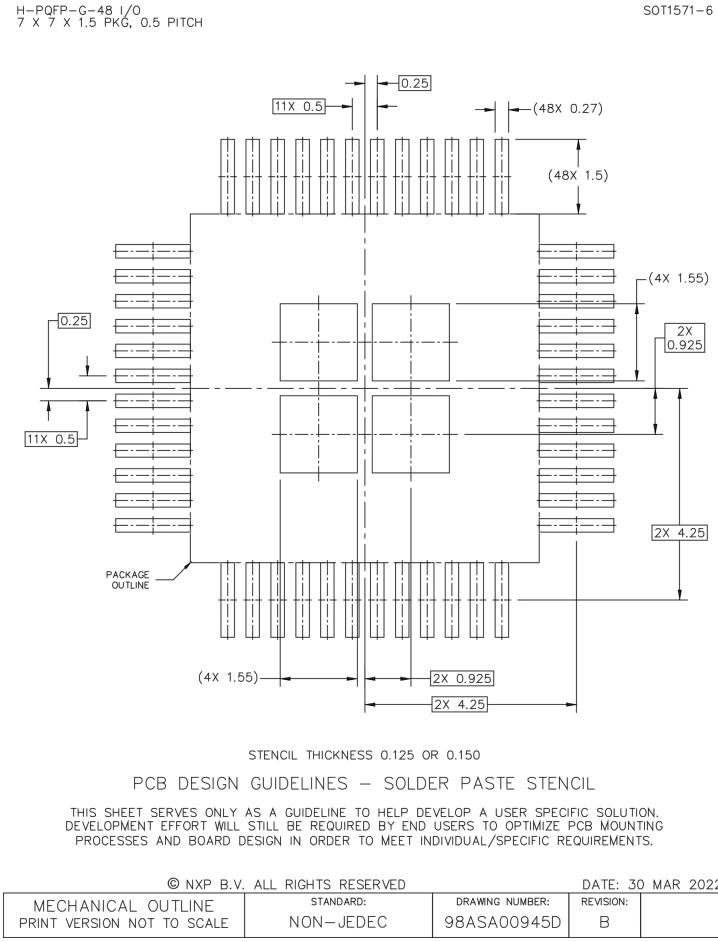

Figure 11. PCB design guidelines - solder paste stencil (SOT1571-6)

13 References

More information will be published on NXP.com

14 Revision history

Table 9. Revision history

Document ID	Release date	Description
VR249_PB.v.1.0	24 March 2026	Initial version

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