Freescale Semiconductor
Product Brief

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PXR40 Product Brief

32-bit Power Architecture® Microcontrollers for Real-Time Applications

The PXR40 series 32-bit microcontrollers provide integrated analog and processing power to give industrial users a reliable, robust controller solution to meet a variety of timing critical application needs, such as motion/motor control, without sacrificing performance during complex operations. Based on Power Architecture®, these system-on-chip devices are 100% user-mode compatible with the classic Power Architecture instruction set.

The e200z7 host processor core of the PXR40 is compatible with the Power Architecture® Book E architecture. It is 100% user-mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the architecture's fit in embedded applications. In addition to the classic PowerPC instruction set, this core also has additional instruction support for digital signal processing (DSP).

The PXR40 has two levels of memory hierarchy, a 16 KB instruction + 16 KB data cache in a Harvard

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architecture bus, and 256 KB of on-chip SRAM. 4 MB of internal flash memory is provided. An external bus interface is also available for special packaged parts to support application development and calibration.

1 Application examples

The PXR40 family's real-time capability makes it suitable for applications such as

- Precision factory control
- Industrial automation
- Industrial transportation
- Motor control/drives
- Medical
- Timing applications

2 Features

This section describes the features of the PXR40.

2.1 PXR40 features

Table 1 displays the PXR40 feature set.

Table 1. PXR40 feature set

Feature	PXR40
Core	e200z7
SIMD	Yes
VLE	Yes
Cache	32 KB (16 KB Instruction/16 KB Data)
Non-maskable interrupt (NMI)	NMI & Critical Interrupt
MMU	64 entry
MPU	Yes
XBAR	5 × 5
Windowing software watchdog	Yes
Nexus	3+
SRAM	256 KB
Flash	4 MB
Flash fetch accelerator	4 × 256 bit (first 1 MB of memory is 4 × 128; last 3 MB are 4 × 256)
External bus	Yes
Calibration bus	16 bit non-muxed 32 bit muxed
DMA	96 channel
DMA Nexus	Class 3
Serial	3
UART_A	Yes

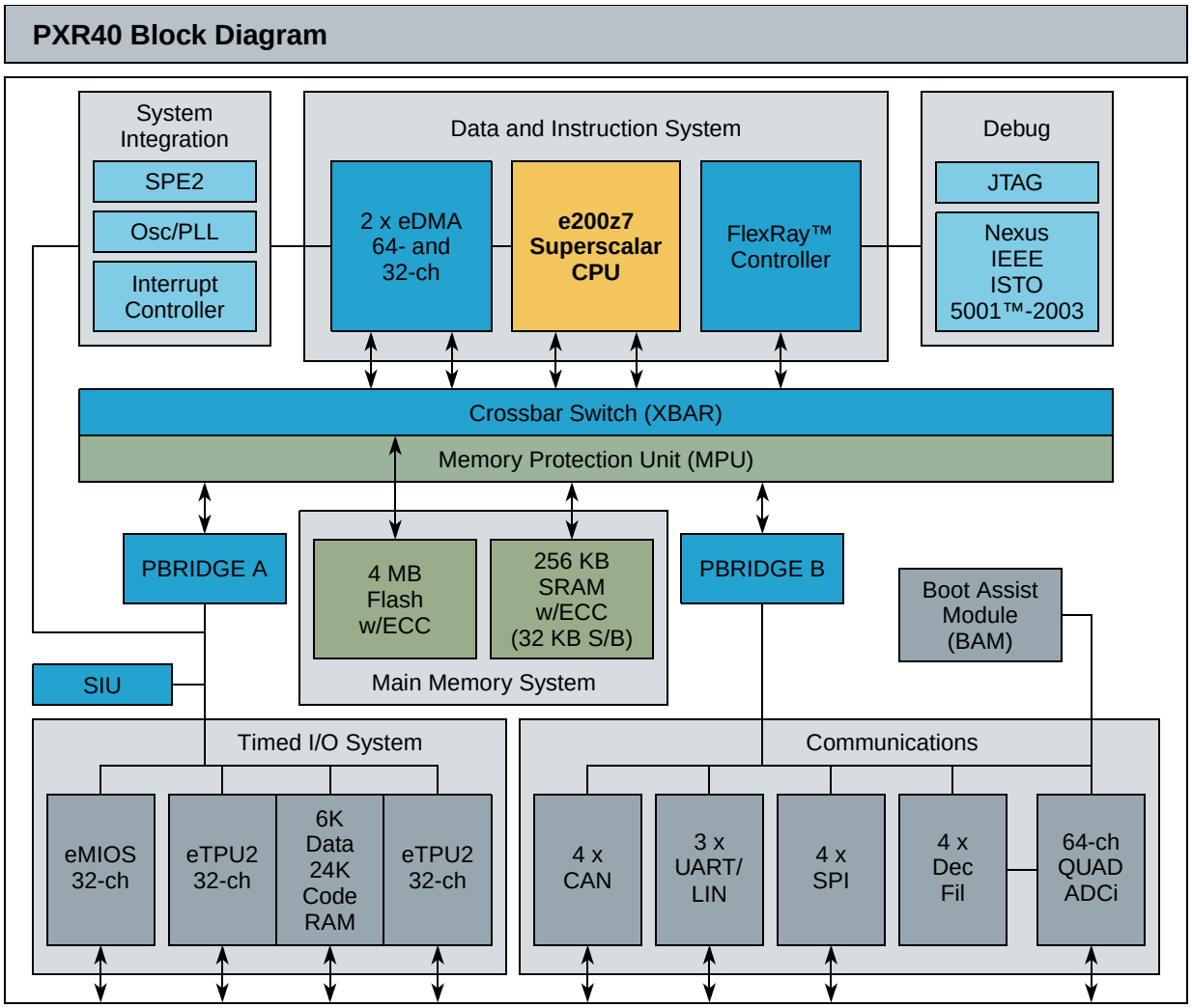
Table 1. PXR40 feature set (continued)

Feature	PXR40
UART_B	Yes
UART_C	Yes
Microsecond bus uplink	Yes
CAN	4
CAN_A	64 message buffers
CAN_B	64 message buffers
CAN_C	64 message buffers
CAN_D	64 message buffers
CAN_E	No
SPI	4
SPI_A	Yes
SPI_B	Yes
SPI_C	Yes
SPI_D	Yes
FlexRay	Yes
Ethernet	No
System timers	4 PIT chan 4 SWT 1 Watchdog
eMIOS	32 channel
eTPU	64 channel
eTPU_A	Yes (eTPU2)
eTPU_B	Yes (eTPU2)
Code memory	24 KB
Data memory	6 KB
Interrupt controller	448
ADC	64 channel
eQADC_A	Yes
eQADC_B	Yes
Temperature sensor	Yes
Variable gain amp.	Yes
Decimation filter	Yes (8 on eQADC_B)
Sensor diagnostics	Yes
PLL	FM
VRC	Yes
Supplies	5V
Low Power Modes	Stop Mode Slow Mode

Note: 3.3 V is required for certain IO segments only during debug/development (e.g., Nexus 3 trace and bus)

2.2 PXR40 block diagram

Figure 1 shows a top-level block diagram of the PXR40 microcontrollers.



ADC – Analog-to-digital converter
ADCi – ADC interface
AIPS – Peripheral I/O bridge
AMux – Analog multiplexer
CAN – Controller area network
DECFIL – Decimation filter
EBI – External bus interface
ECSM – Error correction status module
eDMA2 – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued A/D converter module
eTPU2 – Enhanced time processing unit 2
MMU – Memory management unit
MPU – Memory protection unit
PBRIDGE – Peripheral I/O bridge
S/B – Stand-by
SIU – System integration unit
SPE2 – Signal processing engine 2
SPI – Serial peripheral interface controller
SRAM – General-purpose static RAM
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VLE – Variable length instruction encoding

Figure 1. PXR40 block diagram

2.3 Critical performance parameters

The critical performance parameters of the PXR40 feature the following:

- Maximum CPU frequency: 264 MHz
  - Platform and peripheral modules typically run at half of the CPU frequency
  - Some peripheral modules (including the eTPU modules) support a full frequency mode with a maximum operating frequency of 200 MHz
- Temperature range: –40° to 105 °C
- Nominal power dissipation is less than 1.4 W, while enhancements to allow reduced power operation using clock gating are included
- Separate power supply available for stand-by operation of a portion of SRAM

2.3.1 Low-power modes

The PXR40 includes two special modes to allow reduction of application power consumption:

- Slow mode: Allows the device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled by software.
- Stop mode: System clock stopped to most modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time.

2.4 Package

The PXR40 is offered in a 416-ball PBGA, 1 mm ball pitch, 27 mm × 27 mm outline (no EBI) package type.

2.5 Module features

The following sections provide more details of the modules implemented on the PXR40.

2.5.1 High-performance e200z7 core processor

The e200z7 core includes the following features:

- Dual-issue, 32-bit Power Architecture® CPU
- Supports the 32-bit Power Architecture Book E programmer’s model
- 64-bit general-purpose registers (GPRs) support vector instructions defined by the SPE2 APU
  - All arithmetic instructions that execute in the core operate on data in the GPRs
- Enhanced signal processing extension (SPE2) APU supports real-time fixed point and single-precision embedded numerics operations using the GPRs
- Variable length encoding (VLE) enhancements
  - Allows optional encoding of mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint

  - Minimizes impact on performance
- Six read and three write operations per clock
  - Integrates a pair of integer execution units, a branch control unit, instruction fetch unit and load/store unit, and a multi-ported register file
- Branch target prefetching performed by the branch unit allows single-cycle branches in many cases
- 16 KB instruction cache and 16 KB data cache, both supporting error detection hardware.
- Memory management unit (MMU) with 64-entry fully-associative translation look-aside buffer (TLB)
- Nexus Class 3+ module
- Supports non-maskable interrupt (completely un-maskable and not guaranteed to be recoverable) and critical interrupt (an interrupt that can be masked and is guaranteed to be recoverable) sources
  - Routed from a single package pin, via edge detection logic in the SIU, to the CPU
- An additional Wait for Interrupt instruction:
  - Used in conjunction with low power STOP mode
  - Instruction stops the system clock
  - An external interrupt source or the system wake-up timer restart the system clock, allowing the CPU to service the interrupt
- Includes multiple input signature register (MISR) hardware which can be accessed by software to implement CPU self test functionality

2.5.2 On-chip flash memory

The PXR40 flash memory module provides the following:

- 4 MB of programmable, non-volatile, flash memory
  - Nonvolatile memory (NVM) can be used for instruction and/or data storage
- A fetch accelerator optimizes the performance of the flash memory array to match the CPU architecture
  - Architected to optimize the performance of the flash memory with the CPU to provide single-cycle random access to the flash memory when in full clock mode, and two-cycle access when in double clock mode
  - Configurable read buffering and line prefetch support
- An interface between the system bus and a dedicated flash memory array controller
- Supports a 64-bit data bus width at the system bus port for CPU loads, DMA transfers and CPU instruction fetch
  - Byte, halfword, word, and doubleword reads are supported
  - Only aligned word and doubleword writes are supported
- Hardware and software configurable read and write access protections on a per-master basis
- Pipelined interface to the flash memory array controller allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash memory array designs
- Configurable access timing allowing use in a wide range of system frequencies

- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- ECC with single-bit correction, double-bit detection
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address (due to ECC)
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

2.5.3 General-purpose static RAM (SRAM)

The PXR40 SRAM module provides an internal general-purpose 256 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB block powered by separate supply for standby operation (contents retained)
- Byte, halfword, word, and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 64-bit data elements
- ECC single-bit error corrections are optionally visible to software

2.5.4 Error correction status module (ECSM)

The error correction status module (ECSM) provides the following:

- Status information regarding platform memory errors reported by error detection code (EDC) and error correcting code (ECC) hardware
  - Single-bit correction reporting for SRAM and flash memory
  - Multi-bit error reporting
- Includes facilities to allow CPU software to test the error ECC and EDC operation for on-chip memories by supporting injection of arbitrary error patterns

2.5.5 Enhanced modular input output system (Timer—eMIOS)

The eMIOS module provides the functionality to generate or measure time events. A unified channel (UC) module is employed that provides a superset of the functionality of all of the MIOS channels used on MPC5500 family devices, while providing a consistent user interface. This allows more flexibility as each unified channel can be programmed for different functions in different applications. To identify as many as two timed events, each UC contains two comparators, a time base selector and registers. This structure is able to produce match-events, which can be configured to measure or generate a waveform.

Alternatively, input events can be used to capture the time base, allowing measurement of an input signal. The eMIOS provides the following features:

- 32 unified channels, featuring:
  - 24-bit registers for capture/match values
  - 24-bit internal counter
  - Global prescaler
  - Pin for input/output (each channel signal is routed to a pin, however, most pins are also multiplexed with other signals)
  - Selectable time base
  - Can generate its own time base
- Five 24-bit wide counter buses
  - Counter bus A can be driven by unified channel 23
  - Counter bus B, C, D and E are driven by unified channels 0, 8, 16, and 24, respectively
  - Counter bus A can be shared among all unified channels. UCs 0 to 7, 8 to 15, 16 to 23, and 24 to 31 can share counter buses B, C, D and E, respectively
- Shared time bases with the eTPU
- Synchronization among internal and external time bases
- Shadow FLAG register
- State of block can be frozen for debug purposes

2.5.6 Enhanced timing processor unit (eTPU2)

Two eTPU2 modules are available on the PXR40. The eTPU2 is the second generation of the enhanced timing co-processors (eTPU) that were used on the MPC5500 family. eTPU2 is fully upward compatible with eTPU, runs the same binary code image, and can be used with the same tool suite. eTPU2 includes many enhancements to improve efficiency of compilers, functionality, ease of programming and operability while maintaining the same overall architecture. Some of these enhancements may be accessed using the existing compiler tool chain, while other enhancements require updates to the compiler.

The eTPU2 includes these distinctive features:

- 32 standard channels, each channel is associated with one input and one output signal
- Two independent 24-bit time bases for channel synchronization:
- Event-triggered microengine
  - 24 KB of code memory (SCM)
  - 6 KB of shared parameter (data) RAM (SPRAM)
- Resource sharing features support channel use of common channel registers, memory and microengine time
  - Hardware scheduler works as a task management unit, dispatching event service routines by pre-defined, host-configured priority

  - Channel context switch time is six system cycles. Each channel has its own context of static data memory and timer hardware resources consisting of programmable flags, timer control and status hardware
  - SPRAM shared between host CPU and eTPU, supporting communication either between channels and host or inter-channel
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
  - Enhancements to DMA and interrupt structure to allow any channel to assert any interrupt source or DMA trigger[1]
- Test and development support features:
  - IEEE-ISTO 5001-2003 standard class 3 compliant for the eTPU (Nexus)
  - Data trace via data write messaging and data read messaging
  - Ownership trace via ownership trace messaging (OTM)
  - Program trace via branch trace messaging
  - Watchpoint messaging via the auxiliary port
  - SCM continuous signature-check built-in self test (MISC — multiple input signature calculator), runs concurrently with eTPU normal operation

2.5.7 Software watchdog timer (SWT)

The software watchdog timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. When enabled, the SWT requires periodic execution of a watchdog servicing sequence. Writing the sequence resets the timer to a specified time-out period. If this servicing action does not occur before the timer expires the SWT generates an interrupt or hardware reset. The SWT can be configured to generate a reset or interrupt on an initial time-out, a reset is always generated on a second consecutive time-out.

The following features are implemented:

- 32-bit time-out register to set the time-out period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

2.5.8 Periodic interrupt timer (PIT)

The periodic interrupt timer (PIT) is an array of timers that can be used to generate interrupts and trigger DMA channels. It also provides a dedicated real-time interrupt timer (RTI), which runs on a separate clock and can be used for system wake-up.

The following features are implemented:

- Four independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- Three channels clocked from system clock
- One channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when system enters stop mode. Used to restart system clock after predefined time-out period
- Each channel can optionally generate interrupt request when timer reaches zero
- Channels can optionally produce trigger event when timer reaches zero (used to trigger eQADC queues)

2.5.9 System timer module (STM)

The system timer module (STM) is a 32-bit timer designed to support commonly required operating system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel.

The following features are implemented:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

2.5.10 Enhanced queued analog to digital converter (eQADC)

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The two eQADCs on the PXR40 provide a parallel interface to four on-chip analog to digital converters (ADC), and a single-master to single-slave serial interface to an off-chip external device.

The ADCs include features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pullup and pulldown resistors for biasing and sensor diagnostics.

eQADC_B also integrates four programmable decimation filters capable of taking in ADC conversion results at a high rate, passing them through a hardware low-pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise, while providing a reduced sample rate output to minimize the amount of DSP processing bandwidth required to fully process the digitized waveform.

The eQADCs provide the following features:

- Quad on-chip ADCs

  - 4 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    - 12-bit conversion time as low as1 µS (as fast as 1 M sample/sec)
    - 10-bit conversion time as low as 867 nS (as fast as 1.2 M sample/sec)
    - 8-bit conversion time as low as 733 nS (as fast as 1.4 M sample/sec)
  - Accuracy as high as 10-bit accuracy at 500 K sample/sec and 8-bit accuracy at 1 M sample/sec
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Supports both right-justified unsigned and signed formats for conversion results
- 64 input channels, including 16 channels which can each be converted simultaneously by each eQADC
- Eight additional internal channels for measuring control and monitoring voltages inside the device
  - Including core voltage, I/O voltage, and low-voltage interrupt (LVI) voltages
- As many as eight inputs can be configured as four pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
- Four decimation filters
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Fully programmable 4th order IIR or 8th order FIR
  - Saturated or non-saturated modes
  - Programmable rounding (convergent; two’s complement; truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Six priority-based queues per ADC
- Trigger sources include software, timer channels and input pins
- eTPU result interface
  - Allows any ADC result to be exported to eTPU for use with reaction channels
- Support for an additional 64 – 8 = 56 channels via external multiplexing

2.5.11 Serial peripheral interface module (SPI)

The PXR40 includes four serial peripheral interface (SPI) blocks that provide a synchronous serial interface for communication to external devices. The SPI features the following:

- Supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers
- Channels and register content are transmitted using a SPI protocol
  - The protocol is completely configurable for baud rate, polarity, phase, frame length, chip select assertion, etc.
  - Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals
- Can be configured to serialize data to an external device that is compatible with the Microsecond Bus protocol
- SPI pins support 5 V logic levels or low voltage differential signalling (LVDS) to improve high-speed operation on data and clock signals

The SPIs have multiple configurations:

- Serial peripheral interface (SPI) configuration where the SPI operates as an up-to-16-bit SPI with support for queues
- Deserial serial interface (DSI) configuration where the SPI serializes as many as 32 bits from eTPU, eMIOS, or GPIO output channels and deserializes the received data by placing it on the eTPU, eMIOS, or GPIO input channels
- Combined serial interface (CSI) configuration where the SPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames
- Enhanced deserial serial interface (DSI) configuration where SPI serializes as many as 32 bits with three possible sources per bit
  - eTPU, eMIOS, new virtual GPIO registers as possible bit source
  - Programmable inter-frame gap in continuous mode
  - Bit source selection allows microsecond bus downlink with command or data frames as large as 32 bits
  - Microsecond bus dual receiver mode

For queued operations, the SPI queues reside in system memory external to the SPI. Data transfers between the memory and the SPI FIFOs are accomplished through the use of the eDMA2 controller or through host software.

2.5.12 Serial communication interface module (UART)

The PXR40 includes three serial communications interface (UART) modules. Each UART allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to local interconnect network (LIN) slave devices.

The serial communication interface module offers the following:

- UART features:

- Full-duplex operation
- Standard non return-to-zero (NRZ) mark/space format
- Data buffers with 4-byte receive, 4-byte transmit
- Configurable word length (8-bit or 9-bit words)
- Error detection and flagging
  - Parity, noise and framing errors
- Interrupt driven operation with 4 interrupts sources
- Separate transmitter and receiver CPU interrupt sources
- 16-bit programmable baud-rate modulus counter and 16-bit fractional
- 2 receiver wake-up methods

- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and up to eight data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
  - Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features
    - Loop back
    - Self Test
    - LIN bus stuck dominant detection
  - Interrupt driven operation with 16 interrupt sources
  - LIN slave mode features
    - Autonomous LIN header handling
    - Autonomous LIN response handling
    - Discarding of irrelevant LIN responses using up to 16 ID filters

2.5.13 Controller area network (CAN) module

The PXR40 contains four controller area network (CAN) blocks.

Each CAN module provides the following features:

- 64 message buffers (MB) of zero to eight bytes data length
- Based on and including all existing features of the Freescale TouCAN module
- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames

  - Zero to eight bytes data length
  - Programmable bit rate as fast as 1 Mb/sec
  - Content-related addressing
- Each MB configurable as receive (Rx) or transmit (Tx), all supporting standard and extended messages
- Individual Rx mask registers per message buffer
- Includes 1056 bytes of RAM used for message buffer storage
- Includes 256 bytes of RAM used for individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either eight extended, 16 standard, or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous CAN version
- Programmable clock source to the CAN protocol interface, either bus clock or crystal oscillator
- Unused message buffer and Rx mask register space can be used as general-purpose RAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or local priority on individual Tx message buffers.
- Hardware cancellation on Tx message buffers.
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity

2.5.14 Enhanced direct memory access controller (eDMA2)

The following summarizes the PXR40's implementation of the eDMA2 controller:

- Second-generation modules capable of performing complex data movements via 64 programmable channels (eDMA2-A) and 32 programmable channels (eDMA2-B), without intervention from the host processor
- DMA engine
  - Performs source and destination address calculations
  - Performs data movement operations
- Includes SRAM-based memory containing the transfer control descriptors (TCD) for the channels.
- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes

- TCD organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing
- Channel transfers can be suspended by a higher priority channel
- Nexus data trace support on each DMA

2.5.15 Crossbar switch (XBAR)

The following summarizes the PXR40’s implementation of the crossbar switch:

- Supports simultaneous connections between master ports and slave ports (each master must access a different slave)
- Supports a 32-bit address bus width and a 64-bit data bus width
- Six master ports:
  - e200z7 core complex (two ports)
  - eDMA2 module A
  - eDMA2 module B
  - FlexRay
  - Nexus debug interface (NDI)
- Four slave ports
  - Flash memory
  - SRAM
  - Peripheral bridge A
  - Peripheral bridge B
- Arbitration logic for when a slave port is simultaneously requested by more than one master
- Includes memory protection unit (MPU) hardware to guard against unintended SRAM or peripheral accesses by the CPU, eDMA2 modules, and FlexRay module.

2.5.16 Power management unit (PMU)

The PXR40's power management unit includes the following features:

- Internally the chip has four supply voltages, nominally 5 V, 3.3 V, 1.2 V and V_{STBY}
- Externally 5 V is required with the 3.3 V being supplied by an internal regulator running off the 5 V supply
  - Can also supply 3.3 V externally
- On-chip regulator controller supplies the 1.2 V via external components
- Option to externally supply V_{STBY} when the application requires standby RAM
- All supply voltages have voltage monitors and both the VDD regulator and all monitors except V_{STBY} are adjustable
- The chip uses a protected POR strategy, that is, the chip is guaranteed to run at the voltage point that RESET is released

2.5.17 Interrupt controller (INTC)

The PXR40 implements an interrupt controller that features the following:

- Priority-based preemptive scheduling of interrupt service requests (ISRs), suitable for statically scheduled hard real-time systems
- 448 software-configurable interrupt sources
  - Can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion:
    High priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software-configurable interrupt request to finish the servicing in a lower priority ISR. Therefore these software-configurable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.
- 16 priority levels so that lower priority ISRs do not delay the execution of higher priority ISRs
- Software-configurable priorities of ISR or tasks
  - Modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources
- For high priority interrupt requests, minimized time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR)
- A unique vector for each interrupt request source for quick determination of which ISR needs to be executed
- Support for a critical or non maskable interrupt
  - Non-maskable interrupt (NMI) multiplexed on WKPCFG pin to allow connection to the critical or non maskable input of the CPU core, bypassing the interrupt controller and all multiplexing and selection logic (provides an interrupt request to the core that is higher priority than any other interrupting source in the device)

2.5.18 Frequency-modulated PLL (FMPLL)

The FMPLL allows the user to generate high speed system clocks using a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock to reduce electromagnetic emissions peaks. The PLL multiplication factor and output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency selectable in two ranges:
  - From 4 MHz to 20 MHz
  - From 8 MHz to 40 MHz (when PLLCFG2 pulled high)
- Voltage controlled oscillator (VCO) range from 192 MHz to 680 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without requiring PLL relock
- Three modes of operation:
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation [1]
  - Modulation enabled/disabled through software
  - Triangle wave modulation
  - Programmable modulation depth
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock quality module
  - Optionally causes an interrupt request or system reset if the crystal clock frequency falls outside a predefined range
  - Optionally causes a system reset, or switches the system clock to the crystal clock and causes an interrupt request, if the PLL output clock frequency falls outside a predefined range
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation allows continued operation after failure of crystal clock
- Configuration registers defined as an upwardly compatible superset of MPC5500 FMPLL registers

2.5.19 System Integration Unit (SIU)

The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad

1. You must configure the FMPLL to ensure that the maximum specified system frequency is not exceeded when frequency modulation is enabled.

  - Control of virtual I/O via SPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Sixteen interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical interrupt request
  - Non maskable interrupt request
- GPIO
  - Virtual GPIO via SPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and virtual-GPIO pin
  - Parallel GPIO enables access to as many as eight GPIOs in one write
- Internal multiplexing
  - Allows serial and parallel chaining of SPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and SPI

2.5.20 Boot assist module (BAM)

The BAM is a block of read-only memory containing code that is executed every time the MCU is powered-on or reset in normal mode. The BAM supports multiple boot modes:

- Booting from internal flash memory
- Serial boot loading (a program is downloaded into on-chip general-purpose SRAM via UART or the CAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from flash memory (which may be external to the device) and configures the PXR40 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical addresses to logical addresses with minimum address translation
- Sets up the MMU to allow application boot code to execute as either Classic Power Architecture Book E code (default) or as Freescale VLE code
- Location and detection of application boot code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid
- Supports software-programmable 64-bit password protection for serial boot mode
- Autobaud function in SCI and CAN download mode[1]

- Supports censorship protection for internal flash memory
- Provides an option to enable the software watchdog timer

2.5.21 Dual-channel FlexRay controller

The PXR40 contains one dual-channel FlexRay controller. The controller fully implements the FlexRay Protocol Specification Version 2.1 Rev A. The FlexRay protocol is designed to facilitate implementation of fault tolerant, time-triggered, and highly dependable control systems by offering a fault tolerant clock synchronization mechanism. The FlexRay protocol maintains the global time across the functional nodes of a network with a precision (jitter) of maximum 1 µs at a data rate of 10 Mbit/sec and redundant communication channels.

The FlexRay controller provides the following features:

- FlexRay Communications System Protocol Specification, Version 2.1 Rev A compliant protocol implementation
- FlexRay Communications System Electrical Physical Layer Specification, Version 2.1 Rev A compliant bus driver interface
- Single channel support
  - FlexRay Port A can be configured to be connected either to physical FlexRay channel A or physical FlexRay channel B.
- FlexRay bus data rates of 10 Mbit/sec, 8 Mbit/sec, 5 Mbit/sec, and 2.5 Mbit/sec supported
- 128 configurable message buffers with
  - Individual frame ID filtering
  - Individual channel ID filtering
  - Individual cycle counter filtering
- Message buffer header, status and payload data stored in dedicated FlexRay memory
  - Allows for flexible and efficient message buffer implementation
  - Consistent data access ensured by means of buffer locking scheme
  - Application can lock multiple buffers at the same time
- Size of message buffer payload data section configurable from 0 to 254 bytes
- Two independent message buffer segments with configurable size of payload data section
  - Each segment can contain message buffers assigned to the static segment and message buffers assigned to the dynamic segment at the same time
- Zero padding for transmit message buffers in static segment
  - Applied when the frame payload length exceeds the size of the message buffer data section
- Transmit message buffers configurable with state/event semantics
- Message buffers can be configured as
  - Receive message buffer
  - Single-buffered transmit message buffer
  - Double-buffered transmit message buffer (combines two single buffered message buffer)

1. Feature available only on revision 2 release of device.

- Individual message buffer reconfiguration supported
  - Means provided to safely disable individual message buffers
  - Disabled message buffers can be reconfigured
- Two independent receive FIFOs
  - One receive FIFO per channel
  - As many as 255 entries for each FIFO
  - Global frame ID filtering, based on both value/mask filters and range filters
  - Global channel ID filtering
  - Global message ID filtering for the dynamic segment
- Four configurable slot error counters
- Four dedicated slot status indicators
  - Used to observe slots without using receive message buffers
- Measured value indicators for the clock synchronization
  - Internal synchronization frame ID and synchronization frame measurement tables can be copied into the FlexRay memory
- Fractional macroticks are supported for clock correction
- Maskable interrupt sources provided via individual and combined interrupt lines
- One absolute timer
- One timer that can be configured as absolute or relative
- Nexus data trace support

2.5.22 JTAG controller (JTAGC)

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 and IEEE 1149.7 standards, and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface five pins (JCOMP, TDI, TMS, TCK, and TDO)
- IEEE 1149.7 Serial JTAG Test Access Port interface three pins (JCOMP, TMS, TCK)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE, ACCESS_AUX_TAP_eTPU, ACCESS_AUX_TAP_DMAAN3, ACCESS_AUX_TAP_DMABN3, ACCESS_AUX_TAP_FLEXRAY
- Three test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.

- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.
- Censorship inhibit register
  - 64-bit censorship password register
  - If the external tool writes a 64-bit password that matches the serial boot password stored in the internal flash memory shadow row, censorship is disabled until the next JTAG reset

2.5.23 Nexus

The Nexus debug interface (NDI) block provides real-time development support capabilities for the PXR40 in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the PXR40. The NDI block interfaces to the host processor, the eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCU's internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG-only mode using only the JTAG pins. Nexus also provides data trace support for flexray and both eDMA2s. The following features are implemented:

- 23 or 27 full duplex pin interface for medium and high visibility throughput
  - One of two modes selected by register configuration:
    - Reduced-port mode (RPM) comprises 12 MDO (message data out) pins
    - Full-port mode (FPM) comprises 16 MDO pins
  - Auxiliary output port
- Debug support pins
  - One MCKO (message clock out) pin
  - 12 or 16 MDO (message data out) pins
  - Two $\overline{\text{MSEO}}$ (message start/end out) pins
  - One $\overline{\text{RDY}}$ (ready) pin
  - One $\overline{\text{EVTO}}$ (event out) pin
    - Auxiliary input port
  - One $\overline{\text{EVTI}}$ (event in) pin
  - 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK) or 3-pin (JCOMP, TMS, and TCK)
  - Reduced-pin JTAG mode as per IEEE 1149.7
- Host processor (e200z7) standard class 3 compliant
- eTPU development support standard class 3 compliant
- Supports data trace for the FlexRay controller and both eDMA2 modules
- Run-time access to the on-chip memory map via the Nexus read/write access protocol
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- The NDI block reset is controlled with JCOMP, power-on reset, and the TAP state machine. All these sources are independent of system reset.

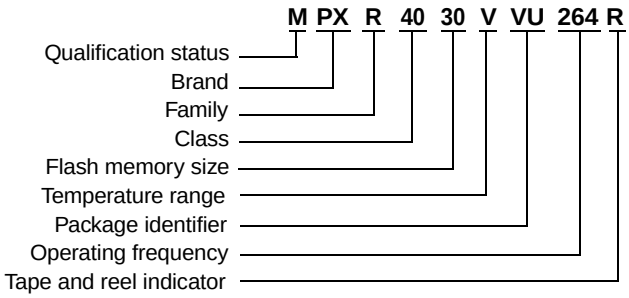
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

3 Developer support

This family of MCUs is suppported by Freescale's Tower Development System as well as a broad set of advanced debug and runtime software:

- CodeWarrior
- FreeMaster
- MQX
- RAppID Init
- RAppID Toolbox

4 Orderable parts



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Time Control
S = Safety

Flash Memory Size
30 = 3 MB
40 = 4 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
VU = 416 PBGA

Operating frequency
1 = 150 MHz
2 = 180 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 2 for more information.

Figure 2. PXR40 orderable part number description

Table 2. PXR40 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXR4030VVU264	3 MB / 192 KB	416 PBGA (27 mm x 27 mm)	264
MPXR4040VVU264	4 MB / 256 KB	416 PBGA (27 mm x 27 mm)	264

5 Revision history

Table 3 describes the changes made to this document between revisions.

Table 3. Revision history

Revision (Date)	Description
Rev. 1 (06/2011)	Initial release

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