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MSC8112 Product Brief

Dual Core Digital Signal Processor

The MSC8112 is a highly integrated system-on-a-chip that combines two SC140 extended cores with a variety of interfaces. The raw processing power of this highly integrated system-on-a-chip device enables developers to create next-generation networking products that offer tremendous channel densities while maintaining system flexibility, scalability, and upgradeability. The MSC8112 is offered with a core speed of 300 MHz. The MSC8112 targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8112 delivers enhanced performance while maintaining low power dissipation and greatly reduces system cost.

Contents

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1 Example Application: 336 G.711-Channel Media Gateway

The Media Gateway application shown in **Figure 1** can process ~336 G.711 channels. The IP interface uses either UTOPIA or 100BaseT connected to the MSC8103 device that is the array aggregator. The MSC8112 performs the translation between the packet world and the PSTN world and the synchronous data is connected to the PSTN world through the TDM interface with a time slot assigner translating to protocols such as H.110 and MVIP. The MSC8103 DMA controller directly accesses the M1 and the M2 memories of the MSC8112 device through its local bus using its UPM. In parallel, it uses its system interface for accessing its SDRAM and flash. In this application 32-bit data DSI is sufficient, so the MSC8112 system bus can support up to 64-bit data. The user can use either a 32-bit wide SDRAM or two 32-bit SDRAM devices for storing channels and code, depending on the bandwidth need. The controller in this application is the MPC8260, and it accesses the MSC8103 HDI16 through its local bus while locating its memories on its system bus. Note that when premium voice is processed, each MSC8112 device performs fewer channels, so more devices can be connected to the MSC8103 device.

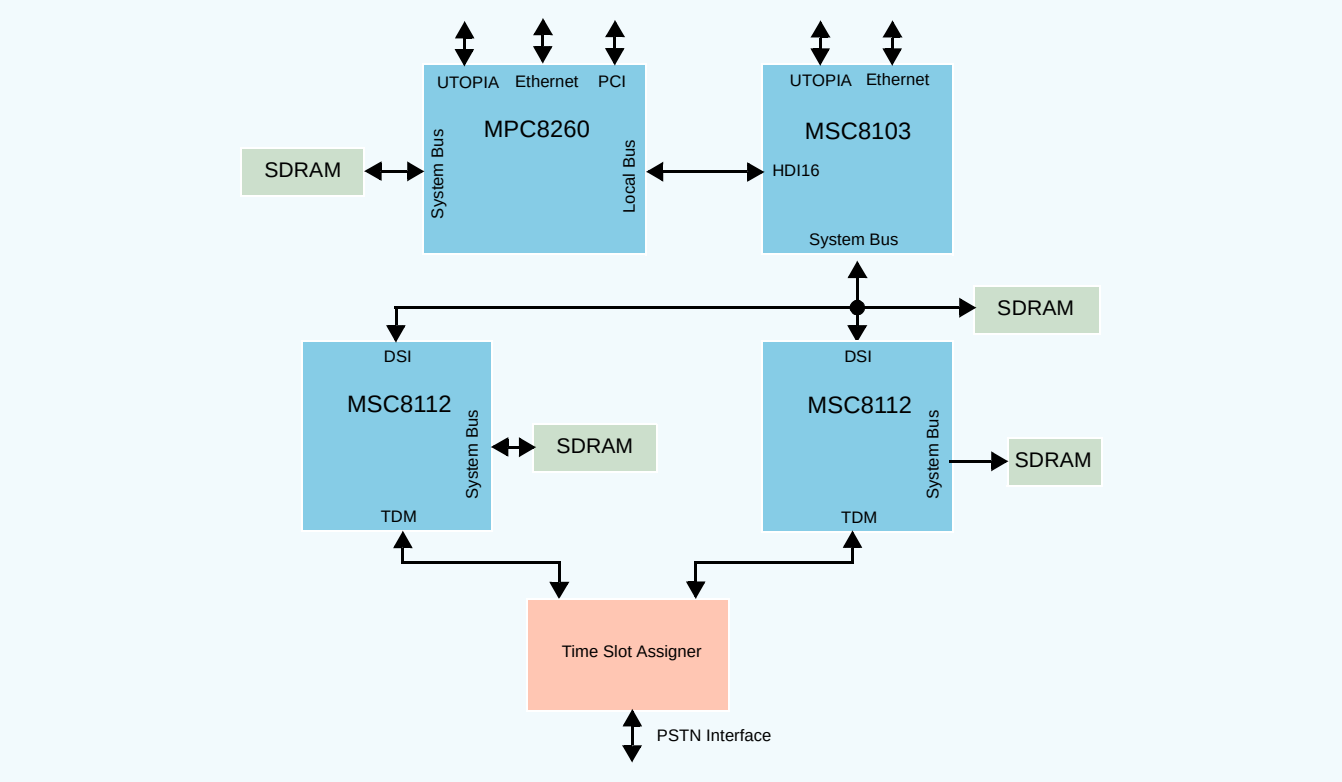


Figure 1. 672 G.711-Channel Media Gateway

2 Features

The MSC8112 device targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications.

2.1 Block Diagram

The MSC8112 is a highly integrated system-on-a-chip that combines two SC140 extended cores with an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), an Ethernet interface, and a multi-channel DMA engine. Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers.

A block diagram of the MSC8112 is shown in **Figure 2**. A separate block diagram for the extended cores is shown in **Figure 3**.

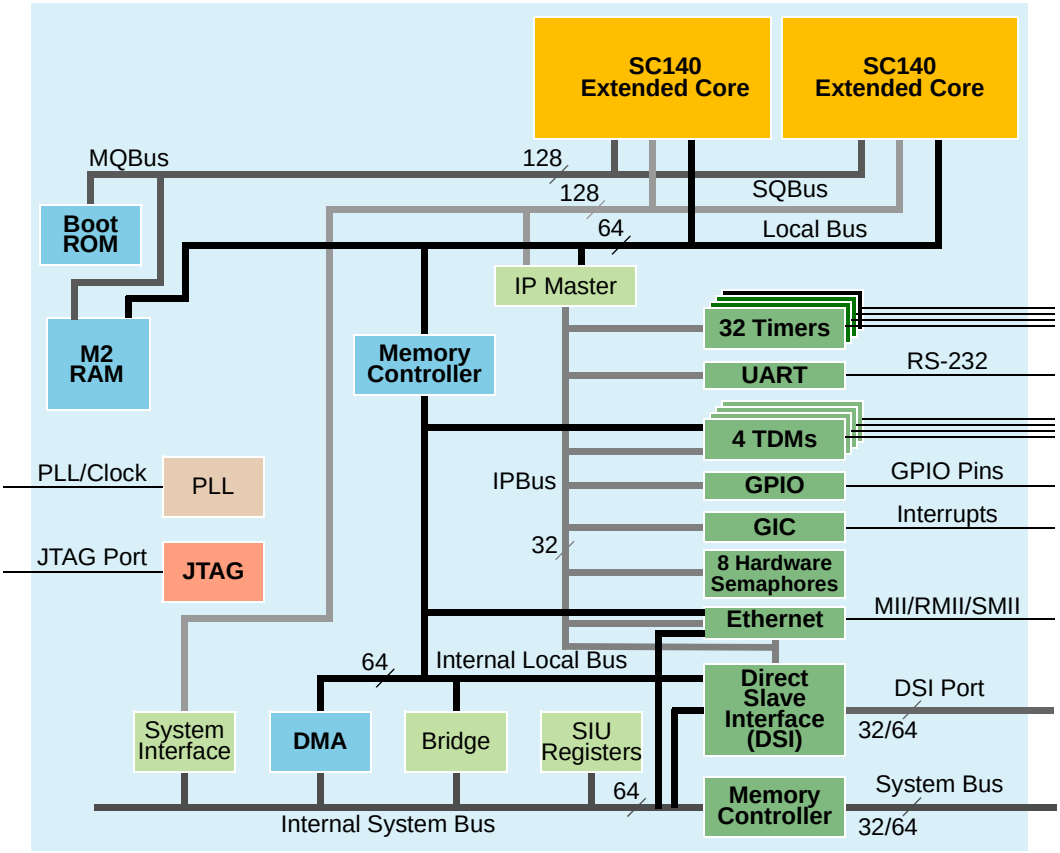
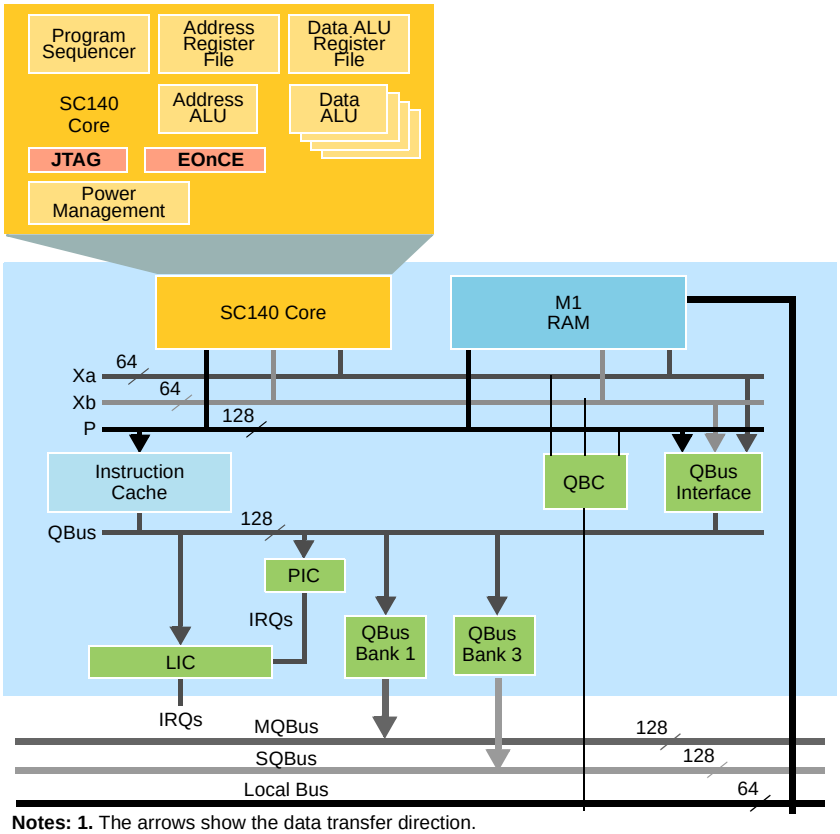


Figure 2. MSC8112 Block Diagram



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 3. StarCore SC140 DSP Extended Core Block Diagram

2.2 Critical Performance Metrics

- Offered with a core frequency of 300 MHz and supports:
  - 16 × 16-bit multiply accumulate instructions. The two extended cores can deliver a total 2400 DSP MMACS performance at 300 MHz.
  - The 8 ALUs deliver a performance equivalent to a single core running at 600 MHz. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update.
- Power supplies:
  - Core and PLL power: 1.1 V nominal
  - I/O power: 3.3 V nominal
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 0.8 mm pitch, 20 mm × 20 mm

2.3 Device Level Features

The MSC8112 device is a highly integrated system-on-a-chip that combines two StarCore® SC140 cores, 1024-channel time division multiplexing (TDM) with hardware support for µ/A-law decoding/encoding, a UART, a 16-channel DMA controller, an Ethernet controller, 1436 Kbyte of SRAM, and a flexible system interface unit (SIU). The MSC8112 device targets high-bandwidth, highly computational DSP applications and is optimized for high-bandwidth wireless transcoding and a high-density packet telephony DSP farm, as well as high-bandwidth base station applications. The MSC8112 delivers enhanced performance while maintaining low power dissipation and greatly reducing system cost. The MSC8112 operates with a core frequency of 300 MHz.

Each SC140 core has four ALUs and performs at a rate of up to 1200 DSP million multiply and accumulate commands per second (MMACS) with an internal 300 MHz clock at 1.1 V. The MSC8112 delivers a total performance of 2400 DSP MMACS. Each SC140 core connects to a level-1 224 Kbyte internal memory (M1) for program and data storage as well as a 16 Kbyte, 16-way instruction cache and a 4-entry write buffer queue for boosting core performance. All the SC140 cores share an internal 476 Kbyte level 2 memory (M2).

The TDM interface can transfer up to 1024 channels in and out of the device. The Ethernet controller port can be used for board-level interconnect and connection between boards. A full-featured multi-master 60x-compatible system port enables the SC140 cores to access external devices and gives an external host direct access to the internal memories. A flexible memory controller supports glueless accesses to various memory devices on the system bus, including SDRAM, DRAM, SRAM, Flash memory, EPROM, and user-definable memory. An external host can also access the MSC8112 device directly through a 32/64-bit direct slave interface (DSI) port. A flexible 16-channel DMA controller transfers data to and from the core M1, the M2 memory, and the serial interfaces.

2.4 Module Level Features

- Each SC140 core provides the following:
  - Up to 2400 MMACS using an internal 300 MHz clock at 1.1 V. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update.
  - 4 ALUs per SC140 core.
  - 16 data registers, 40 bits each.
  - 27 address registers, 32 bits each.
  - Hardware support for fractional and integer data types.
  - Very rich 16-bit wide orthogonal instruction set.
  - Up to six instructions executed in a single clock cycle.
  - Variable-length execution set (VLES) that can be optimized for code density and performance.
  - JTAG port designed to comply with the **IEEE** 1149.1™ standard.
  - Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.
- Each SC140 core is embedded within an extended core that provides the following:
  - 224 Kbyte M1 memory that is accessed by the SC140 core with zero wait states.
  - Support for atomic accesses to the M1 memory.
  - 16 Kbyte instruction cache, 16 ways.
  - A four-entry write buffer that frees the SC140 core from waiting for a write access to finish.
  - External cache support by asserting the Power PC global signal when accessing predefined memory banks.
  - Program Interrupt Controller (PIC).
  - Local Interrupt Controller (LIC).
- Multi-core shared memories:
  - M2 memory (shared memory):
  - A 476 Kbyte memory working at the core frequency.
  - Accessible from the local bus
  - Accessible from all four SC140 cores using the MQBus.
  - 4 Kbyte bootstrap ROM.

- An M2 memory accessible multi-core bus (MQBus):
  - A QBus protocol multi-master bus connecting the four SC140 cores to the M2 memory.
  - Data bus access of up to 128-bit read and up to 64-bit write.
  - Operation at the SC140 core frequency.
  - A central efficient round-robin arbiter controlling SC140 core access on the MQBus.
  - Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.
- Dual bus architecture that can be configured to a 32-bit data system bus and a 64-bit data direct slave interface (DSI) or to a 64-bit data system bus and 32-bit data DSI or to a 32-bit DSI and 32-bit system bus with remaining pins used for the Ethernet.
- 60x-compatible system bus
  - 64/32-bit data and 32-bit address 60x bus.
  - Support for multiple-master designs.
  - Four-beat burst transfers (eight-beat in 32-bit wide mode).
  - Port size of 64, 32, 16, and 8 controlled by the on-device memory controller.
  - Bus can access off-device memory expansion or off-device peripherals, or it can enable an external host device to access internal resources.
  - Slave support, direct access by an external host to on-device resources including the M1 and M2 memories.
  - On-device arbitration between up to 4 master devices.
- Direct Slave Interface (DSI) that provides a 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor.
  - 21–25 bit address, 32/64-bit data.
  - Direct access by an external host to on-device resources, including the M1 and the M2 memories as well as external devices on the system bus.
  - Synchronous and asynchronous accesses, with burst capability in the synchronous mode.
  - Dual or Single strobe modes.
  - Write and Read buffers improves host bandwidth.
  - Byte enable signals enables 1, 2, 4, and 8 byte write access granularity.
  - Sliding window mode enables access with reduced number of address pins.
  - Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs.
  - Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs.
  - Big-endian, little-endian, and munged little-endian support.

- Flexible eight-bank memory controller:
  - Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine
  - Glueless interface to SRAM, 100 MHz page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals.
  - Byte enables for either 64-bit or 32-bit bus width mode.
  - Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and on-device memories. Each bank has the following features:
  - 32-bit address decoding with programmable mask.
  - Variable block sizes (32 Kbyte to 4 Gbyte).
  - Selectable memory controller machine.
  - Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses.
    - Write-protection capability.
    - Control signal generation machine selection on a per-bank basis.
    - Support for internal or external masters on the 60x-compatible system bus.
    - Data buffer controls activated on a per-bank basis.
    - Atomic operation.
    - RMW data parity check (on 60x-compatible system bus only).
    - Extensive external memory-controller/bus-slave support.
    - Parity byte select pin, which enables a fast, glue less connection to RMW-parity devices (on 60x-compatible system bus only).
    - Data pipeline to reduce data set-up time for synchronous devices

- The multi-channel DMA controller has the following features:
  - 16 time-multiplexed unidirectional channels with infrastructure of 32 channels.
  - Services up to four external peripherals.
  - Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals.
  - Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates:
    - a watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination
    - a hungry request to indicate that the FIFO can accept more data.
  - Priority-based time-multiplexing between channels using 16 internal priority levels
  - A flexible channel configuration:
    - All channels support all features.
    - All channels connect to the 60x-compatible system bus or local bus.
  - Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.

- Up to four independent TDM modules, each with the following features:
  - Either totally independent receive and transmit, each having one data line, one clock line, and one frame sync line or four data lines, one clock and one frame sync that are shared between the transmit and receive.
  - Glueless interface to E1/T1 framers and MVIP, SCAS, and H.110 buses.
  - Hardware A-law/μ-law conversion
  - Up to 50 Mbps per TDM (50 MHz bit clock if one data line is used, 25 MHz if two data lines are used, 12.5 MHz if four data lines are used).
  - Up to 256 channels.
  - Up to 16 Mbyte per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte)
  - Receive buffers share one global write offset pointer that is written to the same offset relative to their start address.
  - Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address.
  - All channels share the same word size.
  - Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering.
  - Each channel can be programmed to be active or inactive.
  - 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively.
  - The TDM Transmitter Sync Signal (TxTSYN) can be configured as either input or output.
  - Frame Sync and Data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock.
  - Frame sync can be programmed as active low or active high.
  - Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame.
  - MSB or LSB first support.

- Ethernet controller:
  - Designed to comply fully with the **IEEE®** 802.3® standard.
  - Provides integrated 10/100 Mbps Ethernet MAC port
  - Media Independent Interface (MII)
  - Reduced Media Independent Interface (RMII)
  - Supports half- and full-duplex operations in 10/100 Mbps mode
  - Supports full-duplex flow control feature (802.3x)
  - VLAN tagged frame support (802.3ac)
  - Multicast and broadcast frame detection
  - Pattern matching which support accept/reject of IPv4 and IPv6 addresses
  - Internal DMA engine and transmit and receive FIFOs
  - Four receive and one transmit buffer descriptor rings
  - RMON statistics support
  - Big-and little-endian support.
  - UART
  - Two signals for transmit data and receive data.
  - No clock, asynchronous mode.
  - Serviced either by the SC140 DSP cores or an external host on the system bus or the DSI.
  - Full-duplex operation.
  - Standard mark/space non-return-to-zero (NRZ) format.
  - 13-bit baud rate selection.
  - Programmable 8-bit or 9-bit data format.
  - Separately enabled transmitter and receiver.
  - Programmable transmitter output polarity.
  - Two receiver walk-up methods:
    - Idle line walk-up.
    - Address mark walk-up.
  - Separate receiver and transmitter interrupt requests.
  - Eight flags, the first five can generate interrupt request:
    - Transmitter empty.
    - Transmission complete.
    - Receiver full.
    - Idle receiver input.
    - Receiver overrun.
    - Noise error.
    - Framing error.
  - Parity error.
    - Receiver framing error detection.
    - Hardware parity checking.

  - 1/16 bit-time noise detection.
  - Maximum bit rate 6.25 Mbps.
  - Single-wire and loop operations.
- I^2C Software Module
  - 2-wire serial interface through GPIO
  - Schmitt Trigger, filtered inputs for noise suppression
  - Compatibility with I^2C bus standard (up to 100 kbps Standard mode and 400 kbps Fast-mode)
  - Bidirectional data transfer protocol
  - Scalable clock rate of up to 1 MHz, starting at 50 kbps for the maximum core clock frequency
  - Multiple-master operation that allows any number of devices implementing the I^2C master software module to access the memory simultaneously.
  - Compatible with the widespread I^2C serial EEPROM access protocol, allowing memory accesses of up to 1Mbyte.
  - Defacto industry standard memory access of up to 1 Mbyte
- General-Purpose I/O (GPIO) port:
  - 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports.
  - Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.
- Timers:
  - Two modules of 16 timers each.
  - Each module can generate two DMA requests when counting reaches a programmed threshold.
  - Each timer has the following features:
    - Cyclic or one-shot.
    - Input clock polarity control.
    - Interrupt request when counting reaches a programmed threshold.
    - Pulse or level interrupts.
    - Dynamically updated programmed threshold.
    - Read counter any time.
    - Watchdog mode for the timers that connect to the device.

- Hardware semaphores. Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.
- Global Interrupt Controller (GIC):
  - Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and to the cores.
  - Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access.
  - Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access.
- Power and Packaging
  - Reduced power dissipation:
    - Low power CMOS design.
    - Separate power supply for internal logic (1.1 V) and I/O (3.3 V).
    - Low-power standby modes.
    - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
  - Packaging:
    - 0.8 mm pitch High Temperature Coefficient for Expansion Flip-Chip Plastic Ball-Grid Array (FC-PBGA).
    - 431-connection (ball).
    - 20 mm × 20 mm.

3 Developer Environment

Freescale supplies a complete set of DSP development tools for the MSC8112 device. Our tools are focused on providing easier and more robust ways for designers to develop optimized DSP systems. Whether the application targets IP telephony or media gateways, the development environment gives the designers everything they need to exploit the advanced capabilities of the MSC8112 architecture.

3.1 Tools

The MSC8112 tool components include the following:

- *Integrated development environment (IDE).* Easy-to-use graphical user interface and project manager for configuring and managing multiple build configurations.
- *C compiler with in-line assembly.* The developer can generate highly optimized DSP code by exploiting the StarCore multiple-ALU architecture, with parallel fetch sets and high code density.
- *Librarian*. The developer can create application-specific DSP libraries for modularity.
- *Linker.* The developer can efficiently produce executables from object code and partition memory according to the application architecture; the linker supports code overlay.
- *Debugger.* Seamlessly integrated real-time, non-intrusive, multi-mode and multi-DSP debugger handles highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. Supports RTOS-aware debugger.
- *Royalty-free RTOS*. Included with package.
- *Software Simulator.* Full chip simulation; the developer can design an application and run it on the simulator before running it on the silicon. FCS integrated under IDE, the simulator provides customers with tools to create projects and debug them as they would on silicon.
- *Profiler.* The developer can analyze and identify program design inefficiencies.
- *Data Visualization*. Lets the developer graph variables, registers, regions of memory, and HSST data streams as they change over time. By changing the visualization filter, you can plot this data in a variety of ways; including line charts, logarithmic charts, polar coordinates, and scatter graphs.
- *High Speed Run Control*. PowerTAP high speed host-target interface allows users to program in Flash memory, ROM, and cache.
- *Host Platform Support*. Microsoft Windows and Solaris.
- *Development Board*. The application development system (ADS).
- *Kit for MSC8112*. A complete system for developing and debugging real-time hardware and software. The kit includes the MSC8112 device with a companion memory, JTAG debug interface, Ethernet interface, PCI interface, digital video interfaces and software device drivers.

3.2 Application Software

Freescale offers a broad range of DSP applications through its third-party application software partners; these applications target IP telephony, telephony modem, wireless and multimedia transcoding, and wireless base stations. Applications and software modules are listed in **Table 1**.

Table 1. Application Software Modules

Application	Modules
ETSI/3GPP1 Vocoders	GSM-FR, GSM-HR, GSM-AMR/EFR, 3GPP AMR-WB
TIA/3GPP2 Vocoders	IS127 EVRC, IS893 SMW
ITU G.7xx Vocoders	G.711, G.711 App. 1 and 2 (PLC and VAD/CNG), G.722, G.723.1, G.726, G.726A, G.728, G.729B, G.729AB, G.729E
Modems	Pumps: V.23 CallerID, V.34, V.90, V.92
	V.42 MNP4 (error correction)
	Compression: V.44, V.42bis, MNP5
	Negotiation: V.8, V.8bis
	HDLC
	Relay: V.150.1 (MoIP)
Fax	Pumps: V.17, V.27ter, V.29
	Relay: T.30 (FoIP), T.38
Echo cancellation	G.165, G.168 (64 ms), G.168 2004 (128 ms, windowed), noise reduction, acoustic level control, Acoustic EC (roadmap)
Telephony support	DTMF detection, universal tone generation, special tone event detect, VAD/CNG, PLC, RTP packetization
Device Driver	DMA driver, SRIO driver, TDM driver, Ethernet driver, PCI driver, UTOPIA driver, UART driver, memory allocation, interrupt handling

In addition, Freescale provides a complete VoIP framework for channel scheduling, explicit DMA management of channel state data, memory management, network termination, peripheral drivers, framework control API command/status, and more.

4 Document Revision History

Table 2 provides a revision history for this product brief.

Table 2. Document Revision History

Rev. No.	Substantive Change(s)
0, Draft A	This is the first release of this document.

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