Advance Information

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MC92460 HDLC Controller Technical Summary

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The MC92460 is a 40-channel, high-level data link controller (HDLC) with an aggregate throughput of up to 2.0 Gbps across a synchronous optical network (SONET). A total of eight of these peripheral devices can be connected to the 60x bus of the MPC8260 or the MPC603e.

Applications for the MPC92460 include remote access concentrators, frame relay switches, high-speed direct links, regional office routers, DSLAM (xDSL) and internet access equipment, and uses in the cellular infrastructure.

1.1 Overview

Figure 1-1 shows a block diagram of the MC92460.

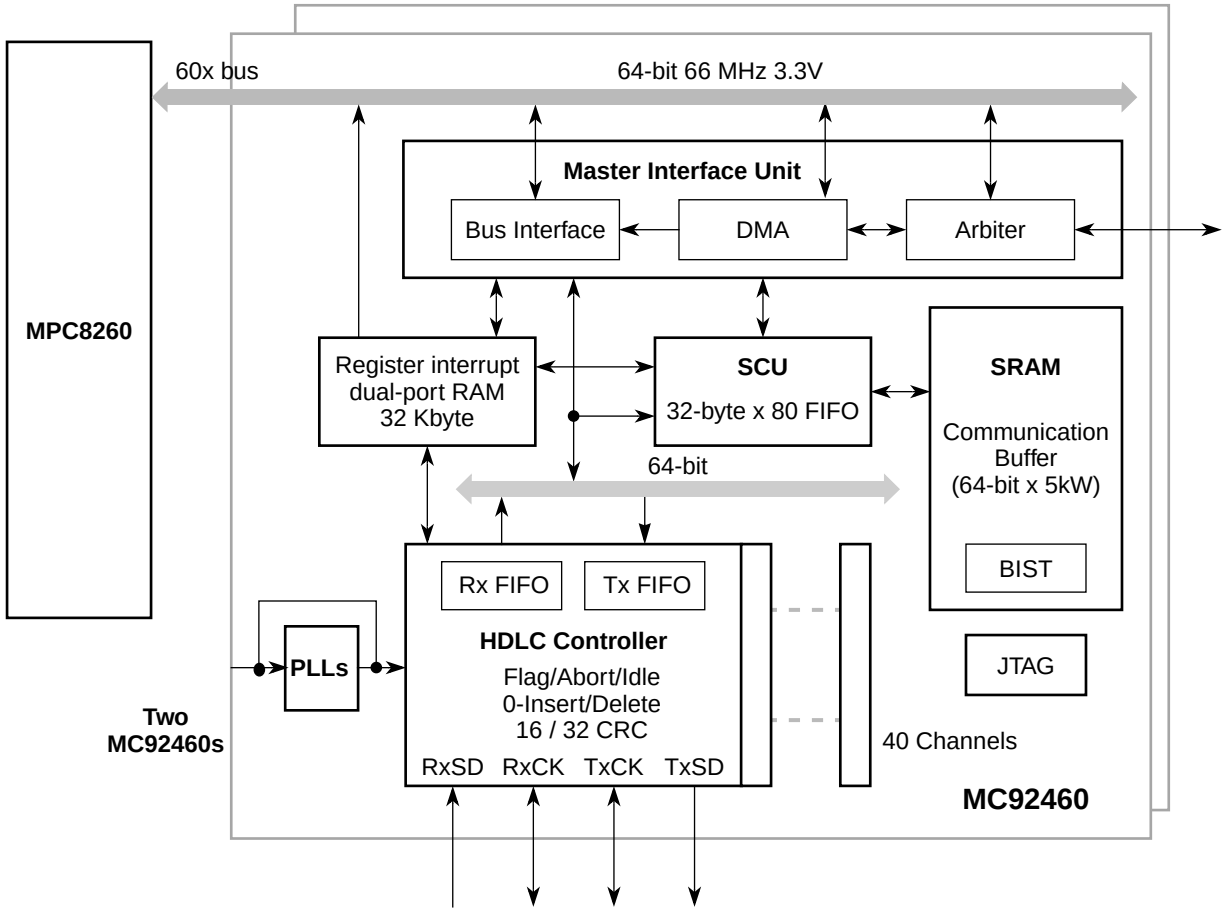

Figure 1-1. MC92460 Block Diagram

1.2 MC92460 Key Features

Major features of the MC92460 include the following:

- Controllers
  - — Maximum throughput of up to 2 Gbps; individual controllers operating up to 66.7 Mbps
  - — All communication controllers operating in asynchronous mode
- HDLC Channels
  - — 40 dedicated full-duplex HDLC channels
  - — Each HDLC channel supporting a maximum of 66.7 Mbps
  - — A default of 64 buffer descriptors per channel (32 TxBD + 32 RxBD) or 4096 total buffer descriptors
  - — Configurable number of buffer descriptors in each channel (minimum of 0, maximum of 4096)

- Buffering
  - 32-Kbyte on-chip dual port RAM for buffer descriptors
  - A default of 64 buffer descriptors per channel (32 TxBD + 32 RxBD) or 4096 total buffer descriptors
  - 256 Kbits on-chip memory for data buffers
  - 256-Kbit communication buffer storing up to 819 bytes per frame
  - Maximum buffer length of 64 Kbytes
  - 80 channel virtual DMA functionality executing between off-chip memory and the communications buffer
- Framing
  - Programmable frame size (maximum 64 Kbytes)
  - Flexible buffers and multiple buffers per frame
  - Separate interrupts for frames and buffers (Tx and Rx)
  - Received frames threshold to reduce interrupt overhead
  - Flag/abort/idle generation and detection
  - Zero insertion and deletion
  - 16- or 32-bit CRC-CCITT generation and checking
  - Detection of non-connected aligned frames
  - Detection of too-long frames
  - Programmable flags (0-15) between successive frames
  - Automatic retransmission in case of collision
  - Echo and local loopback mode for testing
- Master interface unit
  - Directly connects with 64-bit data, 32-bit address 60x bus
  - Supports 66.7 MHz 60x bus speed
  - Virtual DMA supports an 80-channel HDLC master
  - Virtual DMA functionality executing off-chip memory to internal memory
  - Either the master or the slave MC92460 can be the 60x bus master
  - Bus supports multi-master design
  - Up to eight devices may be connected in parallel on the 60x bus
  - Supports single beat and burst accesses
- Baud rate generator (BRG)
  - 40 independent and identical baud rate generators, one per channel
  - On-chip PLL for configurable baud rate generation (maximum of 66.7 MHz)
  - A 16x divider option allows slow baud rates at high system frequencies
  - Each BGR output can be routed to a pin (TxCK*n* and RxCK*n*)
  - On-the-fly changes allowed

- 480-pin TBGA, 1.27mm pitch packaging
- Supports IEEE1149.1 JTAG controller standard
- Separate power supplies for core (1.8V) and internal logic (3.3V)

1.3 Applications

Typical applications for the MC92460 include the following:

- Dedicated rather than switched HDLC channels
- IP service providers
- Network management in a SONET/SDH add-drop multiplexer for OC3, OC12, OC48, OC192, and WDM
- Telecom switching equipment
- Regional office routers
- DSLAM (xDSL) and internet access equipment
- Cellular infrastructure equipment

1.4 MC92460 Functionality

The MC92460 HDLC controller is designed to handle the data link layer [layer 2] of the OSI model. This 40-channel Tx and 40-channel Rx device consists of separate transmit and receive sections whose operations are asynchronous with respect to other HDLCs.

The following sections briefly describe components of the MC92460.

1.4.1 SCU (System Control Unit)

The system control unit is responsible for system configuration and protection (through parameter RAM) and arbitration of the internal memory (SRAM) access between the HDLCs and the external system bus. It stores HDLC channel data in buffers by referencing 4096 buffer descriptors (BD) that reside in dual-port RAM.

Data can be written to internal memory either through a DMA write or through MPC8260 arbitration. The SCU programs the HDLC channels through the max HDLC channel register (MMCR) and sets each receive and transmit channel’s base address through the RBASE and TBASE registers.

1.4.1.1 Parameter RAM

The SCU maintains a section of RAM called the parameter RAM, which contains many parameters for the operation of the HDLC channels. Each channel has 128 bytes of parameter RAM space. Features such as maximum receive buffer length, CRC preset and mask, protocol conditions, and others are stored in the parameter RAM.

1.4.1.2 Buffer Descriptors (BDs)

The SCU stores the data associated with each HDLC channel in buffers (such as SRAM), and each buffer is referenced by an 8-byte buffer descriptor (BD) that can reside anywhere in dual-port RAM. There are 4096 BDs: 2048 RxBDs and 2048 TxBDs. The total number of BDs is limited only by the size of the 32 Kbyte dual-port RAM.

1.4.1.3 Communications Buffer (SRAM)

This is a 64-bit x 4K-word SRAM that can be used to hold the transmit and receive buffer data pointed to by TxBD and RxBD. The bus master (MPC8260, MPC603e, and DMA devices) can be accessed as memory.

1.4.2 HDLC Controller

The 40 HDLC controllers of the MC92460 consist of separate transmitter and receiver components that are asynchronous with respect to each other and require little or no core intervention once enabled. Each controller can support a maximum of 66.7 Mbps.

The transmitter starts sending flags or idles as programmed in the HDLC mode register. The HDLC polls the first BD (buffer descriptor) in the TxBD table. When there is a frame to transmit, the HDLC fetches the data from memory and starts sending the frame after sending the minimum number of flags specified between frames.

The receiver performs address recognition, CRC checking, and maximum frame length checking. Received frames can be used to implement any HDLC-based protocol. The receiver waits for an opening flag character. When it detects the first byte of the frame, the HDLC compares the frame address with four user-programmable, 16-bit address registers and an address mask. If an address match is detected by the HDLC, the receiver fetches the next buffer descriptor and starts transferring the incoming frame to the buffer.

Each controller has its own baud rate generator to provide HDLC channel clocks.

1.4.3 Master Interface Unit (MIU)

The master interface unit supports the 60x bus. This module is connected through the 60x compatible bus mode of the processor.

The system bus arbiter of the MIU is responsible for allocating both the internal master bus and the 60x external bus whenever the MPU core (which implements the Power PC architecture, MPC603e, or MPC8260) relinquishes bus control. This arbiter manages the internal master bus and the 60x external bus for the DMA module.

1.4.4 Test Access Port (TAP)

The MC92460 provides a dedicated user accessible test access port (TAP) that is fully compatible with the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture. The TAP consists of five dedicated signals: a 16-state TAP controller and four test data registers. A boundary scan register links all device signals into a signal shift register. The test logic, which is implemented using static logic design, is independent of the device system logic.

1.4.5 Phase-Locked Loop (PLL)

The MC92460 has two phase-locked loop (PLL) blocks. The phase-locked loop 1 (PLL1) block generates all clocks for the device, including a high-frequency master clock as a system and bus clock with the SYSCLK reference.

The phase-locked loop 2 (PLL2) block generates a high-frequency master clock as a serial clock with the EXCLK reference.

1.4.6 Reset

There are multiple inputs to the reset logic. The reset block has reset control logic that determines the cause of reset, synchronizes it if necessary, and resets the appropriate logic modules. The system control unit, HDLC controller, master interface unit, register, and I/O signals are initialized only on hard reset.

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