EL2M

Product Description for EL2Monitor

Rev. 2.0 — 11 March 2026 **Product brief**

1 Software product overview

This section contains a product description as follows:

EL2-Monitor is a partitioning hypervisor which enables further partitioning of the Real Time Unit (RTU) cores into “R52 partitions”.

Without EL2-Monitor or a similar product each two R52 cores belonging to the RTU can’t be 100% isolated from each other due to the shared GIC distributor.

The EL2-Monitor uses the EL2 MPU to protect the shared HW GIC and offers an exclusive virtual GIC distributor to each core.

The EL2-Monitor does not offer virtual CPUs thus the allocation is always 1:1 (VMs: physical Cores)

The EL2 Monitor shall be the only component running at EL2.

The following diagrams illustrates some use cases addressed by EL2Monitor.

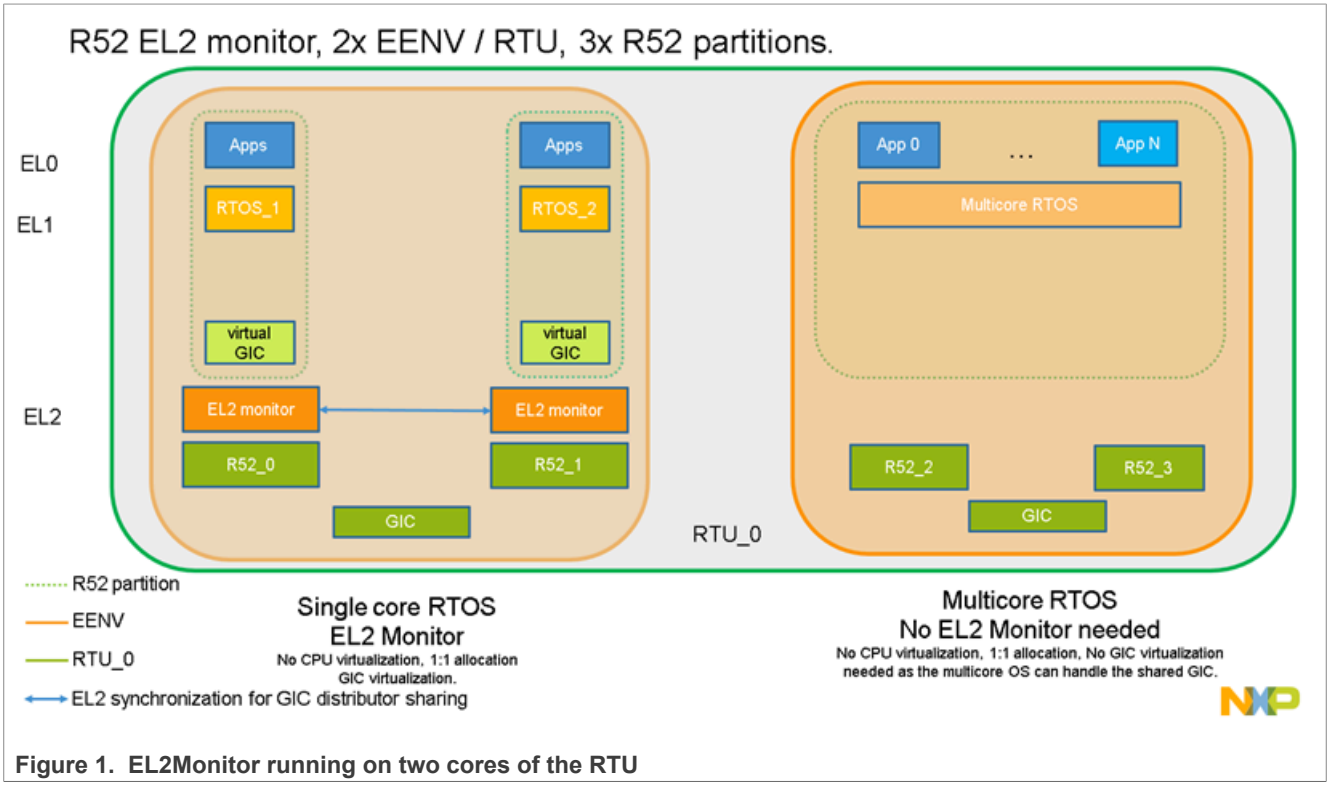

Figure 1. EL2Monitor running on two cores of the RTU

In Figure 1 EL2 Monitor is running on two of the RTU cores that share the GIC.

Both cores belong to the same EENV and each RTOS is seeing an exclusive virtual GIC.

The other two cores belong to a different EENV and a multicore OS is aware of the shared GIC and handles it internally.

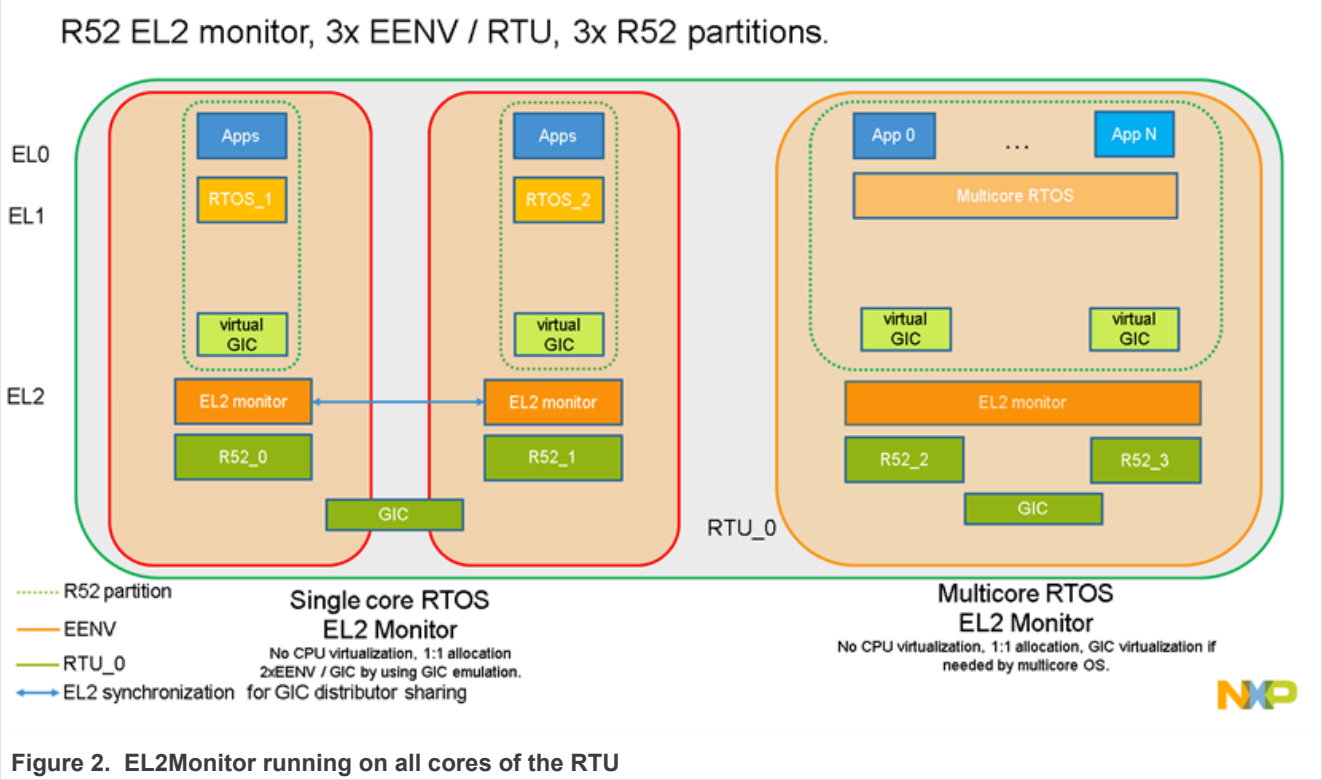

Figure 2. EL2Monitor running on all cores of the RTU

In Figure 2 the EL2 Monitor is running on all the cores.

The left two cores belong to different EENVs and EL2 Monitor facilitates the partitioning by providing each core a virtual GIC. Additionally, the EL2 MPU is further used to facilitate the creation of the R52 partitions.

The right two cores belong to the same EENV and are running a multicore RTOS that can't handle the shared GIC. In this case the EL2 Monitor provides a virtual GIC to each core.

2 Software content

This section contains the list of major supported features or reference to applicable standards (e.g., Autosar).

EL2Monitor software package contains:

- EL2Monitor partitioning hypervisor source code
- EL2Monitor configuration plugin for Tresos
- EL2Monitor configuration plugin for S32CT
- Basic sample application

EL2Monitor software package also contains:

- Release Notes:
  - Supported platforms
  - Validated compilers
  - Instructions to configure, compile, build and run the sample application on top of EL2Monitor
  - Known limitation

  - Licensing and support
- User Manual:
  - This document contains the integration manual of the EL2 Monitor components which support partitioning and isolation of applications on the ARM R52 processor by providing GIC virtualization/paravirtualization and EL2 MPU protection.
  - The document is intended to describe the steps the user must take to:
    - Run the delivered EL1 sample application together with the EL2 Monitor
    - Integrate the EL2 Monitor into an existing project

- SBOM
  - This document contains the EL2M product license information for each release

- Quality Package - delivered to customers for PRC and RFP releases
- Safety Package – delivered to customers for PRC and RFP releases

2.1 Architecture

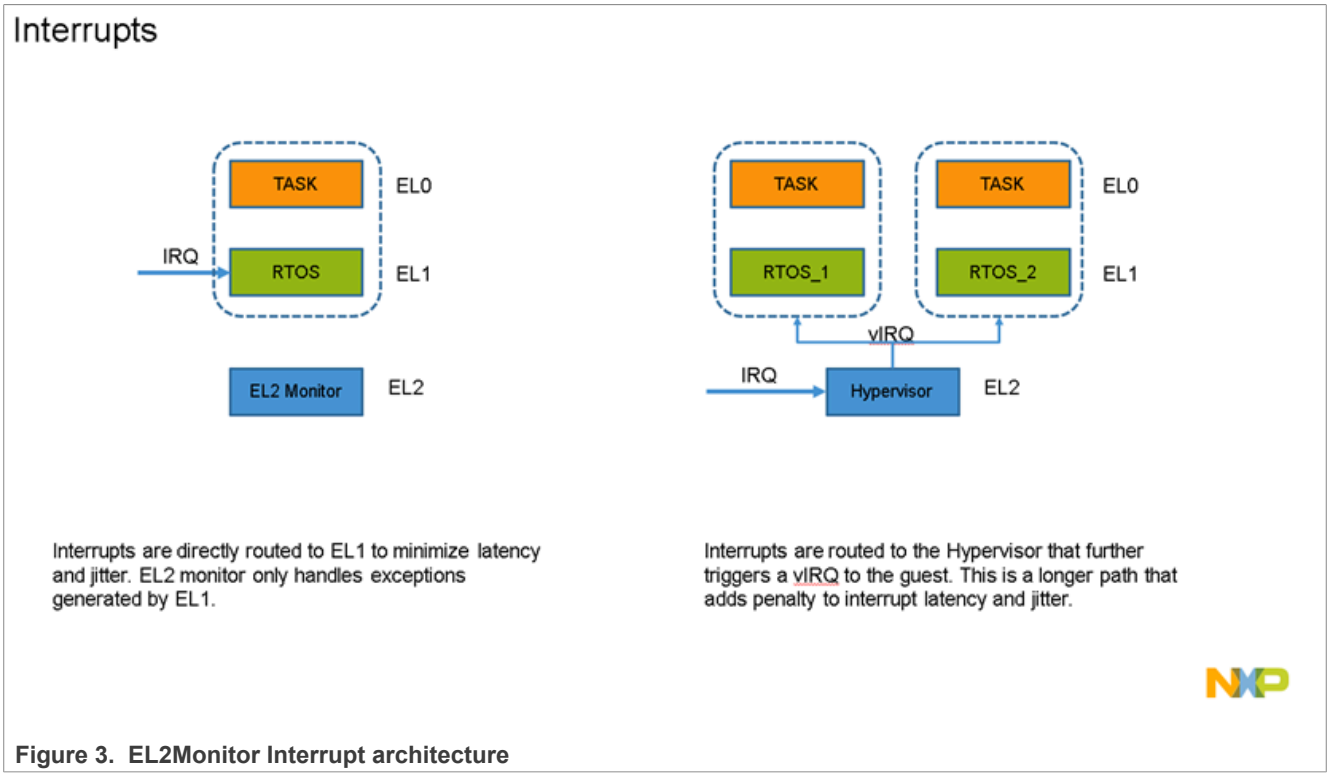

Figure 3. EL2Monitor Interrupt architecture

Figure 3 shows the EL2Monitor approach to interrupts to minimize interrupt latency and jitter.

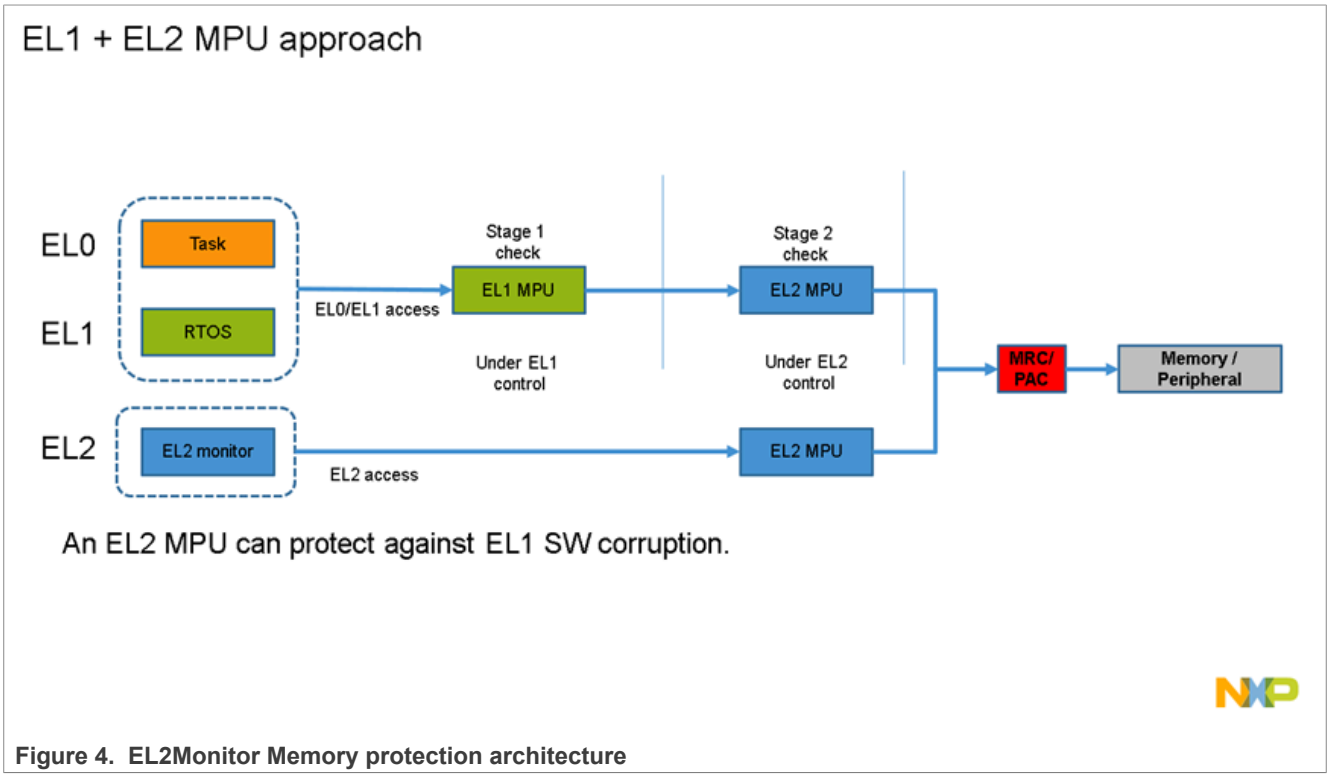

Figure 4. EL2Monitor Memory protection architecture

Figure 4 shows the EL2 Monitor Memory protection architecture.

In order to implement the virtual GIC and further create the R52 partition the EL2 MPU is used.

3 Supported Targets

The software described in this document is intended to be used with NXP Semiconductors S32N, S32K5, S32J100, S32ZE devices.

4 Quality Standards Compliance, Safety Standard Compliance, Security Standard Compliance and Testing Approach

The software described in this document is developed according to NXP Software Development Process, that is Automotive-SPICE: 3.1, IATF 16949:2016, ISO 26262: 2018, ISO 21434:2021 and ISO 9001:2015 compliant.

The EL2Monitor product is developed according to NXP Software Development Processes that are Automotive-SPICE, ISO26262, IATF16949 and ISO9001 compliant.

The Quality package includes:

- SW Traceability Matrix (full: Req-design-code-tests)
- SW Traceability Warning Report
- SW Test Specification (at all test levels)
- SW Test Report
- System Test Results
- SW Static Analysis Report (MISRA, Code Metrics, CERT-C, CWE and others)
- SW Code Coverage Report
- Profiling Report/ Benchmark Report
- Code and Stack Size Report
- Memory Report/ RAM Size Report
- Compiler Warning Report
- Quality Matrix

The Safety package includes:

- Safety manual
- FMEA

The Software package includes:

- Source code/ binaries
- SW Customer Documentation - Release Notes
- SW Customer Documentation - User Manual
- Software Bill of Materials (SBOM)

As the GIC Distributor peripheral is shared among each two/four cores of the ARM R52 processor (depending on the core configuration in an RTU), the main scope of the EL2 Monitor is to emulate the GIC peripheral for cores that share the GIC. EL2 Monitor also provides the functionality of setting up user defined EL2 MPU regions to isolate the running applications.

Testing framework consists of 8 test suites to test all aspects of EL2 Monitor: Configuration, GIC Registers access, Memory Protection Unit (MPU), Semaphore implementation, Latency and Memory footprint demonstration.

The compilers used for validation are mentioned in the release notes document.

5 Revision history

Document ID	Release date	Description
EL2M_PB v.2.0	11 March 2026	Migrated to new template
EL2M_PB v.1.0	06 June 2025	First version

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