MOTOROLA
Semiconductor Product Information

DSP56654P/D
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DSP56654 Integrated Cellular Baseband Processor Product Brief

Motorola designed the DSP56654 to support the rigorous demands of the cellular subscriber market. Optimized for narrow-band wireless systems such as GSM and TDMA/AMPS, the high level of on-chip integration in the DSP56654 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low power consumption and cost-effective system performance. The DSP56654 chip combines the power of Motorola's 32-bit M•CORE™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor) core with on-chip memory, protocol timer, and custom peripherals to provide a single-chip cellular base-band processor. Figure 1 shows the DSP56654 basic block diagram.

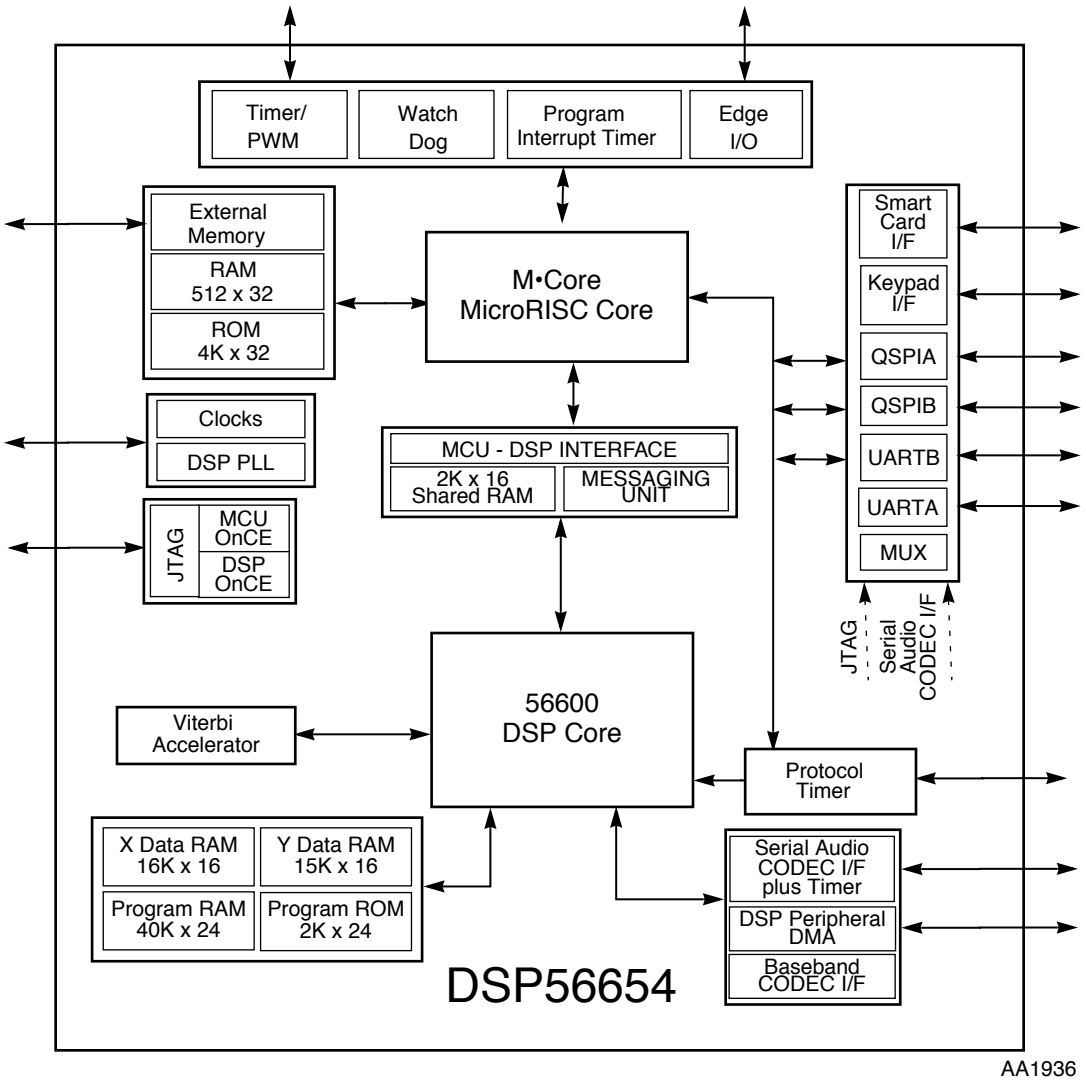

Figure 1. DSP56654 System Block Diagram

Features

- RISC M•CORE MCU
  - 32-bit load/store RISC architecture
  - Fixed 16-bit instruction length
  - 16-entry 32-bit general-purpose register file
  - 32-bit internal address and data buses
  - Efficient four-stage, fully interlocked execution pipeline
  - Special branch, byte, and bit manipulation instructions
  - Support for byte, half-word, and word memory accesses
  - Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file
- High-performance DSP56600 core
  - 1 × engine (e.g., 70 MHz = 70 MIPS)
  - Fully pipelined 16 × 16-bit parallel multiplier-accumulator (MAC)
  - Two 40-bit accumulators including extension bits
  - 40-bit parallel barrel shifter
  - Highly parallel instruction set with unique DSP addressing modes
  - Position-independent code support
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip support for software patching and enhancements
  - Realtime trace capability via external address bus
- On-chip memories
  - 4K × 32-bit MCU ROM
  - 512 × 32-bit MCU RAM
  - 40K × 24-bit DSP Program RAM
  - 2K × 24-bit DSP Program ROM
  - 31K × 16-bit DSP data RAM, split into 16K × 16-bit X data RAM and 15K x 16-bit Y data RAM spaces
  - 2K x 16 DSP/MCU interface, dual port RAM (part of the 16K x 16 X data RAM)
- On-chip peripherals
  - Fully programmable phase-locked loop (PLL) for DSP clock generation
  - External interface module (EIM) for glueless system integration
  - External 22-bit address and 16-bit data MCU buses
  - Thirty-two source MCU interrupt controller
  - Intelligent MCU/DSP interface (MDI) dual 2K x 16-bit dual port RAM (shares 2K DSP X data RAM) with messaging status and control
  - Serial audio codec port
  - Serial baseband codec port

  - Protocol timer frees the MCU from radio channel timing events
  - Two queued serial peripheral interface (QSPI) communicate with external peripherals
  - Keypad port capable of scanning up to an 8 × 8 matrix keypad
  - Software watchdog timer, DSP timer, O/S programmable interrupt timer, and MCU general-purpose timers
  - Pulse width modulation (PWM) output
  - Two universal asynchronous receiver/transmitter (UARTs) with FIFO
  - IEEE 1149.1-compliant boundary scan JTAG test access port (TAP)
  - Integrated DSP/M•CORE On-Chip Emulation (OnCE™) module
  - DSP address bus visibility and DSP data bus visibility modes for system development
  - ISO 7816-compatible SmartCard port
- Operating features
  - Comprehensive static and dynamic power management
  - M•CORE operating frequency: dc to 16.8 MHz at 1.8 V
  - DSP operating frequency: dc to 58.8 MHz at 1.8 V
  - Internal operating voltage range: 1.8–2.5 V with 3.3 V-tolerant I/O
  - Operating temperature: –40˚ to 85˚C ambient
  - 256-pin 17 x 17mm plastic ball grid array (PBGA) package

Target Applications

The DSP56654 is intended for use in cellular subscriber applications, primarily GSM and TDMA/AMPS, and other applications needing both DSP and control processing.

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