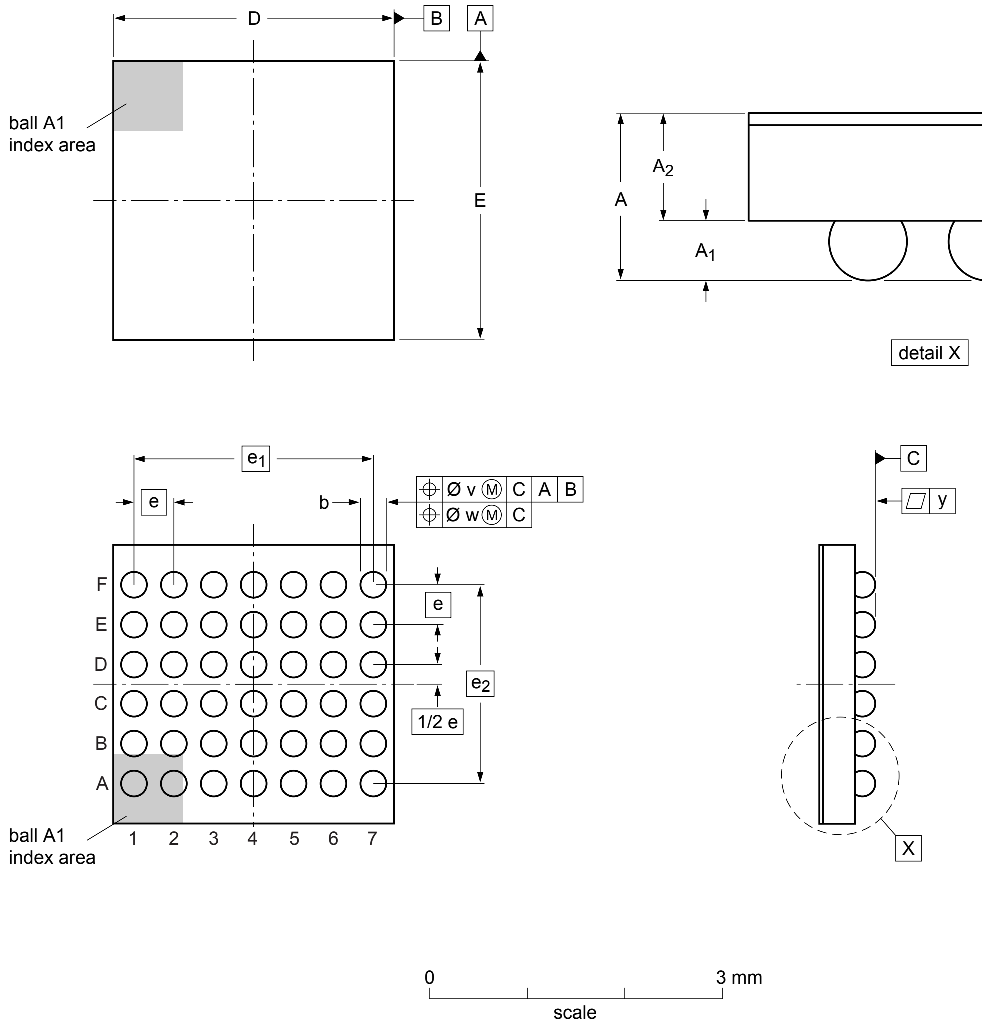
Package outline

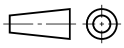
WLCSP42: wafer level chip-scale package; 42 bumps; 2.88 x 2.80 x 0.54 mm (backside coating included) **PN549**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.58	0.23	0.37	0.29	2.90	2.82						
	nom	0.54	0.20	0.34	0.26	2.88	2.80	0.4	2.4	2.0	0.15	0.05	0.05
	min	0.50	0.17	0.31	0.23	2.86	2.78						

wlcsp42_pn549_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PN549	- - -	- - -				~~14-07-01~~ 15-08-06

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