

3 September 2018

Package information

Package summary

Terminal position code Q (quad) **HVQFN56** Package type descriptive code

Package style descriptive code HVQFN (thermal enhanced very thin quad

flatpack; no leads)

Mounting method type S (surface mount)

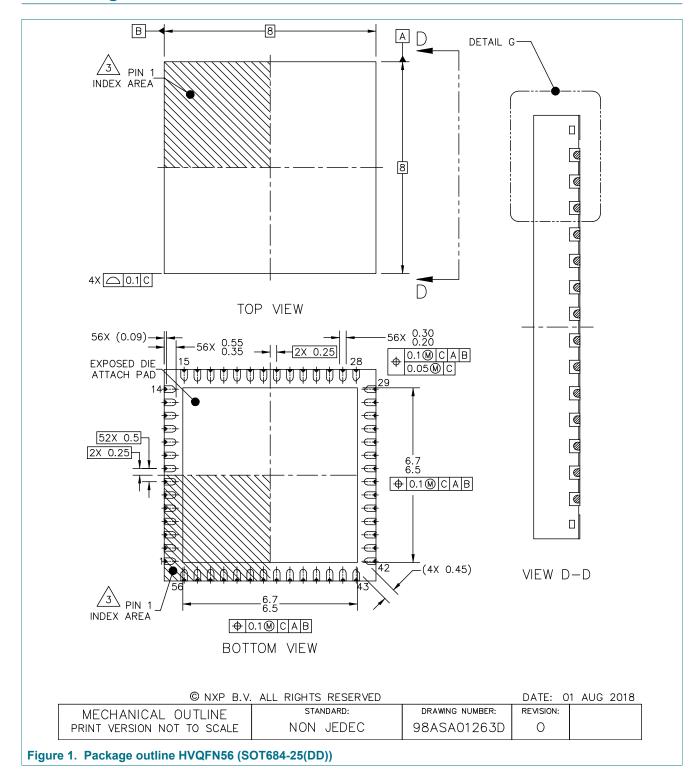
Issue date 01-08-2018 98ASA01263D Manufacturer package code

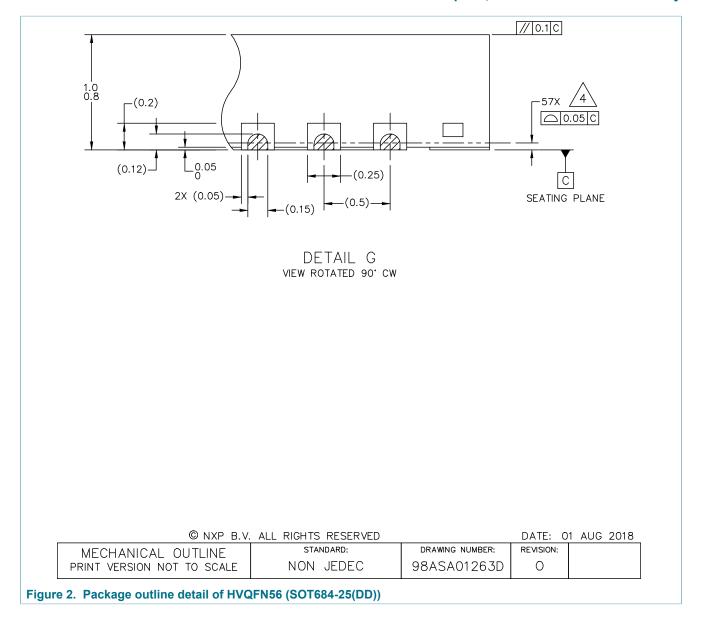
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	8	-	mm
package width	-	8	-	mm
seated height	-	0.85	-	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	56	-	



2 Package outline







- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.

5. MIN. METAL GAP SHOULD BE 0.25 MM.

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Figure 3. Package outline note HVQFN56 (SOT684-25(DD))

3 Soldering

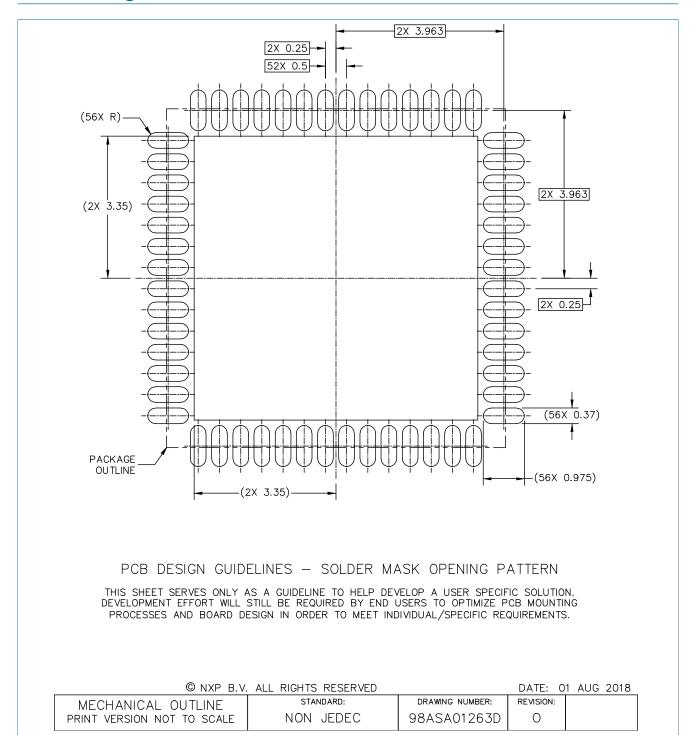
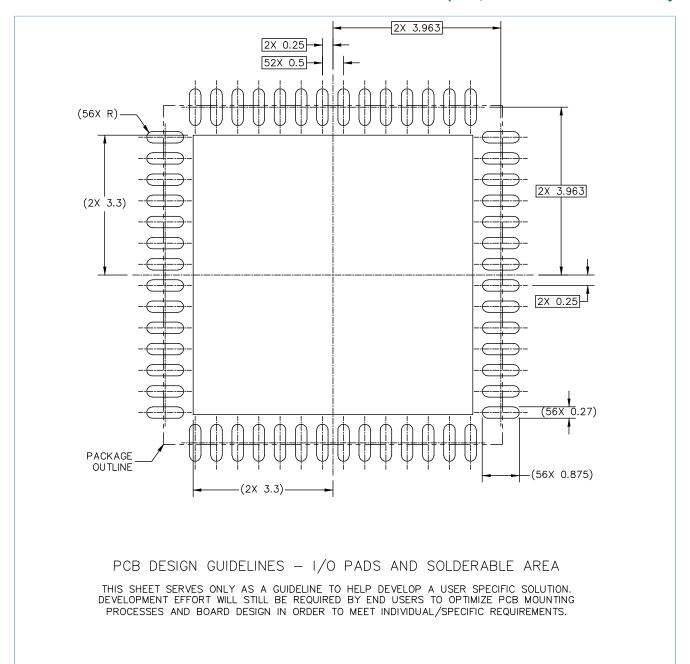


Figure 4. Reflow soldering footprint part1 for HVQFN56 (SOT684-25(DD))



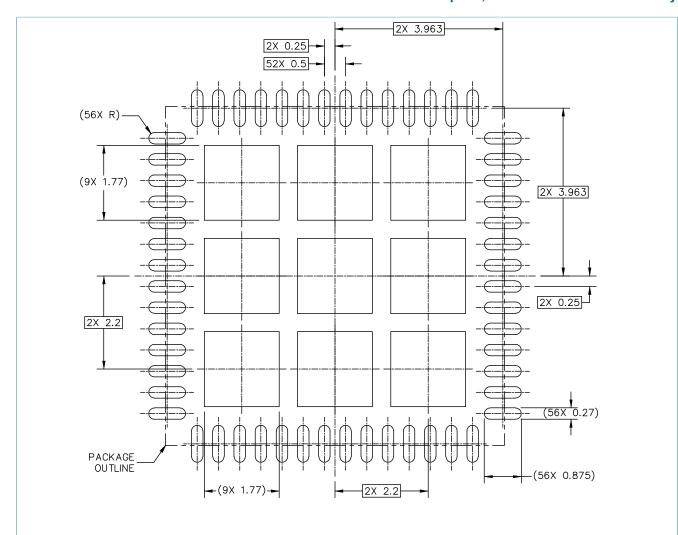
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Figure 5. Reflow soldering footprint part2 for HVQFN56 (SOT684-25(DD))

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PRI



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES - SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Figure 6. Reflow soldering footprint part3 for HVQFN56 (SOT684-25(DD))

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SOT684-25(DD)

HVQFN56, thermal enhanced very thin quad flat package; no leads; dimple wettable flank; 56 terminals; 0.5 mm pitch, 8 mm x 8 mm x 0.85 mm body

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