

SOT2069-1

WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

3 September 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP141
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	13-07-2020
Manufacturer package code	98ASA01653D

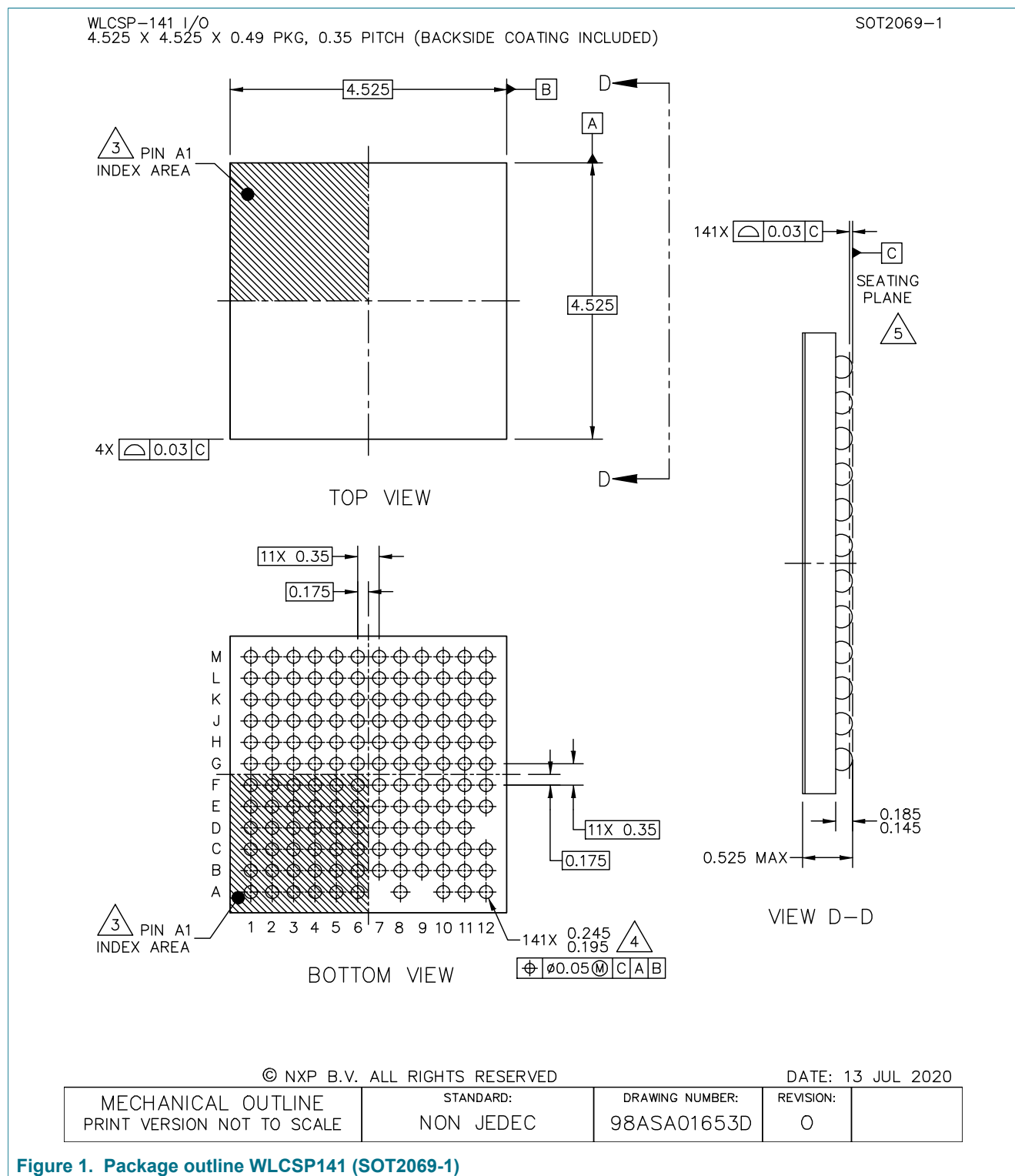
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	4.495	4.525	4.555	mm
package width	4.495	4.525	4.555	mm
package height	-	0.49	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	141	-	



WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

2 Package outline

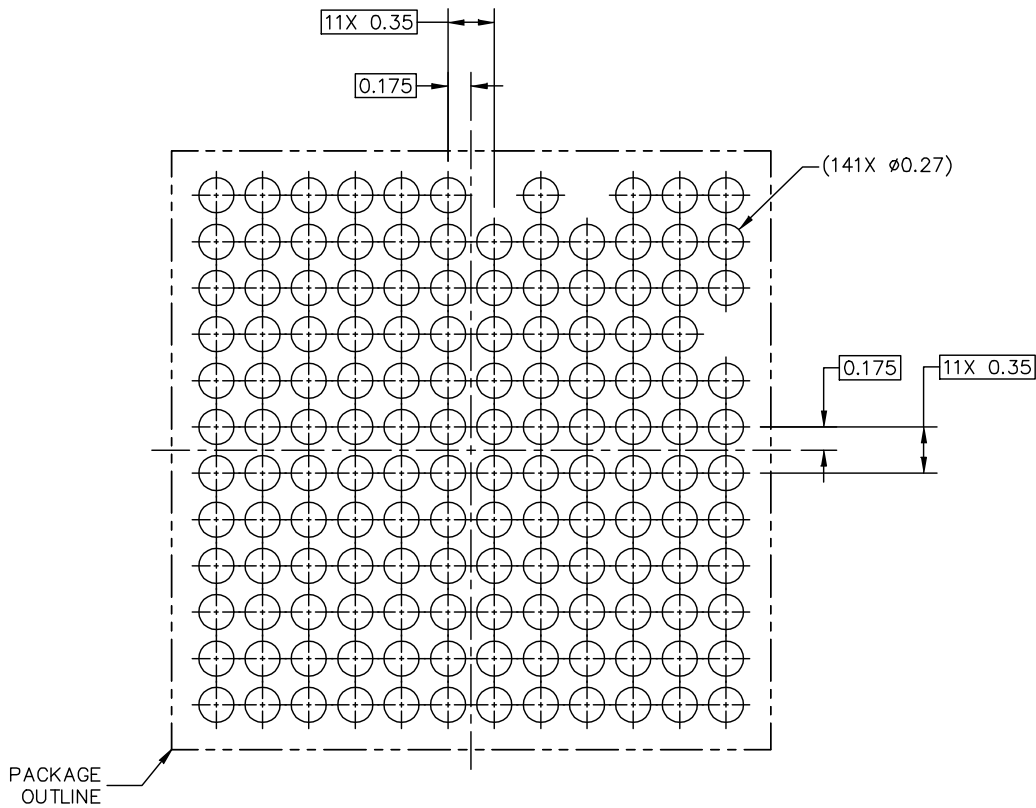


WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

3 Soldering

WLCSP-141 I/O
4.525 X 4.525 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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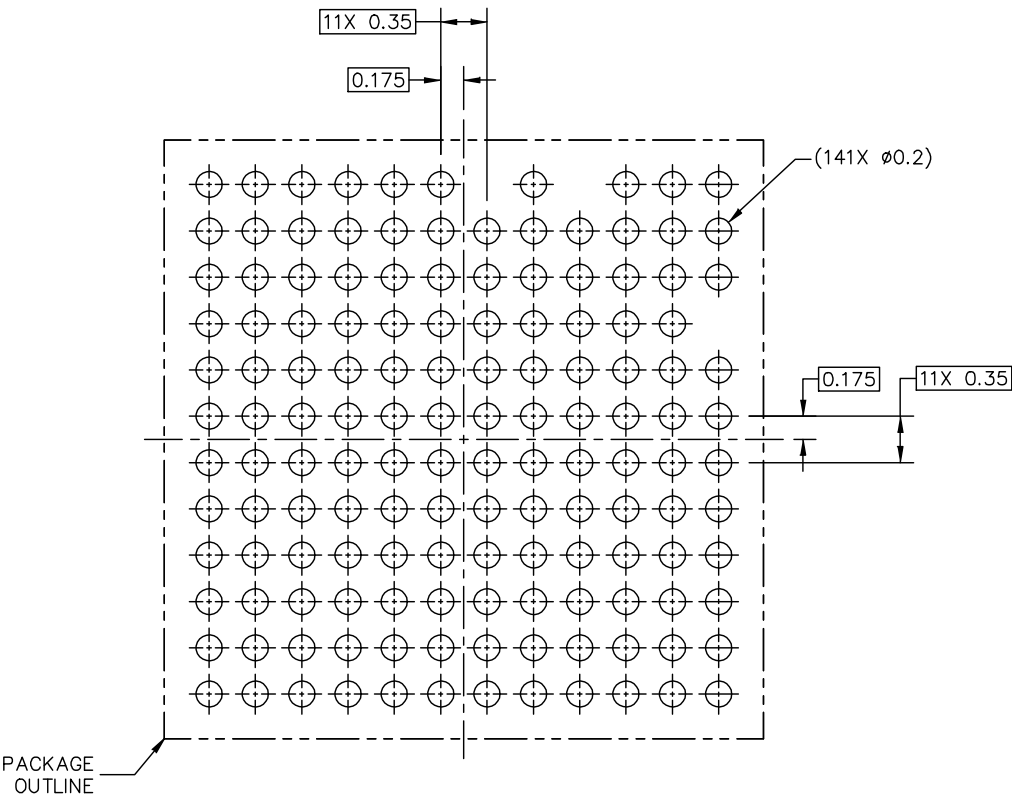
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01653D	REVISION: 0	
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Figure 2. Reflow soldering footprint part1 for WLCSP141 (SOT2069-1)

WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

WLCSP-141 I/O
4.525 X 4.525 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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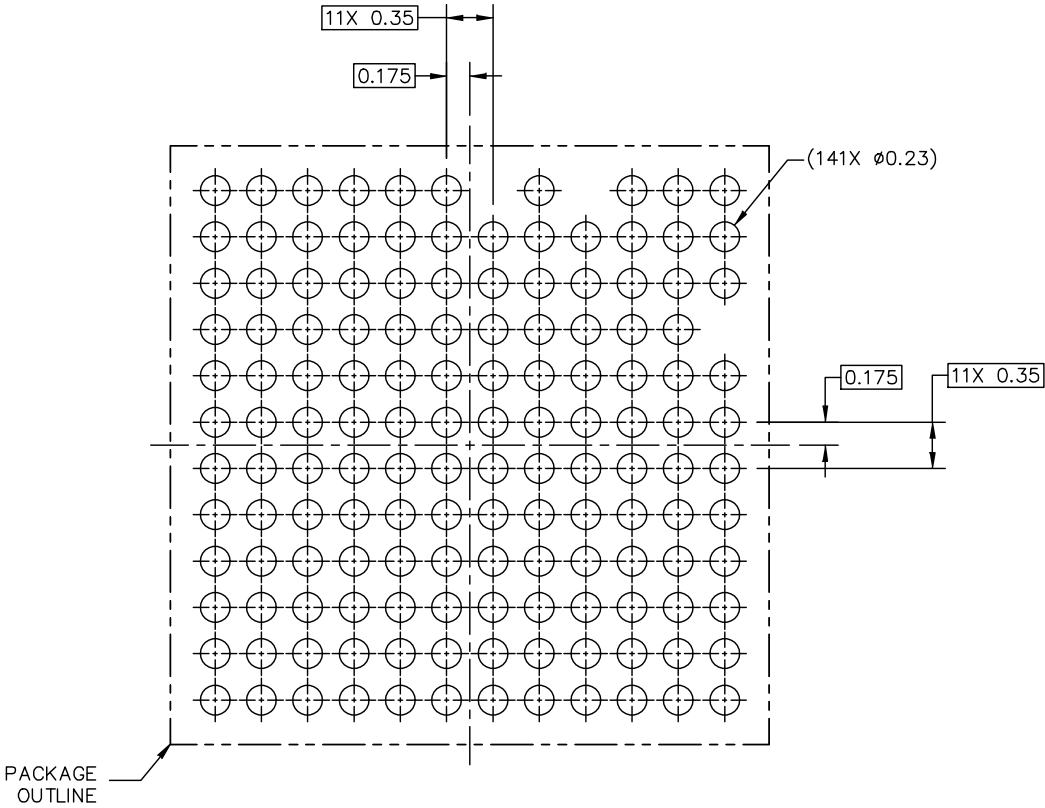
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01653D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP141 (SOT2069-1)

WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

WLCSP-141 I/O
4.525 X 4.525 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01653D	REVISION: 0
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Figure 4. Reflow soldering footprint part3 for WLCSP141 (SOT2069-1)

WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

WLCSP-141 I/O
4.525 X 4.525 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP141 (SOT2069-1)

WLCSP141, wafer level chip scale package, 141 terminals, 0.35 mm pitch, 4.525 mm x 4.525 mm x 0.49 mm body (back side coating included)

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