SOT1782-3

WLCSP64, wafer level chip-scale package; 64 bumps; 3.24 mm x 3.24 mm x 0.625 mm body (backside coating included)

3 August 2018 Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP64
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	02-08-2018
Manufacturer package code	98ASA01270

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	3.24	-	mm
package width	-	3.24	-	mm
seated height	-	0.625	-	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	64	-	

2 Package outline

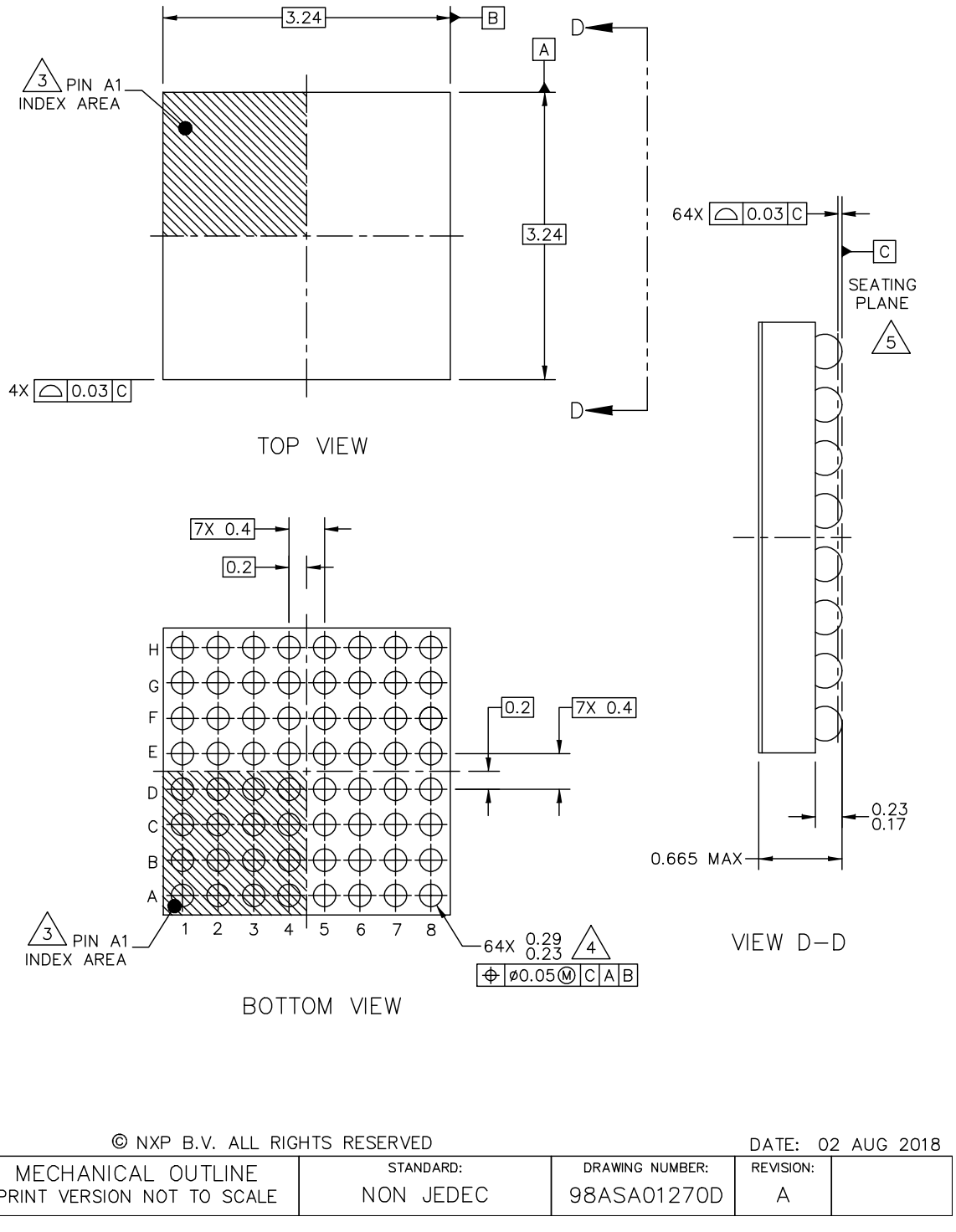


Figure 1. Package outline WLCSP64 (SOT1782-3)

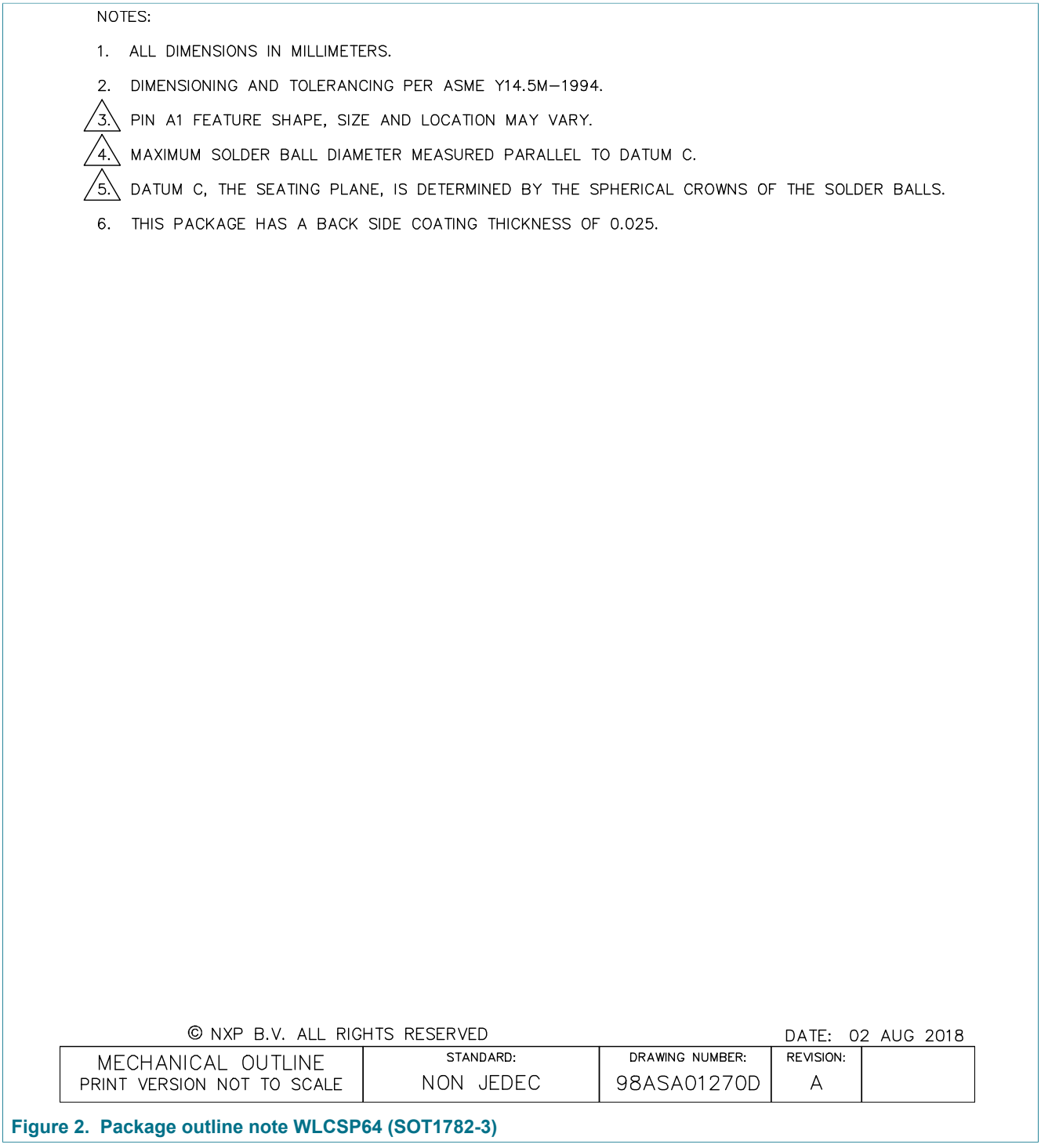
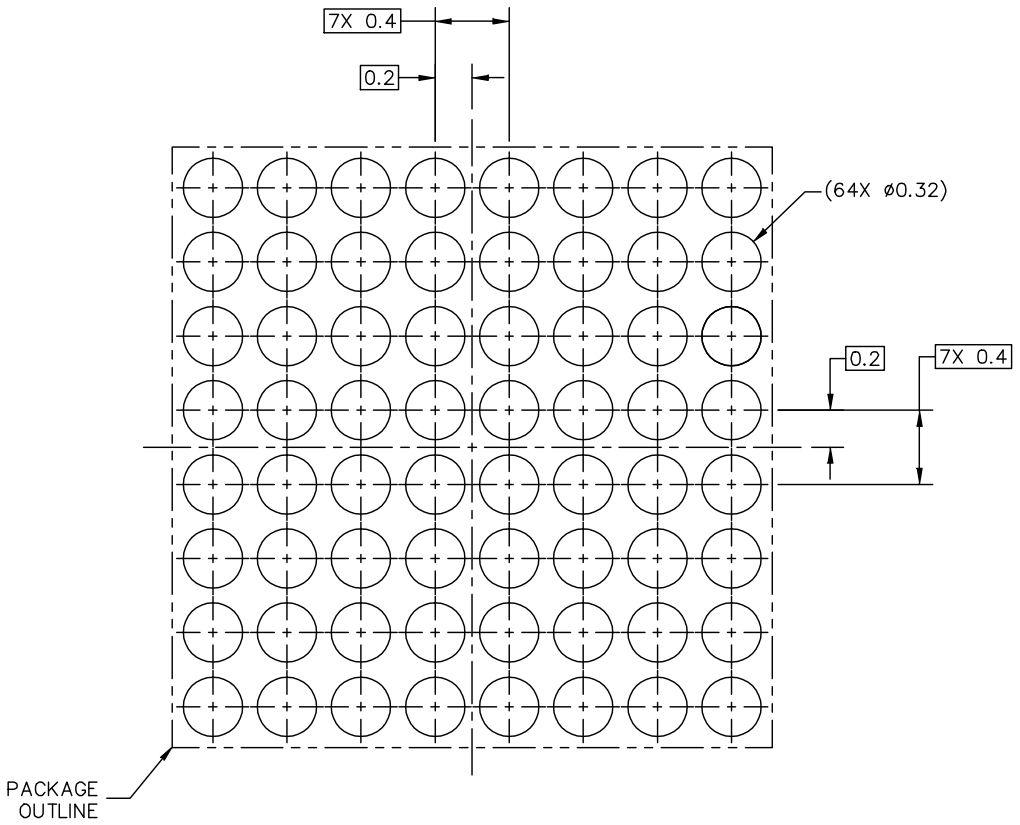


Figure 2. Package outline note WLCSP64 (SOT1782-3)

3 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 02 AUG 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01270D	REVISION: A	

Figure 3. Reflow soldering footprint part1 for WLCSP64 (SOT1782-3)

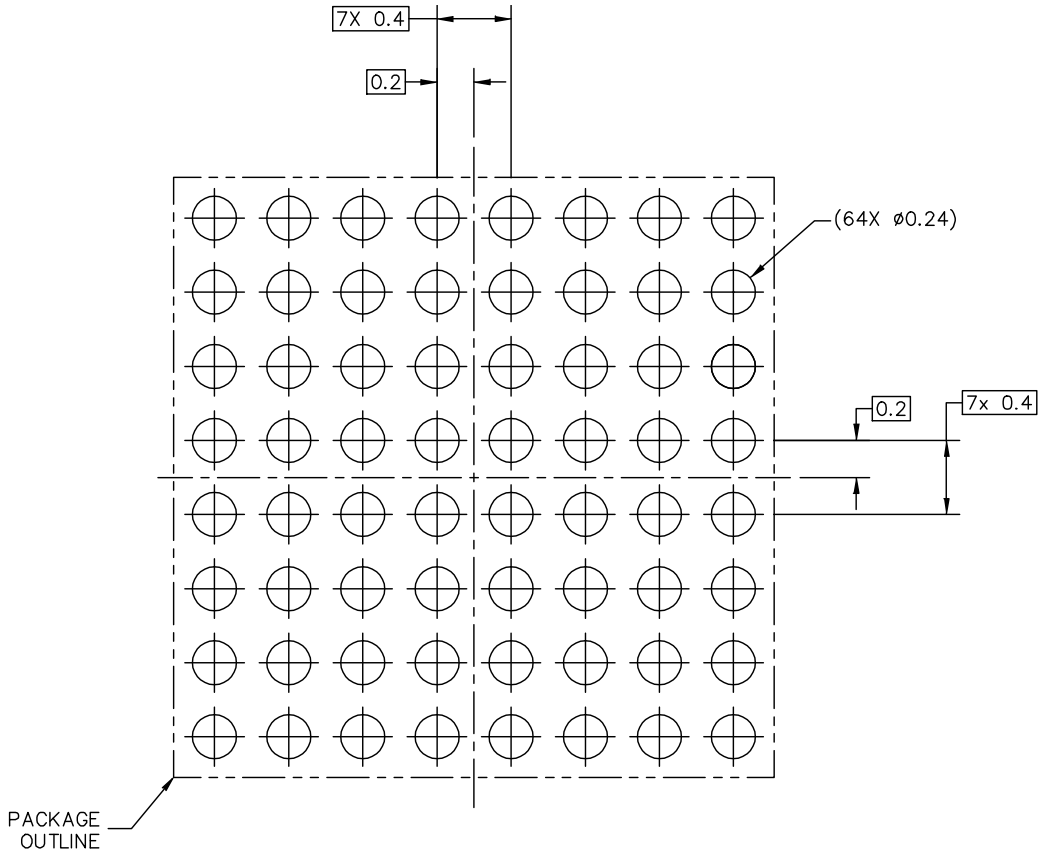


Figure 4. Reflow soldering footprint part2 for WLCSP64 (SOT1782-3)

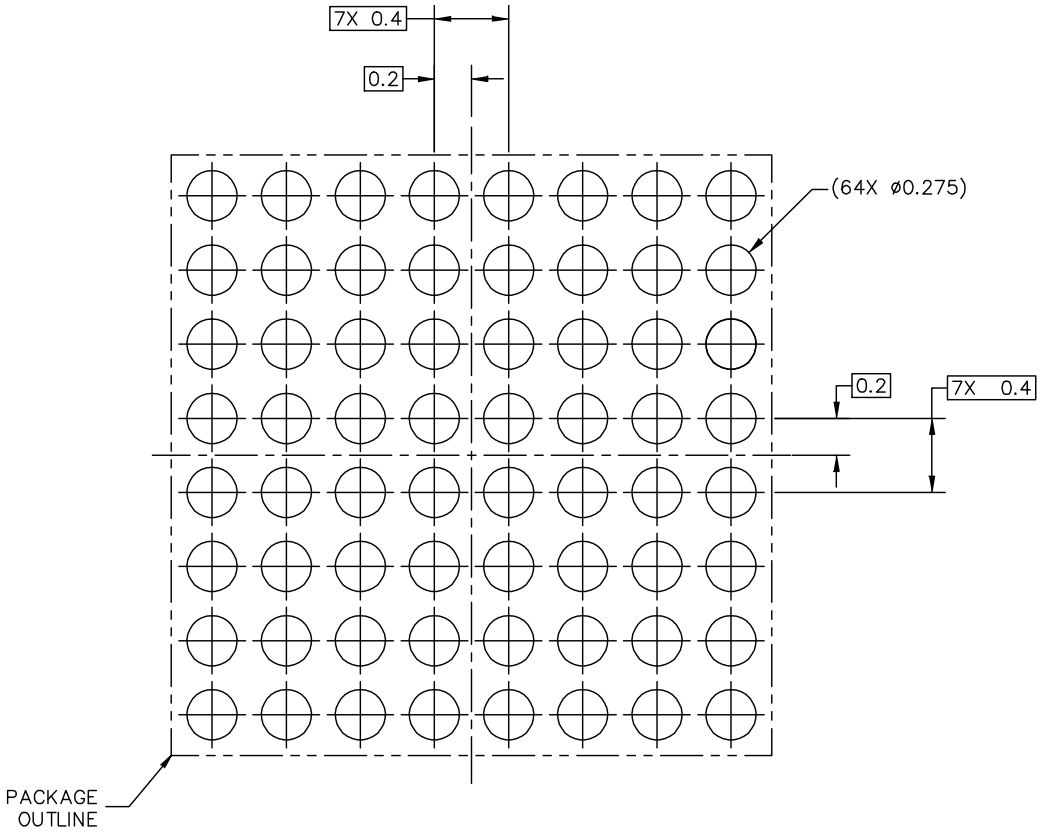


Figure 5. Reflow soldering footprint part3 for WLCSP64 (SOT1782-3)

4 Legal information

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Contents

For more information, please visit: http://www.nxp.com
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