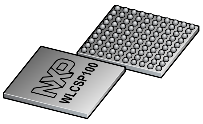


SOT1450-2

WLCSP100, wafer level chip-scale package; 100 bumps; 5.07 mm x 5.07 mm x 0.53 mm body

23 April 2018 Package information

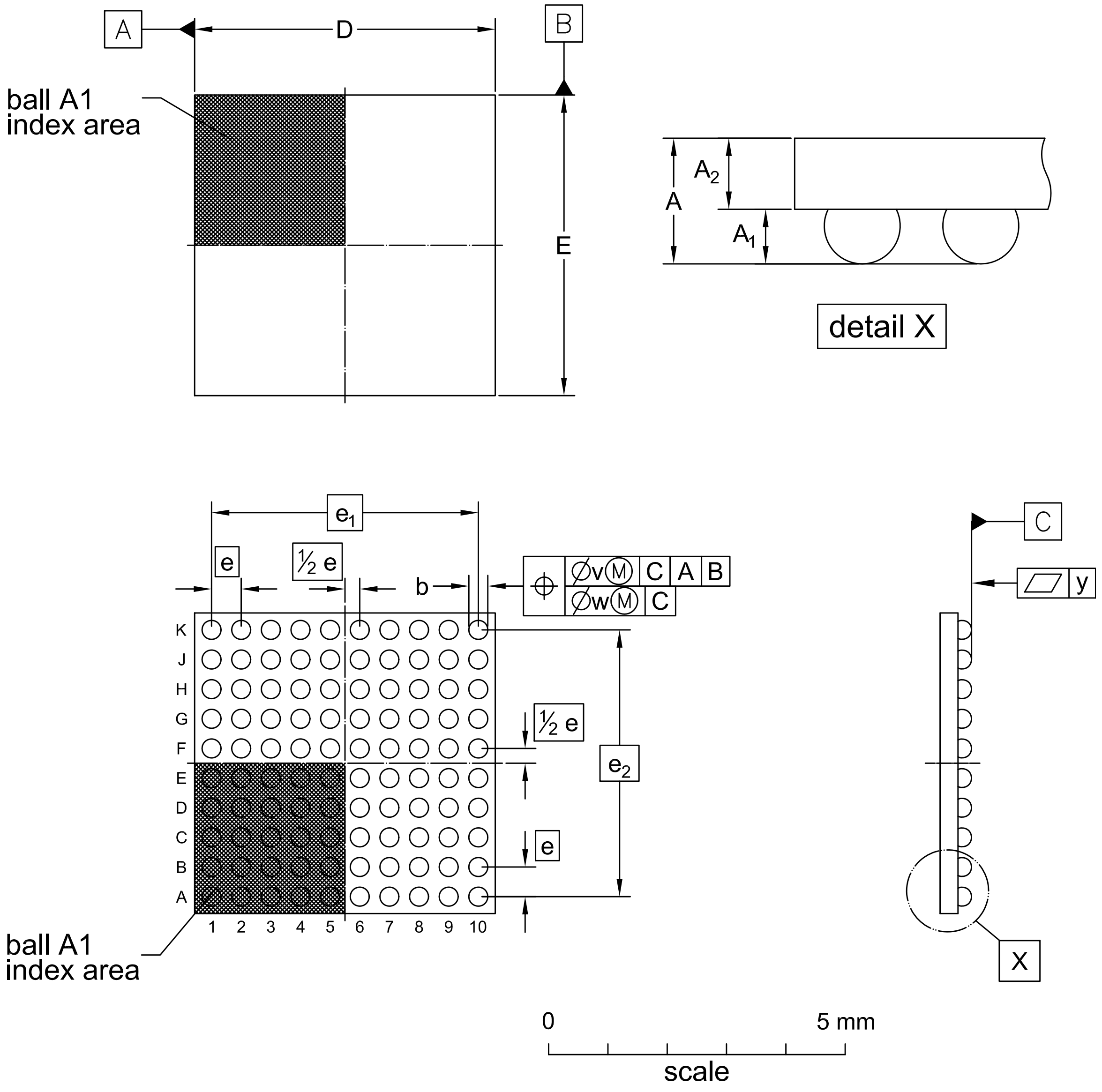
1. Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP100
Package type industry code	WLCSP100
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	6-3-2018
Manufacturer package code	SOT1450-2

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		5.04	-	5.07	5.1	mm
E	package width		5.04	-	5.07	5.1	mm
A	seated height		0.49	-	0.53	0.57	mm
A_2	package height		0.275	-	0.3	0.325	mm
e	nominal pitch		-	-	0.5	-	mm
n_2	actual quantity of termination		-	-	100	-	A/A

2. Package outline

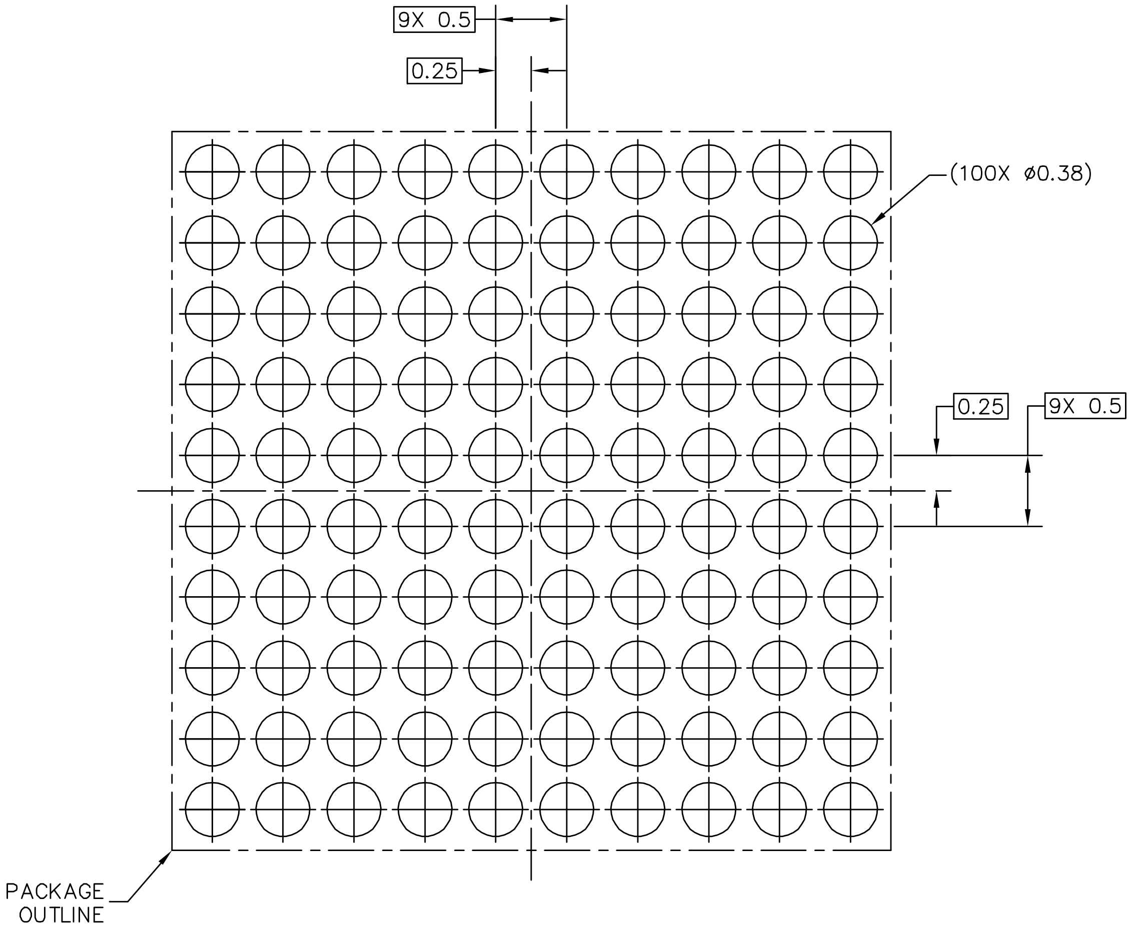


DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX NOM MIN	0.57 0.53 0.49	0.26 0.23 0.20	0.325 0.300 0.275	0.35 0.32 0.29	5.10 5.07 5.04	5.10 5.07 5.04	0.5	4.5	4.5	0.15	0.05	0.03

Fig. 1. Package outline WLCSP100 (SOT1450-2)

3. Soldering



PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN

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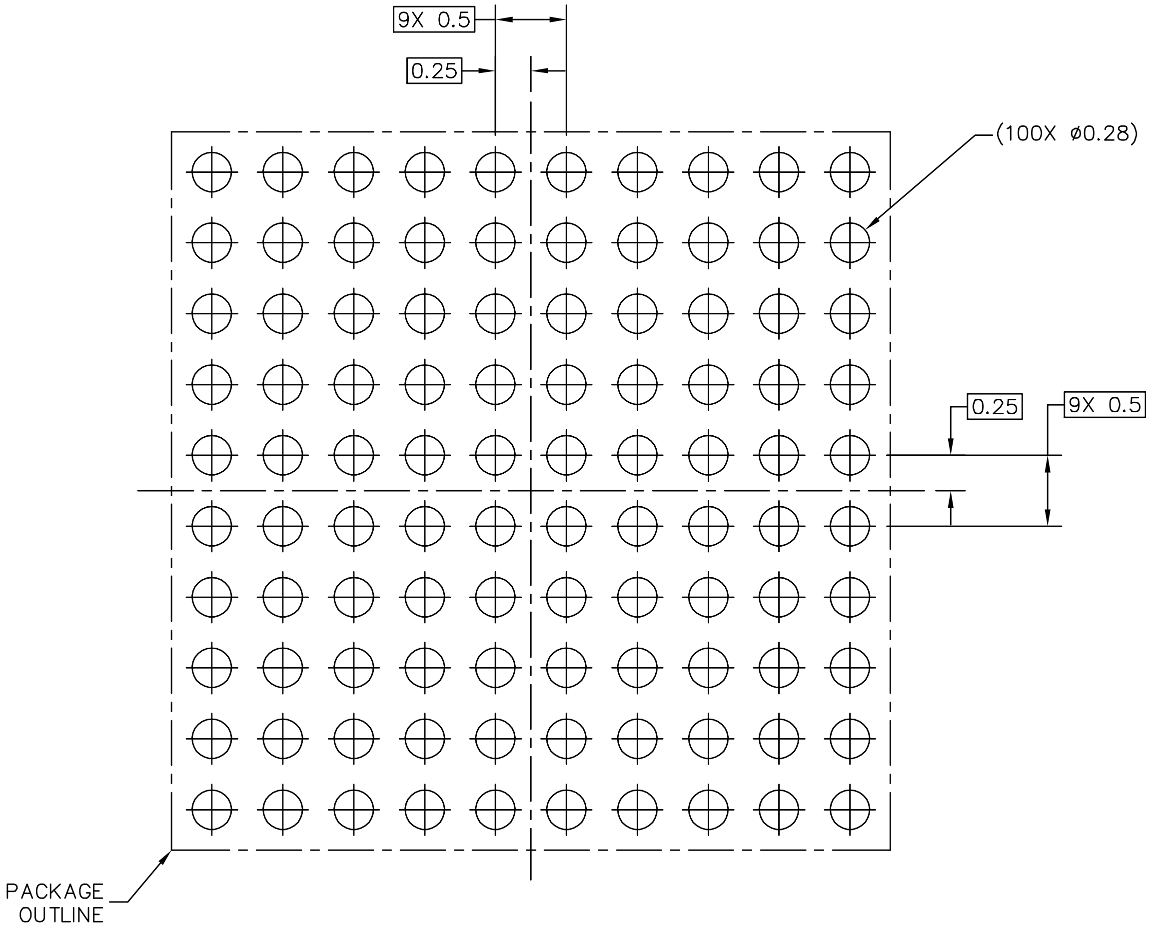
DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450−2	REVISION: 0	

Fig. 2. Reflow soldering footprint for WLCSP100 (SOT1450-2)



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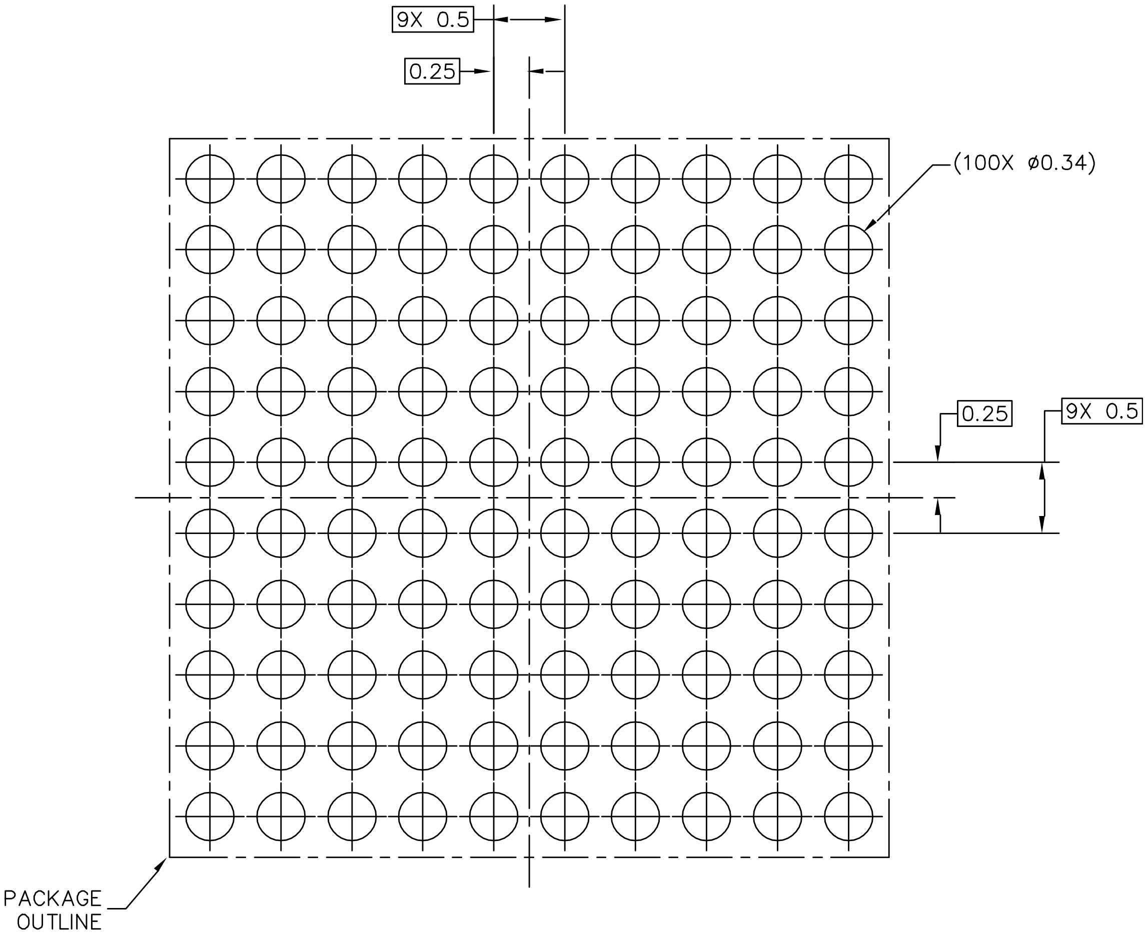
DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450−2	REVISION: 0	

Fig. 3. Reflow soldering footprint part2 for WLCSP100 (SOT1450-2)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450−2	REVISION: 0	

Fig. 4. Reflow soldering footprint part3 for WLCSP100 (SOT1450-2)

4. Legal information

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