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PR533 HW integration guide

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Application note
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Abstract	The PR533 Application note. Description of the PR533 for easier HW integration

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Contact information

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1. Introduction

The PR533 is a highly integrated transmission module for contactless communication at 13.56 MHz including microcontroller functionality based on an 80C51 core.

The PR533 combines a modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz, with an easy-to-use firmware for the different supported modes and the required host interfaces.

The PR533 has also a Master I^2C interface enabling to drive an I^2C peripheral (memory) or contact card reader IC.

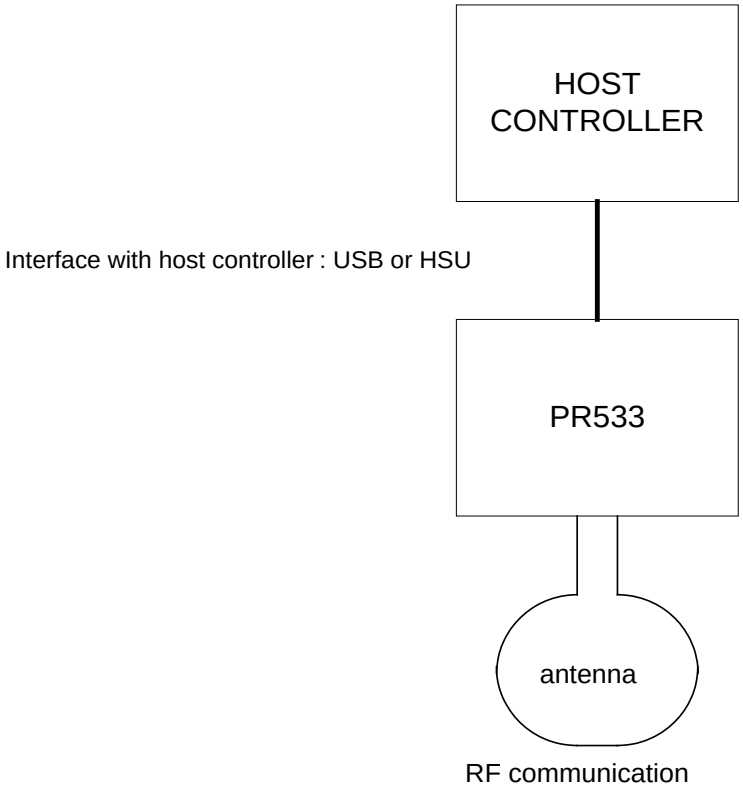

Fig 1. Simplified system view

This document intends to allow the customer designing easily the PR533. It summarizes the PR533 functionalities, and the full configurations to implement them.

More information on how to use the PR533 and detailed description of its firmware, can be found in the PR533 User manual (refer to Section 10 “References”).

More description of the PR533 IC can be found in the PR533 data sheet.

The **PR533** with **embedded firmware** has following features:

- Supports ISO/IEC 14443A reader/writer up to 848Kbit/s
- Supports ISO/IEC 14443B reader/writer up to 848Kbit/s

- Supports MIFARE Classic with 1KB/4KB memory encryption in reader/writer mode at 106Kbit/s
- Supports contactless RF communication according to the Felica protocol at 212 Kbit/s and 424Kbit/s
- Embedded firmware commands allow compliancy with EMVCo v2.0.1 specifications
- Reader mode for Innovision Jewel cards
- Includes 80C51 micro-controller
- Integrated LDO to allow 2.7 to 5.4V power supply voltage
- Integrated antenna component detector
- Host interfaces:
  - USB 2.0 full speed interface
  - High Speed UART (data rate up to 1.288 Mbit/s)
- USB bus-powered or host-powered mode possibility
- On-chip PLL to generate internally 96 MHz for the USB interface
- I^2C master interface to fetch PID, VID, USB descriptor and RF settings from an external EEPROM
- I^2C master interface to support the bridge to the TDA8029 contact reader (2 dedicated GP-IOs)
- 3 additional GP-IOs for external devices control

2. PR533 configuration modes

Default mode of PR533 is standard mode.

To behave in standard mode, two GPIOs need to be configured during the power-on reset phase of the IC.

Notice that no external resistors are needed to pull selection pins to high level; they can be left open.

Table 1. Configuration modes

Mode	Selection Pins	
	P70_IRQ (pin #21)	P35 (pin #20)
Standard	1	1
	0	0
PN512 emulation	1	0
RF field ON	0	1

IC correspondence: In the documents, the following correspondence may be used in the names of the IC:

Table 2. IC correspondence

Commercial name	Application Note name
PR5331C3HN/C360	PR533

2.1 Standard mode

This is the default mode of the PR533. The description of this mode is detailed in this document.

2.2 PN512 emulation mode

In this test mode, the PR533 is configured to act as real PN512 IC using serial interface.

The PN512 is a transmission module for contactless communication at 13.56 MHz. It integrates a modulation and demodulation concept for different kind of contactless communication methods and protocols.

The link used is RS232 at 9600 bauds. It is not possible to change the value of the baud rate.

The emulation of the PN512 IRQ pin is supported as well; the pin used is P70_IRQ.

The level of the P70_IRQ pin is low when an interrupt occurs.

2.3 RFfieldON Mode

In this mode, the PR533 is configured to switch on its RF field immediately after the reset.

The modulation and the baud rate used depend on the selection GPIOs P33_INT1 and P34 and random data bytes are continuously sent.

In this mode, the temperature sensor is not activated, so that tests can be done at temperature higher than 125°C.

Table 3. TX framing and TX speed in RFfieldON configuration

TX framing – TX speed	Selection Pins	
	P33_INT1 (pin #31)	**P34** (pin #34)
MIFARE product - 106 kbps	1	1
	0	0
FeliCa - 212 kbps	0	1
FeliCa - 424 kbps	1	0

3. PR533 block diagram

The PR533 is based on an 8051 core. The chip contains a contactless UART, a contactless front end and a “PCR” block that controls clocks and power.

It can be connected to the host controller through USB or HSU interface. The interface is selected using I0 and I1 pins.

The integrated fractional PLL generates clock for the USB interface from the 27.12MHz crystal oscillator.

The IC can be powered directly from USB supply VBUS (between 4.02V and 5.25V).

An internal voltage regulator (LDO) is used to generate other supply voltages (typical output= 3.3V).

The pad power supply PVDD must be provided between 1.6V and 3.6V.

The PR533 integrates an I²C bus Master interface to drive an external memory EEPROM or a contact reader IC like the TDA8029. External pull-up resistors connected to DVDD supply are mandatory on I²C bus lines.

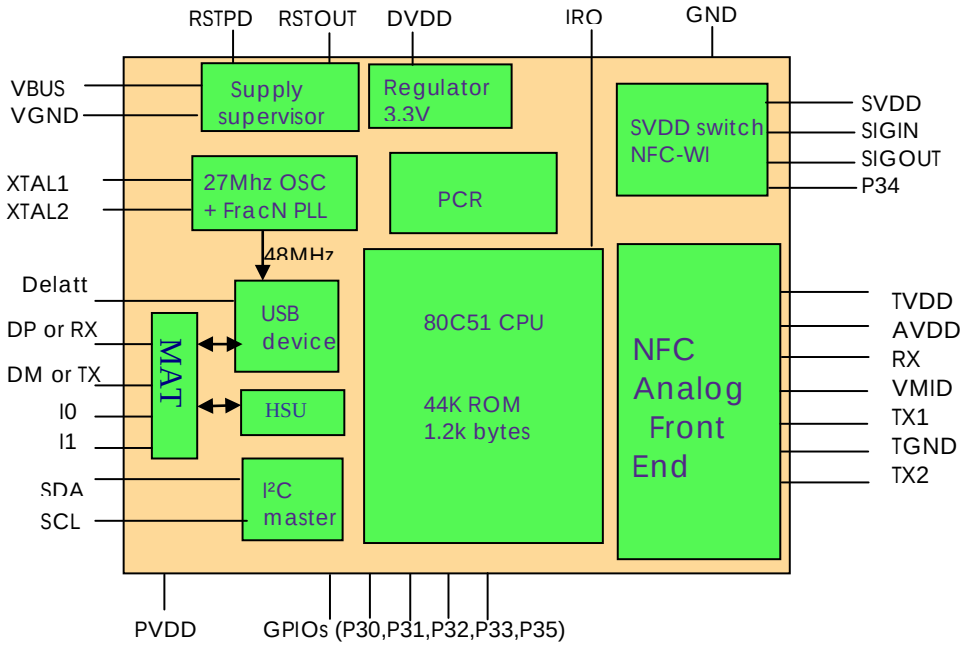

Fig 2. PR533 Block Diagram

4. Power distribution

Here is defined power distribution scheme of the PR533 according to different system configurations.

4.1 USB bus powered application

The PR533 is only supplied by the USB supply (VBUS) and the PR533 internal regulator generates supply voltage for all parts. During power-up phase, inrush current is limited to less than 100 mA. Total current consumption of the PR533 application when RF field is emitted is below 100 mA (=80 mA typical value).

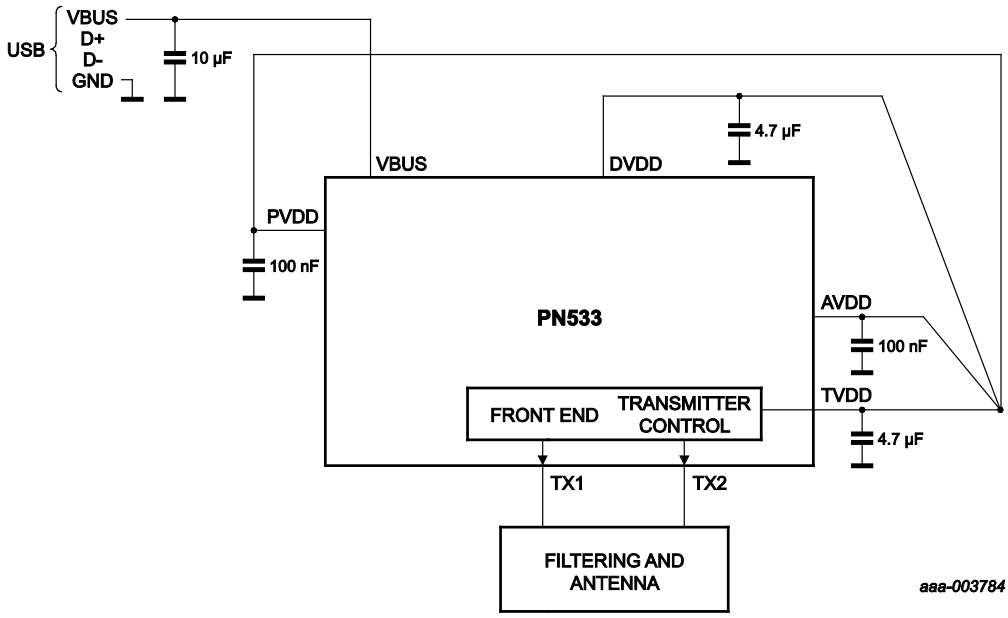

Fig 3. USB Bus powered

4.2 Host powered application (single source)

Host powered application is used when the HSU interface is used; the internal regulator is then deactivated.

Here is the case when the PR533 is supplied by a single power supply source.

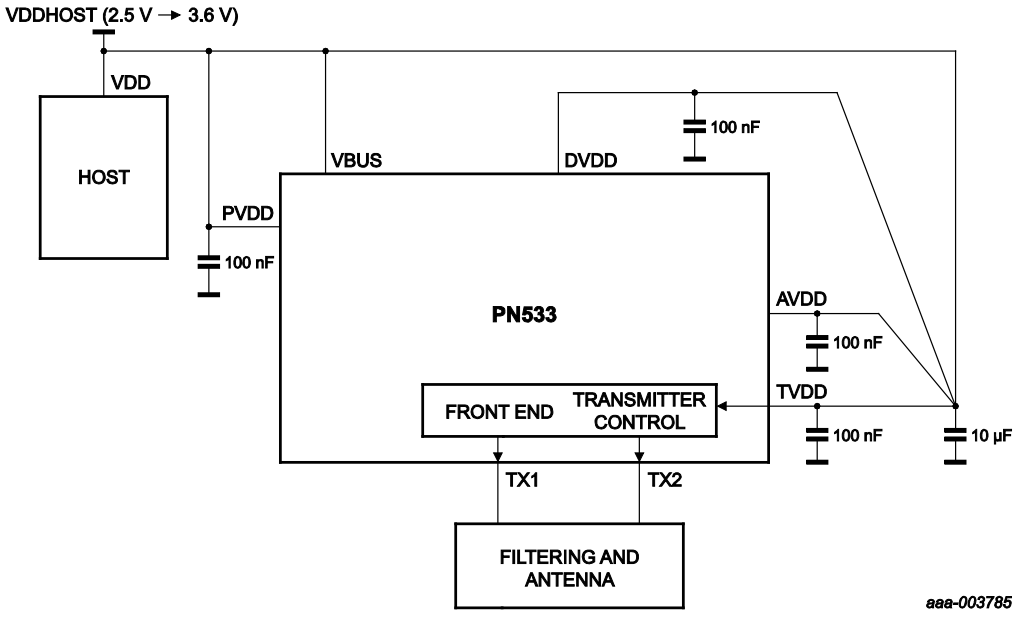

Fig 4. HOST powered application

4.3 Host powered application (two sources)

Host powered application is used when the HSU interface is used; the internal regulator is then deactivated.

Here is the case when the PR533 is supplied by two power supply sources.

Two different power supplies are used for the Host controller interface supply and the PR533 supply. The Host controller supply has to be also connected to the PVDD supply pin of the PR533.

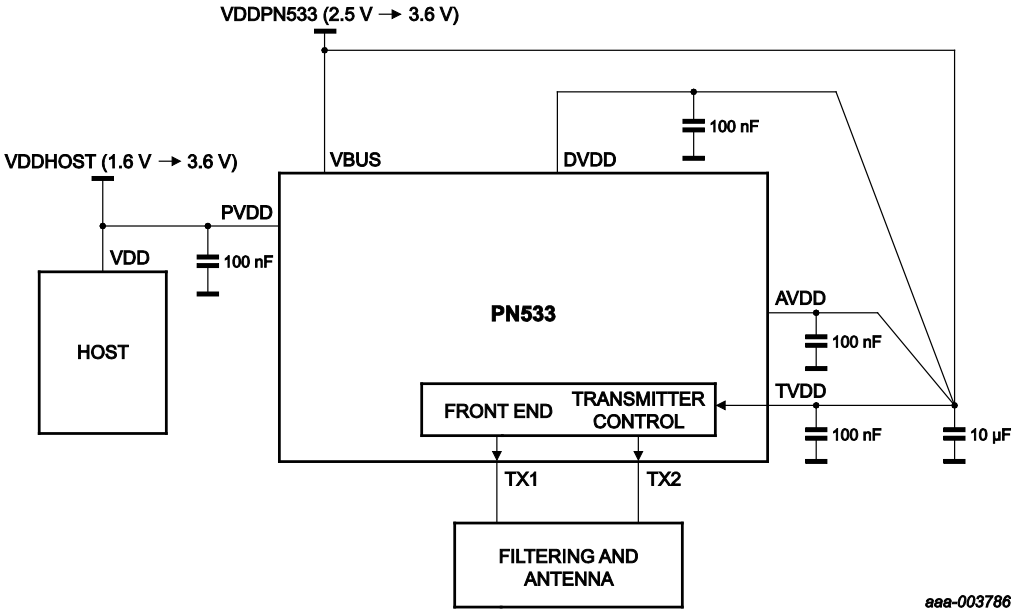

Fig 5. Two power supplies application

5. GP-IOs

4 GP-IOs are available for customer application: P32, P34, P35 and P70.

Other GP-IOs are already used by the embedded software of the PR533; for instance, the link to the smart card contact reader TDA8029 uses P30, P31 and P33.

Available GP-IOs can be accessed directly with the ReadGPIO and WriteGPIO commands: see user manual.

Notice that P32 is also an interrupt input; then setting P32 to zero will prevent the PR533 to correctly enumerate when going out of suspend mode.

P34 is powered by the SVDD supply that is not switched on as default setting. The SVDD supply is used to power a secure element connected to the PR533 via the NFC-WI interface. Therefore, the SVDD supply has to be switched on and P34 has to be enabled before using the P34 GP-IO. It is done by writing to the Control_switch_rng register (address 6106h).

Here is the command to switch on and enable P34:

// Enable the SVDD switch (bit4 = 1) and enable P34 (bit6 = 0)

FF E1 02 01 03 61 06 1B;

// Read and check after writing

FF E1 02 00 02 61 06;

P35 and P70 are used by the PR533 in default mode to drive LEDs as defined by eID requirements. Therefore, these two pins can only be used differently if the automatic LED management is disabled.

To disable it, the host must send an ATD Configuration command with parameter 4 (Byte 4 in data In) equal to 0.

For example, the following command disables the automatic LED management, and keeps the other default parameter of the Automatic Tag Discovery:

FF E1 04 02 05 7F 1E 01 01 03

After this command has been issued, P35 and P70 can be used as standard GPIOs with the Read GPIO and Write PIO commands.

6. Interfaces with the host controller

6.1 Interface selection

The system host controller can communicate with the PR533 by using the USB or the HSU interface.

The pins 24 and 25 of the HVQFN40 package are used for both interfaces. They are referenced to the PVDD supply.

The pin 24 is the DM data line in USB mode or TX in HSU mode.

The pin 25 is the DP data line in USB mode or RX in HSU mode.

The selection of the interface requires a hardware configuration (Interface mode lines I0-I1) during the power up sequence of the chip.

Notice that the HSU interface is selected by connecting the I0 and I1 pins to ground, therefore the internal voltage regulator is deactivated: please refer to the host powered schematic in previous chapter for power supply connection.

Table 4. Interface selection

	Interface Selection Pin	
	I0 (pin #17)	**I1 (pin #18)**
USB	1 DVDD	1 DVDD
HSU	0 Ground	0 Ground
Reserved for Future Use (Don't use)	0 Ground	1 DVDD
	1 DVDD	0 Ground

The embedded software manages the communication with the host controller and the communication on the RF side.

6.2 USB interface

6.2.1 Introduction

The PR533 embeds a USB device interface that enumerates as CCID Class. This Class allows the PR533 to be recognized and the driver automatically installed by the host computer if this CCID driver is available.

This CCID driver is available in most standard OS (Win XP higher than SP3, Windows 7, Most Linux distributions, MAC OS).

In the case the CCID driver is not available and not automatically installed when PR533 is plugged, a simple OS update should resolve the problem.

For deeper description of the USB device of the PR533, refer to the PR533 User Manual.

6.2.2 Hardware

To connect the PR533 to the host through a USB connector, the standard USB pins must be connected: VBUS, D+, D- and GND. These pins must be connected directly to the corresponding pin on the PR533.

VBUS is the only power supply input of the PR533 in this mode. See section Power Distribution for more detail.

In addition, D+ must be connected to the DELATT pin of the PR533 through a 1.5k resistor, in order to allow the PR533 to send the information to the host that it has to be enumerated.

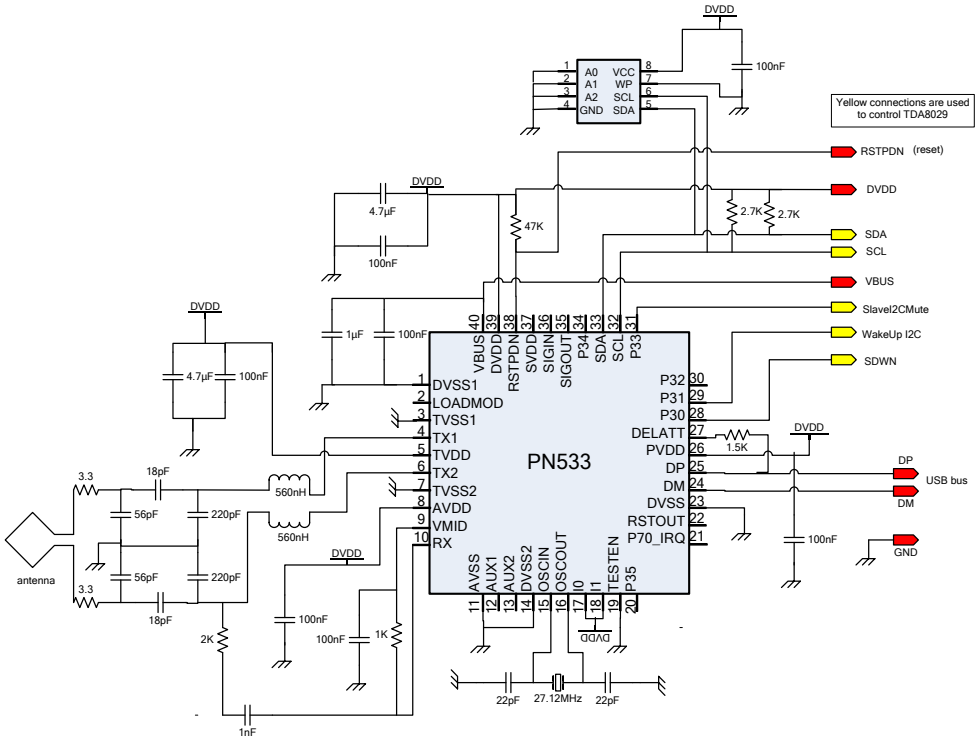

Fig 6. PR533 application diagram: USB interface

6.3 HSU interface

The HSU interface can be used to control the PR533 through a microcontroller using a standard UART.

The default baud rate is 115’200 bits per second. It always starts with this default baud rate and can be changed afterwards with a host command.

6.3.1 Protocol

6.3.1.1 Description

The communication protocol of this HSU link is based on encapsulated CCID Frames. The full frame is built as follows:

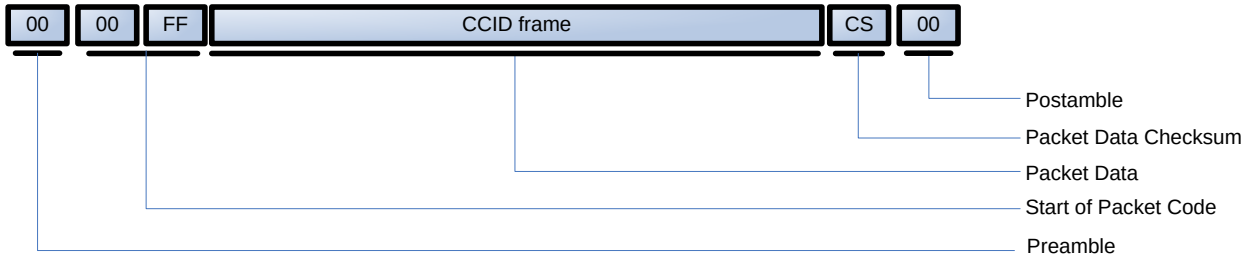

Fig 7. HSU Frame

The CCID frame is defined by the CCID standard.

In this HSU mode, the most command CCID frame is the transceive frame, called PC_to_RDR_XfrBlock. This frame allows to convey a command APDU and its answer.

This Frame composition is given in the next figure.

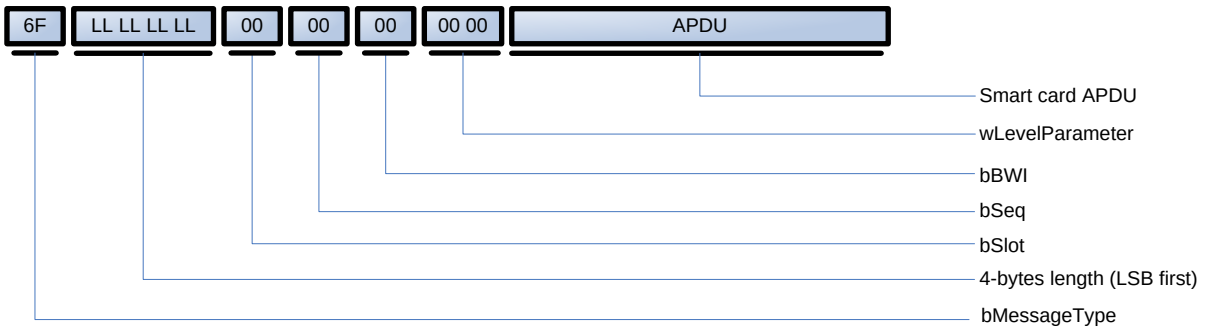

Fig 8. CCID Frame for PR533 HSU communication

The defined parameters are fixed for the communication to the PR533. Only the length and the APDU data must be adapted to the data to be sent.

The APDU can have two destinations:

- Direct communication to the PR533. For this APDU type, refer to the PR533 User Manual UM10463 for a list of all the available commands
- APDU to the Smart card when it is connected. In this case, the APDU is defined by the smart card datasheet.

When the PR533 receives a valid frame, it answers with an ACK frame:

Fig 9. PR533 HSU ACK frame

And finally, the PR533 gives the answer when ready. The structure is the same as the command including the C-APDU:

Fig 10. PR533 HSU answer

6.3.1.2 Example

As an example, the following data represents the HSU exchange during a Firmware version request. The proprietary APDU to send to the PR533 is the GetFWVersion command:

FF E1 00 00 04

Then the frame to send over HSU is

TX → 00 00 FF 6F 05 00 00 00 00 00 00 00 FF E1 00 00 04 A8 00

The PR533 acknowledges the command:

RX ← 00 00 FF 00 FF 00

And answers to the command

RX ← 00 00 FF 80 06 00 00 00 00 00 02 00 00 33 03 60 11 90 00 51

The answer has the same CCID structure as the command. So, the R-APDU is here 33 03 60 11 90 00. The latest 2 bytes mean “OK”, so the Firmware version is **33 03 60 11**.

6.3.1.3 Source code

Next page is an example function source code that builds a frame to be sent to the PR533 when the APDU is provided.

Based on the input (C-APDU), the ccidFrame buffer is built and has simply to be sent to the PR533 through the host ‘s Tx HSU pin.

```
/*-------------------------------------------------------------------------
     --- PR533_BuildCcidFrame ---

   Function to build the CCID frame:
     ------------------------------------------------------------------
     | 00 00 FF | CCID msg type (0x6F) | APDU len LSB first 4 bytes |
     ------------------------------------------------------------------
     ------------------------------------------
     |Parameters 5 bytes 00h | APDU | DCS | 00 |
     ------------------------------------------

- Input:  pBufferReq = pointer to the APDU to send
        BufferReqSize = APDU size
        ccidBuf = pointer to the returned CCID frame
        ccidBufSize = Size of the buffer to return CCID frame

- Output: Result (0 = OK)
 -------------------------------------------------------------------------*/
unsigned char PR533_BuildCcidFrame(unsigned char *pBufferReq, unsigned int BufferReqSize,
unsigned char *ccidBuf, unsigned int ccidBufSize)
{
   unsigned char i, dcs = 0;

//unsigned char *tmpCcidCmd = pBufferReq;

   if (BufferReqSize > ccidBufSize-15)
      return PR533_BUFFERTOOSMALL;

   *(ccidBuf++) = 0x00;
   *(ccidBuf++) = 0x00;
   *(ccidBuf++) = 0xFF;
   *ccidBuf = 0x6F;
   dcs += *(ccidBuf++);
   *ccidBuf = BufferReqSize & 0xFF;          // length LSB
   dcs += *(ccidBuf++);
   *ccidBuf = (BufferReqSize >> 8) & 0xFF;
   dcs += *(ccidBuf++);
   *ccidBuf = (BufferReqSize >> 16) & 0xFF;
   dcs += *(ccidBuf++);
   *ccidBuf = (BufferReqSize >> 24) & 0xFF;    // length MSB
   dcs += *(ccidBuf++);
   *(ccidBuf++) = 0x00;                 // No need to compute DCS as value is 00
   *(ccidBuf++) = 0x00;                 // No need to compute DCS as value is 00
   *(ccidBuf++) = 0x00;                 // No need to compute DCS as value is 00
   *(ccidBuf++) = 0x00;                 // No need to compute DCS as value is 00
   *(ccidBuf++) = 0x00;                 // No need to compute DCS as value is 00

   for (i=0; i<BufferReqSize; i++)
   {
      *ccidBuf = *(pBufferReq++);            // Data
      dcs += *(ccidBuf++);
   }
   *(ccidBuf++) = (unsigned char) 0x100 - dcs;      // Checksum
   *ccidBuf = 0x00;                      // Postamble

   return PR533_OK;

}
```

Fig 11. PR533 HSU mode – Build CCID frame

6.3.2 Hardware

When HSU mode is used, the below diagram must be followed. HSU uses only two pins: TX and RX.

TX is the data pin from PR533 to the host and must be connected to the D- pin of the PR533, while RX is the data pin from host to PR533 and must be connected to the D+ pin of the PR533.

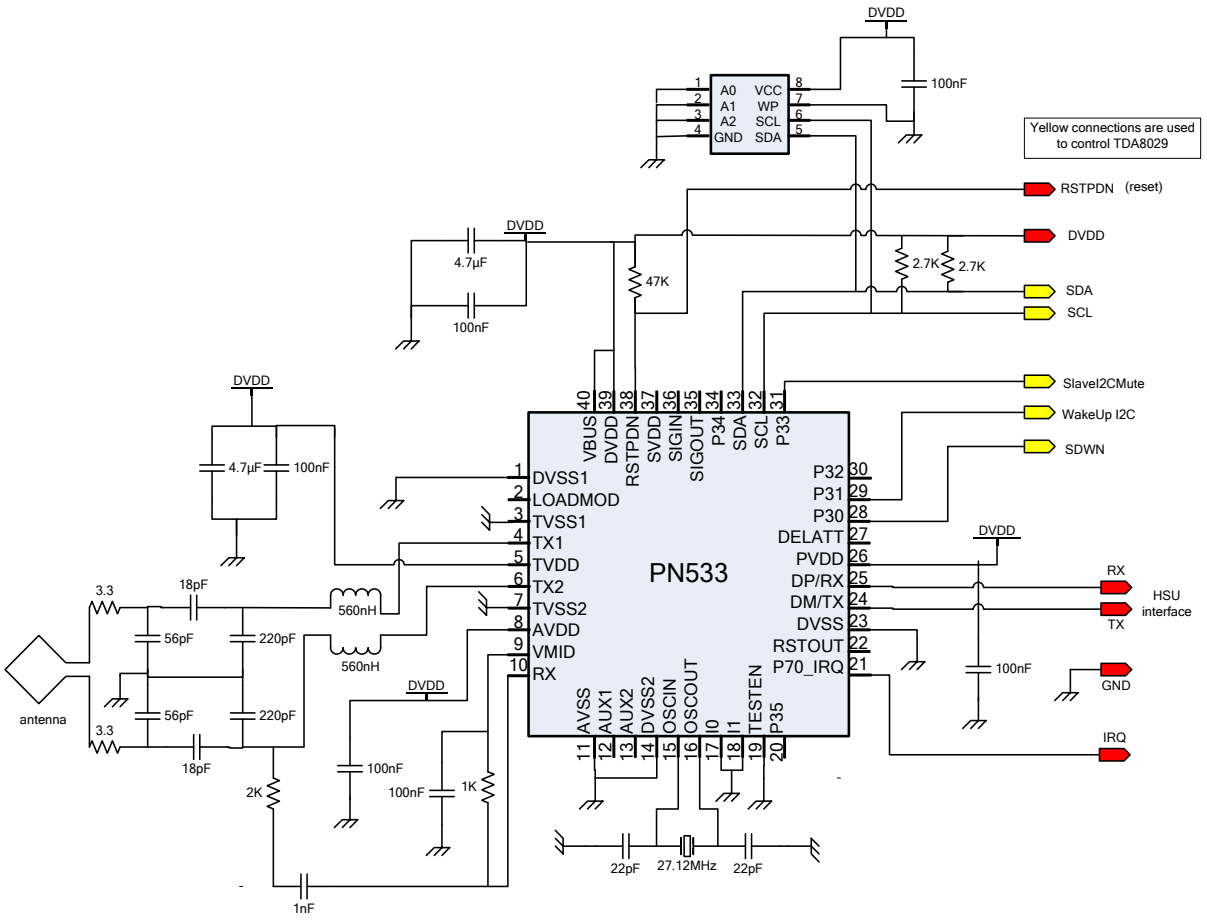

Fig 12. PR533 application diagram: HSU interface

In this mode, the PR533 must be powered according to the Power Distribution section.

7. I²C master interface

The I²C master interface of the PR533 is compliant with the I²C bus specification.

The PR533 is configured as master and is able to communicate with an EEPROM (address 0xA0) and a smart card reader (address 0x50).

- Serial data line (SDA), has to be connected to pin 33 of the PR533
- Serial clock line (SCL), has to be connected to pin 32 of the PR533.

External pull-up resistors have to be connected to DVDD supply (=3.3V).

For both connections, the communication mode is fixed. It means that the host cannot use the I²C master to drive any other device than the ones allowed by the PR533.

The PR533 will then handle the full communication for each device.

7.1 I²C EEPROM

7.1.1 Use of EEPROM

The EEPROM can be used to provide specific information about the reader: PID, VID, name, and customized settings (bit rates, RF Settings…)

The PR533 can read and write information from EEPROM connected on its I²C bus with I²c address equal to 0xA0.

The protocol used to access this EEPROM is fixed and fits with most of the I²C EEPROM available in the market.

The specification of the used EEPROM should fulfill the following requirements:

a. I²C address 0xA0

b. Clock frequency > 400 kHz

To get the data from the EEPROM, the following sequence is applied:

Table 5. Sequence of reading information on I²C EEPROM to perform enumeration

Step	Description
1	When the PR533 is supplied, it shall check if USB information is contained in the EEPROM
2	During this step, PR533 will look for tags: 0x02, 0x03, 0x04 and 0x05 (see data organization in following chapter). Once a tag is discovered, the firmware will read the content of its associated block and save it in RAM. If the 4 blocks have been read correctly in EEPROM, this information is used as initial values after power-on, otherwise ROM code information is used as initial values after power-on.
3	PR533 shall active the USB_SoftConnect switch. The voltage of D+ will be set to ‘1’ (see next figure).
4	The host shall detect this voltage change and it shall send a request to ask for USB device information for the enumeration phase.
5	The PR533 has to fill the IN Bulk Endpoint with its USB information.
6	The Host has to read the content of the IN Bulk Endpoint. After this reading, the PR533 should be correctly enumerated.

7.1.2 Hardware

The EEPROM must be connected using the following schematics:

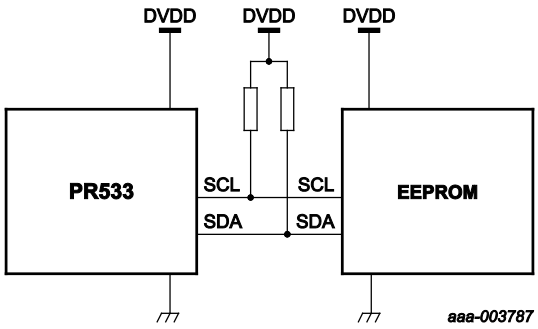

Fig 13. EEPROM connection

7.1.3 EEPROM data

7.1.3.1 Data organization

The data structure in EEPROM must follow the defined rules. This chapter introduces to these rules, but the full description can be found in the PR533 User Manual.

The data organization in EEPROM has to respect the following structure:

Fig 14. EEPROM Data organization

Each tag represents one parameters block. Each block must respect its own structure. (cf. User Manual UM10463).

Each tag must be present and must respect its own defined structure otherwise the full information in EEPROM becomes useless. In this case the PR533 uses its default ROMed values, as if no EEPROM were present.

7.1.3.2 Data access

The EEPROM can be filled before the manufacturing of the PCB. In this case, at first start the PR533 will be used the EEPROM information if they are correct.

Another possibility is to build the PCB with a blank EEPROM, and write it afterwards during the production test for instance. The PR533 gives access to the EEPROM data through the host interface.

To access to the EEPROM, the Read Register and Write Register commands can be used. They are fully defined in UM10463.

Each byte of the EEPROM can be accessed through the address A0XXh, where XX is the address of the byte in the EEPROM.

For example, the following command APDU writes ABh in EEPROM at its location 12h:

FF E1 02 01 03 A0 12 AB

If the EEPROM is correctly connected, the answer should be **90 00**.

This APDU reads back data from addresses 12h of EEPROM:

FF E1 02 00 02 A0 12

The answer should be **AB 90 00**.

7.2 TDA8029 over I²C

The host I²C interface of the PR533 provides a link to a contact smart card interface from NXP called TDA8029. This device is a standalone contact smart card reader, embedding a full low-level protocol to communicate with smart cards.

The PR533 embeds a full driver allowing the user to control the TDA8029. As this driver is dedicated to TDA8029, it is not possible to use any other smart card reader or device that uses I²C.

7.2.1 Hardware connections

The maximum SCL frequency used for transactions with the TDA8029 is less than 50 kHz.

- Pin 1 of the TDA8029 has to be connected to ground to enable I2C interface.
- Pin 25 is connected to VDD to enable Energy Saving Mode (ESM).
- SDA is connected to pin 32 of the TDA8029.
- SCL is connected to pin 2 of the TDA8029.

In addition to I2C bus specification, we shall use three other lines to manage Energy Saving Mode (ESM) mechanism of the TDA8029.

- WakeUpSlave line is used to wake up the TDA8029. It has to be connected between INT1 (pin 30 of the TDA8029) and P31 (pin 29) of the PR533.
- SlaveI2CMute line is used by the TDA8029 to indicate to the host controller either that it is ready to receive a command frame, or to send the corresponding answer, or to signal a hardware event. It has to be connected between pin 24 of the TDA8029 and P33 (pin 31) of the PR533.
- Shut-down line is used for entering in the TDA8029 shut-down mode. This mode is set when the TDA8029 SDWN_N pin is set to 0. The only way to leave shut-down mode is when pin SDWN_N is set to 1. The SDWN_N pin has to be connected to P30 (pin 28) of the PR533.

For a full description of the TDA8029 hardware connections, refer to its application note AN10207: http://www.nxp.com/pip/TDA8029.html.

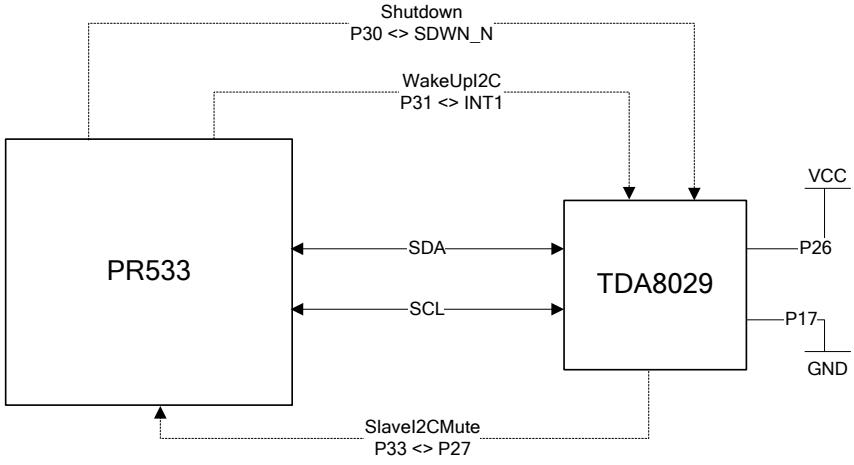

Fig 15. PR533 and TDA8029 connections

Warning: The contact reader TDA8029 is used only as a SAM reader; it cannot be EMVCo approved when Energy Saving Mode is used (clock-stop mode is not allowed).

The PR533 contactless application can be EMVCo approved.

When EEPROM transactions are performed, the TDA8029 has to be in Shut-down mode (SDWN pin has to be set to 0) in order not to disturb the TDA8029. At the end of transactions with the EEPROM, the TDA8029 has to leave shut-down mode (SDWN pin has to be set to 1). This is done by using the command SetParameters with flag bit fTDApowered (see user manual UM10463).

7.2.2 TDA8029 communication protocol

To control the TDA8029 through the PR533, the host must know the communication protocol of the TDA8029, called ALPAR, and encapsulate the full ALPAR command into a control APDU.

The ALPAR protocol and all commands accepted by the TDA8029 are described in AN10207.

Once the TDA8029 has been powered using the fTDApowered bit, ALPAR commands can be sent encapsulated in a specific APDU:

Fig 16. TDA8029 command

If the communication between the PR533 and the TDA8029 is performed correctly, the PR533 answers with an R-APDU including the TDA8029 answer, followed by “90 00”:

Fig 17. TDA8029 response

7.3 Typical application schematics

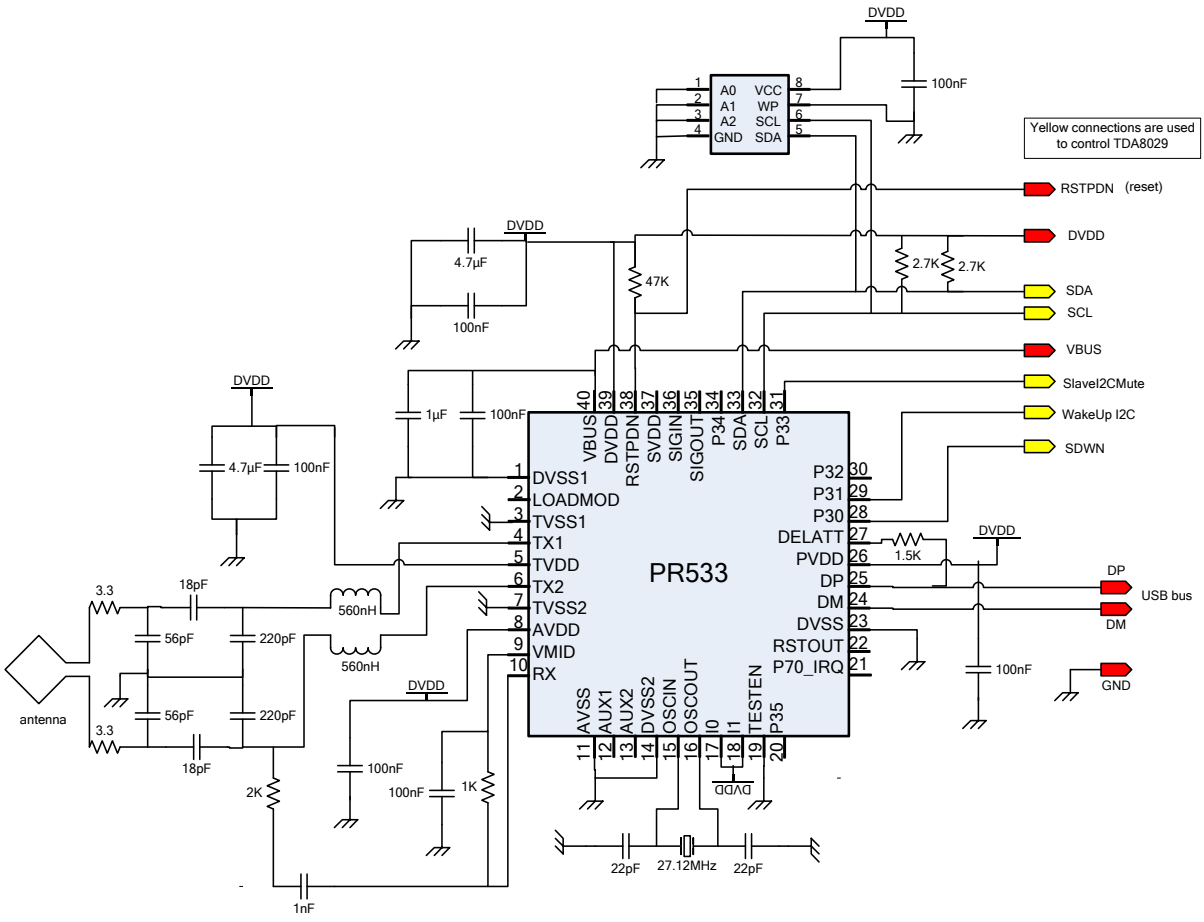

Fig 18. PR533 application diagram: USB interface

Antenna and RF design guide AN1445 gives detailed information about external components to be used with RF transmitter and receiver.

It is an USB bus powered application.

VBUS is the power supply provided by USB link.

DVDD supply is output from PR533 internal regulator and it has to be externally connected to other supply pins AVDD, TVDD and PVDD.

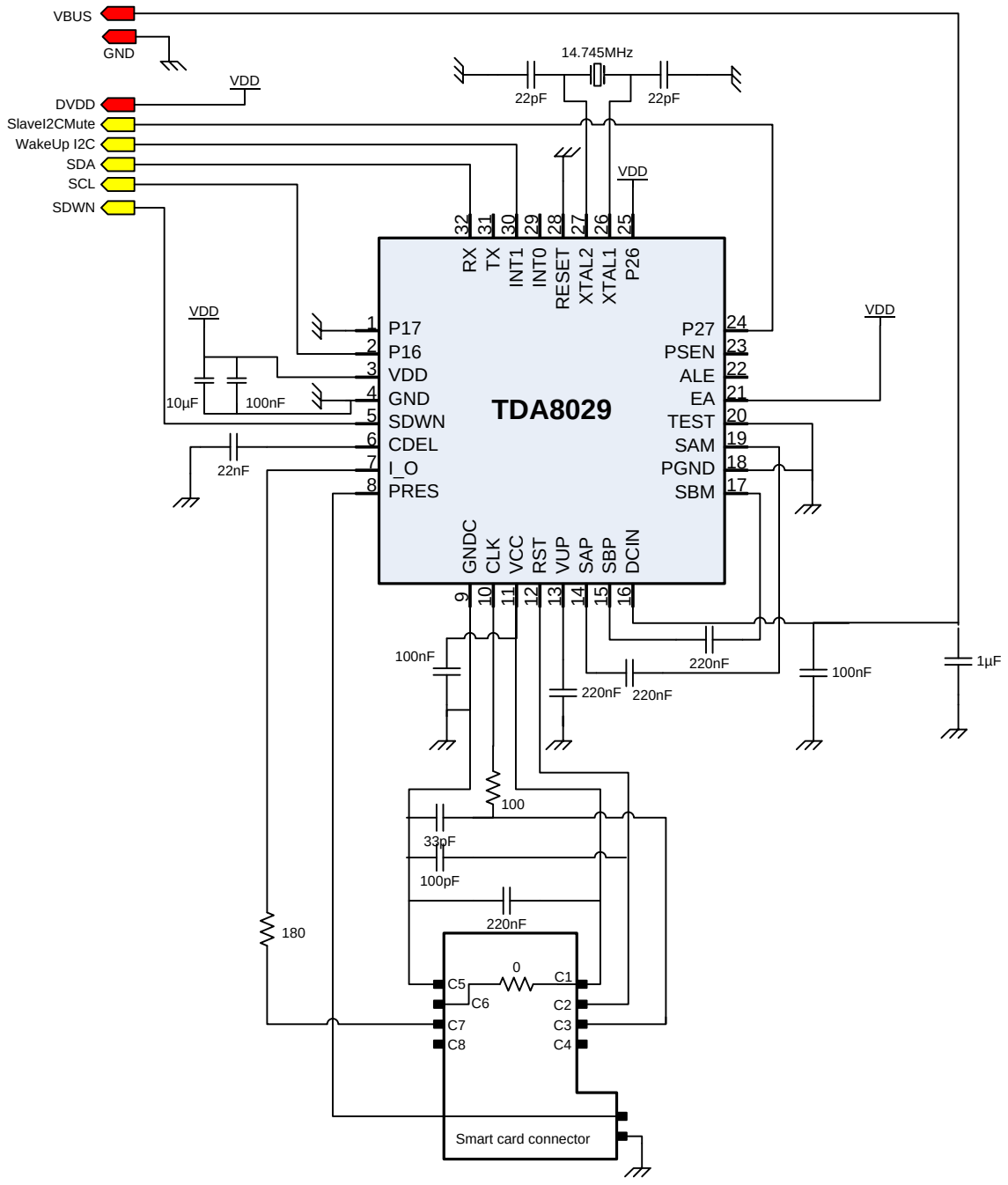

Fig 19. TDA8029 application diagram (Energy Saving Mode enabled)

DVDD output (=3.3V) from the PR533 is used as VDD supply for the TDA8029.

VBUS supply (>4.2V) from the USB bus is used as DCIN supply for the TDA8029.

DVDD cannot be used as DCIN supply because current consumption may be as high as 250 mA.

8. EMVCo compliancy

8.1 Protocol

The embedded firmware command InActivateDeactivateCard with EMVCo option (see user manual) allows compliancy with EMVCo v2.0.1 specifications with respect to the protocol. This command fully takes in charge Polling / Anti-Collision / Activation and PICC removal procedure with respect to the EMVCo specifications.

8.2 RF power and signal interface

The EMVCo contactless specifications define an operating volume where a minimum magnetic field strength has to be provided. This field strength cannot be achieved in all the operating volume by the transmitter of the PR533 because it is powered by a typical supply voltage of 3.3V only.

An external RF amplifier is needed. This RF amplifier is made of few discrete components and it is connected to TX1, TX2 outputs of the PR533 transmitter instead of the usual matching/ tuning antenna network.

An additional power supply is needed to power this external RF amplifier. Depending on the application environment, a supply voltage of 6V may be needed to fulfill the EMVCo specification. Typical current consumption is around 150mA. The implementation of the RF amplifier is fully described in the application note AN1425xx.

Here is a block diagram of a complete EMVCo compliant application:

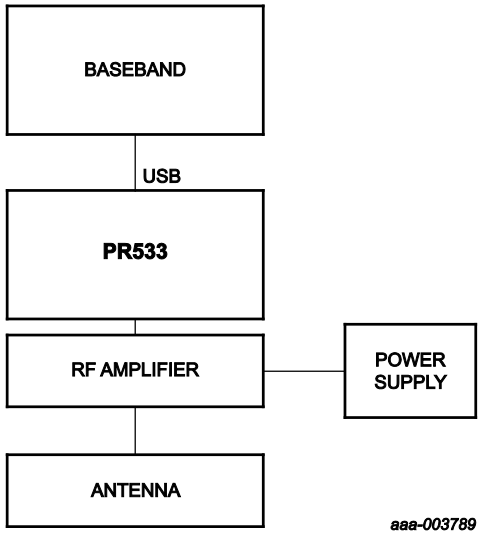

Fig 20. EMVCo compliant application

Following are an example of schematics of the RF amplifier, and the list of components.

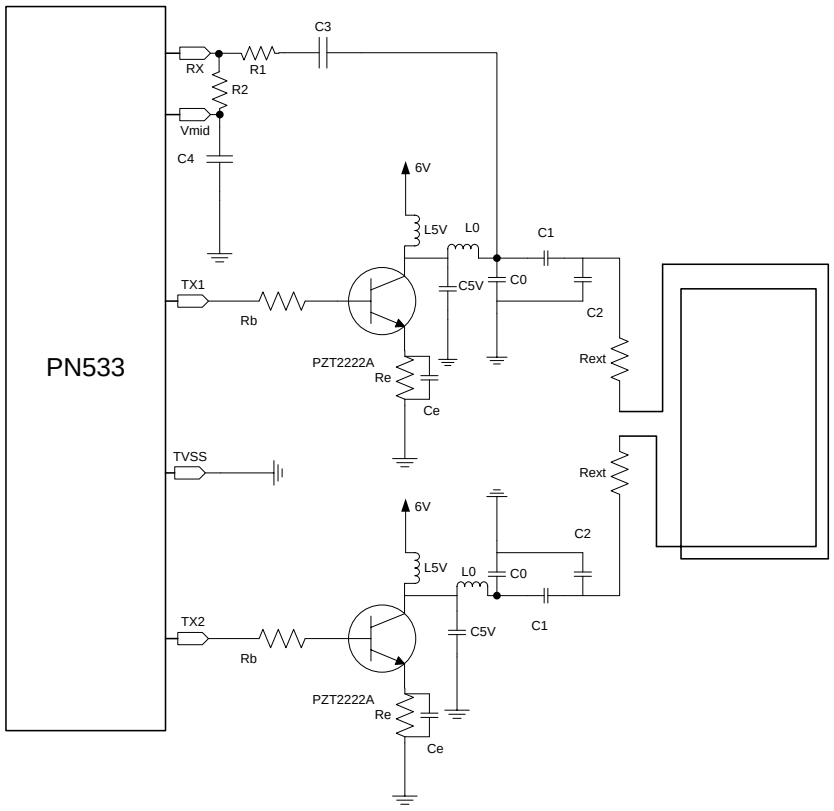

Fig 21. RF Amplifier schematics

Components	Values
C_0	180pF
C_1	68pF
C_2	280pF
C_3	1nF
C_4	100nF
C_{5V}	91pF
C_e	22pF
L_0	560nF
L_{5V}	1.5uH, Q>=20 @ 13.56MHz
R_1	3.3kR
R_2	1kR
R_b	22R
R_e	18R
T_1, T_2	PZT2222A

Fig 22. RF Amplifier components

9. Abbreviations

Table 6. Abbreviations

Acronym	Description
CIU	Contactless Interface Unit
EMV	Europay MasterCard Visa
HSU	High Speed UART
I^2C	Inter Integrated Circuit
PCD	Proximity Coupling Device
PCR	Power, Clock and Reset controller
PICC	Proximity Integrated Circuit Card
PMU	Power Management Unit

10. References

[1] **PR533 User Manual** – UM10463.pdf

[2] **PR5331C3HN data sheet** - PR5331C3HN_SDS.pdf

[3] **ISO/IEC 14443-2** - Identification cards – Contactless integrated circuit(s) cards Proximity card(s) - Part 2: RF power and signal interface

[4] **ISO/IEC 14443-3** - Identification cards – Contactless integrated circuit(s) cards - Proximity card(s) - Part 3: Initialization and anti-collision

[5] **ISO/IEC 14443-4** - Identification cards – Contactless integrated circuit(s) cards - Proximity card(s) - Part 4: Transmission protocol

[6] **AN1445**[1)] **NFC Transmission Module Antenna and RF Design Guide** - AN1445**.pdf

[7] **AN1425****- RF amplifier for NXP contactless NFC reader ICs

[8] **USB** - Universal Serial Bus Specification

[9] **I2C** - I^2C bus Specification

[10] **EMVCo** - EMV Contactless Communication Protocol Specification V2.0.1

(1) ** … document version number

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