



Ultra-Reliable MCUs

# Why Ultra-Reliable Processors Matter

Freescal's portfolio of ultra-reliable processors is the broadest in the industry and is ideal for challenging environments found in industrial, infrastructure, automation, communications, transportation and medical applications. It offers best-in-class quality, reliability and safety for applications that need to perform in the harshest environments.

## Why Safety Matters

- Eliminate risks due to hazards caused by malfunctioning of electronic systems
- Avoid random failures, main impairment to safety

<div>Single Point Failure</div> <div>Immediate potential for hazard</div>	<div>Latent Failure</div> <div>Danger with second fault</div>	<div>Common Cause Failure</div> <div>Annul redundancy-based measures</div>
<div></div>	<div></div>	<div></div>
<div>Freescal Solution</div> <ul style="list-style-type: none"><li>• Structure redundancy [Core, DMA]</li><li>• Information redundancy [E2E, ECC, EDC]</li></ul>	<div>Freescal Solution</div> <ul style="list-style-type: none"><li>• Hardware self test [memory, logic]</li><li>• 90% stuck-at-fault</li></ul>	<div>Freescal Solution</div> <ul style="list-style-type: none"><li>• Delayed checker core</li><li>• Clock, temp, power monitor</li><li>• Independent safety clock</li></ul>

## What Makes an MCU Ultra-Reliable?

Features	Ultra-Reliable	Consumer	Traditional Industrial	Reliable
Dielectric Lifetime (TDDB)	<ul style="list-style-type: none"> <li>&lt; 1ppm</li> <li>Auto-specific model</li> <li>Voltage limit checking</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Standard model</li> <li>Subset voltage limit checking</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Industrial model / standard model</li> <li>Subset voltage limit checking</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 10 ppm</li> <li>Auto-specific model</li> <li>Voltage limit checking</li> </ul>
Transistor Aging (HCI, BTI)	<ul style="list-style-type: none"> <li>Circuit use-profile</li> <li>Custom-aged model</li> </ul>	<ul style="list-style-type: none"> <li>Limited margining</li> </ul>	<ul style="list-style-type: none"> <li>Limited margining</li> </ul>	<ul style="list-style-type: none"> <li>Circuit use-profile</li> <li>Custom-aged model</li> </ul>
Metalization Reliability (Electromigration)	<ul style="list-style-type: none"> <li>&lt; 1 ppm</li> <li>Current mode/ profile specific</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Current mode/ profile specific</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Current mode/ profile specific</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 10 ppm</li> <li>Current mode/ profile specific</li> </ul>
Metalization Reliability (Stress Migration)	<ul style="list-style-type: none"> <li>Zero failure in stress</li> <li>Geometry specific design rules</li> </ul>	<ul style="list-style-type: none"> <li>Zero failure in stress</li> <li>Geometry specific design rules</li> </ul>	<ul style="list-style-type: none"> <li>Zero failure in stress</li> <li>Geometry specific design rules</li> </ul>	<ul style="list-style-type: none"> <li>Zero failure in stress</li> <li>Geometry specific design rules</li> </ul>
Metalization Dielectric Lifetime (TDDB)	<ul style="list-style-type: none"> <li>&lt; 1 ppm</li> <li>Auto-specific model</li> <li>Geometry / use condition design rules</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Standard model</li> <li>Subset voltage limit checking</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 1000 ppm</li> <li>Industrial model /standard model</li> <li>Subset voltage limit checking</li> </ul>	<ul style="list-style-type: none"> <li>&lt; 10 ppm</li> <li>Auto-specific model</li> <li>Geometry / use condition design rules</li> </ul>
Radiation Immunity (SER / SEL)	<ul style="list-style-type: none"> <li>SER: &lt; 1 FIT</li> <li>SEL: &lt; 0.1 FIT</li> </ul>	<ul style="list-style-type: none"> <li>SER: &lt; 100000 FIT</li> <li>SEL: &lt; 1000 FIT</li> </ul>	<ul style="list-style-type: none"> <li>SER: &lt; 1000 FIT</li> <li>SEL: &lt; 10 FIT</li> </ul>	<ul style="list-style-type: none"> <li>SER: &lt; 1000 FIT</li> <li>SEL: &lt; 10 FIT</li> </ul>