RapidIO™ General FAQ

RapidIO Interconnect Architecture & Trade Association

Q: What is the RapidIO interconnect architecture?

A: The RapidIO interconnect architecture is a new electronic data communication standard for interconnecting chips on a circuit board and for interconnecting circuit boards using a backplane.

The RapidIO standard increases bandwidth, lowers cost, and provides for a faster time to market for future networking products.

Q: What is the RapidIO Trade Association?

A: The RapidIO Trade Association will be a 501(c)6 nonprofit organization, which will direct community development and promote wide adoption of the new RapidIO interconnect technology as an open standard.

Q: What is the RapidIO interconnect target market?

A: The RapidIO interconnect is primarily targeted at the networking market. Unlike other contemporary computer-centric interconnects, the RapidIO technology addresses the networking industry's needs for software transparency, greater reliability, and higher bandwidth in an "in-the-box interconnect." The RapidIO interconnect provides higher bus speeds that allow chip-to-chip and board-to-board communications at performance levels scaling greater than ten gigabits per second.

Additionally, the RapidIO interconnect architecture is well suited to address the needs of other high performance embedded applications such as storage, multimedia, and signal processing.

Q: How is software development impacted by the RapidIO technology?

A: Software development is independent of the RapidIO interconnect architecture. RapidIO technology is transparent to the existing software base. To software, the RapidIO interconnect can look just like a traditional microprocessor and peripheral bus. RapidIO technology also bridges easily to PCI and PCI-X. These features allow users to mix legacy software and PCI chips with RapidIO chips.

Q: How is the RapidIO technology uniquely optimized?

A: RapidIO technology provides a rich set of hardware features for high availability and configuration. One such example is the ability to detect and recover from transmission errors.

In its simplest form, a RapidIO end-point can fit inside an FPGA. RapidIO end-points are small enough to leave most of the FPGA available for other functionality.

RapidIO technology is flexible, allowing a number of system topologies, address maps, and transactions to suit a variety of applications.

RapidIO implementations can boast high throughput, deterministically low latency, low cost, and low power. Designers can add multiple RapidIO ports to new I/O chips, providing the performance benefits of a fabric interconnect without incurring the costs associated with adding a dedicated switching chip.

Q: Where will I find the RapidIO interconnect architecture?

A: Integrated directly onto future microprocessors, digital signal processors, network processors, and communications processors. You will also find RapidIO technology used inside PCI-X and PCI fabrics. In more technical terms, the RapidIO technology is a high-performance, packet-switched, in-the-box interconnect.

Q: What does the RapidIO interconnect architecture look like?

A: RapidIO technology is a packet-switched protocol implemented on standard printed circuit board technology. Different parts of a RapidIO fabric can run at different rates. Thus, RapidIO interconnects have the potential to evolve over time to support other segments of the embedded market.

The first version of the RapidIO specification requires 40 pins per port. Each port has a data path that is 8-bits wide and is full duplex. The physical signaling is standard Low Voltage Differential Signaling (LVDS) operating at 250 MHz or higher. Data is transferred with a source synchronous clock and sampled on both clock edges. The total bandwidth per port is ten gigabits per second or higher. The draft RapidIO specifications also describe a different version of the RapidIO specification that is both twice as wide and twice as fast (a total bandwidth of forty gigabits per second per port).

To software, RapidIO interconnects look like a traditional microprocessor and peripheral bus, so hardware implementations can hide things like discovery and error management from software, unless a software system elects to participate. This is another example of the RapidIO technology's inherent compatibility with legacy system and application software.

The RapidIO interconnect architecture also boasts an optional distributed globally shared memory protocol extension that is useful for symmetric multiprocessing and shared data structures.

In its simplest form, a RapidIO end-point easily fits into an FPGA, with plenty of room left over for application-specific logic.

Q: Why create a RapidIO Trade Association?

A: The new association will direct future development and promotion of the new interconnect as an open standard, welcoming and encouraging networking market participants to join and thereby participate in the future of the RapidIO interconnect standard.

The RapidIO architecture's community-oriented development process will produce a true open standard.

Q: Who are the founders of the RapidIO Trade Association?

A: The companies who have communicated intent as of February 29, 2000 to join the RapidIO Trade Association are (in alphabetical order):

- Cisco Systems
- Galileo Technology
- HAL Computer Systems, Inc.
- Lucent Technologies
- Mercury Computer Systems
- Motorola, Inc.
- Nortel Networks
- Seagull Semiconductor, Ltd.
- Tundra Semiconductor Corp.
- Xilinx, Inc.

Q: Where can I find the latest information on the RapidIO Trade Association and RapidIO interconnect architecture?

A: Visit the RapidIO Trade Association's web site at www.RapidIO.org.