## PowerPC® Processors

At-a-Clance


## Overview

During these tight times-when competition is more intense and sales dollars are fewer-our customers are focused on protecting software investments, lowering development costs and delivering higher value solutions. This at-a-glance guide to PowerPC® ${ }^{\circledR}$ processors is designed to give you the information you need to make the right choices about processors. This guide includes key features, roadmaps, benchmarks, software/hardware tools support and URLs to help you find more information on our Web sites.

Motorola's G4 processors are ideal solutions for the networking infrastructure, telecom and embedded markets. In the first quarter of 2002, Motorola's G4 MPC7455 was recognized by In-Stat/MDR as the High-Performance Embedded Processor of 2001. This prestigious award was the result of Motorola's strong G4 family roadmap and consistent performance delivery over the past three years: $7400-400 \mathrm{MHz}$ (Aug. 1999), $7410-533 \mathrm{MHz}$ (March 2000), 7451-667 MHz (Jan. 2001), the 7455-1 GHz (Jan. 2002) and the 7457-1.3 GHz (Feb. 2003).

In spite of all of this acclaim, Freescale is not relaxing our commitment to this family; in fact, we will continue to deliver new G4 solutions-the MPC7457, for example, which delivers 1 GHz at less than 10 watts will be offered next year.

MOTOROLA'S HIGH-PERFORMANCE EMBEDDED MICROPROCESSOR PRODUCTS


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## Features and Benefits

The following information focuses on the benefits of Motorola's PowerPC G4 architecture,
such as its support for system upgrades, its performance enhancement beyond 60x bus
mode, and how it compares, feature by feature, to IBM's 750CXe and 750FX products.

SUPPORT FOR SYSTEM UPGRADE

## BENEFITS

1. Pin-Compatible
2. SoftwareCompatible
3. Power Savings
4. Performance

Improvement


## FREESCALE: THE LEADER IN COMMUNICATIONS PROCESSORS

- Proven platform in networking and embedded applications with more than 100 million processors shipped
- >300 customers; >4000 design wins
- 70\% market share (Source: Cahners In-Stat)
- Long-term support for our Smart Networks

Platform solutions

- 10 years of support for $6 x x / 7 x x$ product families
- 10+ years of support for communications processors
- Best-in-class tools support
- With Smart Networks partners, largest variety of development tools
- Reference design support with Sandpoint, MVP and Excimer systems
- Dedicated resources that have developed and improved the architecture for many years
- Pin-for-pin compatible products for three generations of process technologies providing ever improving performance and power


## POWERPC G4 ARCHITECTURE: DELIVERING PERFORMANCE ENHANCEMENT BEYOND 60X BUS MODE

- Address and data bus streaming for reduced cycle latency
- 60x bus requires a dead cycle between back-to-back address tenures or data tenures.
- MPX bus supports both "address streaming" and "data streaming": A master may drive consecutive address tenures or consecutive burst data tenures without a dead cycle in between.
- Data intervention for fewer memory accesses
- Snoop Hit Scenario: Processor "A" performs a read operation; The target data is modified in Processor "B's" cache.
- 60x bus-Write to main memory and read from main memory: " $B$ " responds with a retry and pushes the data to memory; "A" repeats the read request and loads the data from memory.
- MPX bus—Single fast write on the bus: "B" asserts the data ready signal and uses a data-only transaction to supply the data directly to "A."
- Out-of-order transactions
- 60x bus: Data tenures must occur in the same order as the associated address tenures.
- MPX bus: When a processor receives data out-of-order, the processor uses an index value (driven with the data) to associate the data on the bus with a previous address tenure.
- Out-of-order transactions may hide the latency of a slow memory or peripheral access.


## PowerPC ${ }^{\circledR}$ Processors

| FREESCALE |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 7410 | 7441 | 7445* | 7447* | 7451 | 7455* | 7457* |
| CPU Speed (MHz) | 400-550 | 600-700 | 733-1000 | 733-1300 | 533-667 | 733-1000 | 733-1300 |
| Bus Speed (MHz) | 133 | 133 | 150/166 | 166/200 | 133 | 150/166 | 166/200 |
| MPX Bus Support | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| L2 Cache (KB) |  | 256 | 256 | 512 | 256 | 256 | 512 |
| Backside Cache Support (MB) | 1 or 2 | N/A | N/A | N/A | 1 or 2 | 1 or 2 | 1,2 or 4 |
| Process | $0.18 \mu 6 \mathrm{LM}$ | $0.18 \mu 6 \mathrm{LM}$ | $\begin{aligned} & 0.18 \mu \mathrm{LLM} \\ & \text { SOI } \end{aligned}$ | $\begin{gathered} 0.13 \mu \text { 9LM } \\ \text { SOI } \end{gathered}$ | $0.18 \mu 6 \mathrm{LM}$ | $\begin{gathered} 0.18 \mu \mathrm{LLM} \\ \text { SOI } \end{gathered}$ | $\begin{gathered} 0.13 \mu \mathrm{BLM} \\ \text { SOII } \end{gathered}$ |
| Pipeline | 4 stage | 7 stage | 7 stage | 7 stage | 7 stage | 7 stage | 7 stage |
| SPECint95 (est.) | $\begin{gathered} 22.8 @ \\ 500 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 32.1 @ \\ 733 \mathrm{MHz} \end{gathered}$ |
| SPECfp95 (est.) | $\begin{gathered} 17 @ \\ 500 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ | $\begin{gathered} 23.9 @ \\ 733 \mathrm{MHz} \end{gathered}$ |
| Other <br> Performance | 1210 MIPS <br> @ 500 MHz | 1617 MIPS <br> @ 700 MHz | 1848 MIPS <br> @ 800 MHz | 1848 MIPS <br> @ 800 MHz | 1617 MIPS <br> @ 700 MHz | 2310 MIPS <br> @ 1 GHz | 2310 MIPS <br> @ 1 GHz |
| Dhrystone MIPS/MHz | 2.42 | 2.31 | 2.31 | 2.31 | 2.31 | 2.31 | 2.31 |
| Address and Data Bus Streaming | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Data Intervention Support | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Out-of-Order Transaction | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| AltiVec ${ }^{\text {TM }}$ Support | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| SMP Support | MESI | MESI | MESI | MESI | MESI | MESI | MESI |
| Instructions/Clock | 3 (2+branch) | 4 (3+branch) | 4 (3+branch) | 4 (3+branch) | 4 (3+branch) | 4 (3+branch) | 4 (3+branch) |
| Typical Power Consumption | 5.3W @ 500 MHz | 11.5W @ 600 MHz | 11.2W @ 800 MHz | 6.5W @ 900 MHz | 11.7W @ 600 MHz | 11.2W @ 800 MHz | $\begin{gathered} 7.5 \mathrm{~W} @ \\ 1 \mathrm{GHz} \text { (est.) } \end{gathered}$ |

# Freescale and Third-Party Tools <br> Support for G4 Family 

Along with our Smart Networks Alliance members, Freescale provides extensive, best-in-class tools to assist customers in their system design process. The chart below displays the extensive support available for the G4 family from both third-party vendors and Freescale. Tool support includes embedded OSes, compilers, debuggers, coverification tools, emulators, chipsets and more. For more information about tools, visit www.freescale.com

## G4 THIRD-PARTY SUPPORT

| Third-Party Vendor | Embedded Operating Systems | Compilers and Code Generation Tools | Software Debuggers | Coverification <br> Tools and <br> Simulation <br> Models | Emulators and Diagnostic Tools | Logic Anayzers | Reference and Evaluation Boards | $\begin{aligned} & \text { Support } \\ & \text { Chips } \end{aligned}$ | Chipsets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Abaton |  |  |  |  | - |  |  |  |  |
| Acilent Tectnologies |  |  |  |  | - | - |  |  |  |
| Applied Microsslstems |  |  | - |  | - |  |  |  |  |
| Apogee Sofivare |  | - |  |  |  |  |  |  |  |
| Arris Microssstems |  |  |  |  |  |  | - |  |  |
| Corelis |  |  | - |  | - |  |  |  |  |
| Green Hills Sofiware | . | - | . |  | - |  |  |  |  |
| Inoveda |  |  |  | - |  |  |  |  |  |
| Kadak | - |  | - |  |  |  |  |  |  |
| Lineo | - |  | - |  |  |  |  |  |  |
| LymuWorks | . | - | . |  |  |  |  |  |  |
| Macraigor Systems |  |  | - |  | - |  |  |  |  |
| Mavell Technologr |  |  |  |  |  |  | - | - | - |
| Mentor Graphics |  |  |  | - |  |  |  |  |  |
| MetaWare |  | - | - |  |  |  |  |  |  |
| Metrowerks |  | - | - |  |  |  |  |  |  |
| MirroAPL |  | - |  |  |  |  |  |  |  |
| MontaVista Sofiware | - |  | - |  |  |  |  |  |  |
| Fressale |  |  |  | - |  |  | - . |  |  |
| Freescale Computer Group |  |  |  |  |  | - |  |  |  |
| MPl Soitware Technology |  | . | . |  |  |  |  |  |  |
| OSE Systems | - |  | - |  |  |  |  |  |  |
| Pacifi-Sierra Research |  | - |  |  |  |  |  |  |  |
| PLXTecthology |  |  |  |  |  |  | - | - | - |
| Precise Software Technologies | - |  | - |  |  |  |  |  |  |
| OnX Sotiware Systems | - | - | - |  |  |  |  |  |  |
| Red Hat | $\bigcirc$ | $\div$ | $\div$ |  |  |  |  |  |  |
| RedSwitch |  |  |  |  |  |  |  |  | - |
| Simpod |  |  |  | - |  |  |  |  |  |
| Sun Microssstems | - | - | - |  |  |  |  |  |  |
| Symopss |  |  |  | $\bigcirc$ |  |  |  |  |  |
| Tekkonix |  |  |  |  |  | - |  |  |  |
| Tundia Semiconductor |  |  |  |  |  |  |  | - |  |
| Wasabi Systems | - | - | - |  |  |  |  |  |  |
| Wind River SVyt | . | . | . |  | . |  | . |  |  |

For More Information On This Product, Go to: www.freescale.com

## G4 Family Parametrics

Use the following charts to find facts, features and parametric data about the members of the MPC74xx (G4) family.

| CHECK APPROPRIATE |  |  |  |
| :---: | :---: | :---: | :---: |
| - H/W Specifications <br> - Part Number Specifications |  |  |  |
|  | Freq | Vcore | Tj |
| P | Fastest | Highest | $65^{\circ} \mathrm{C}$ |
| L | Faster | High | $105^{\circ} \mathrm{C}$ |
|  | Fast | Low | $105^{\circ} \mathrm{C}$ |

MPC7410

- 360 BGA
- 4-stage execution pipe
- Backside bus
- 2M L2/private memory
- 133 MHz MPX/60x bus

MPC7441

- 360 BGA
- No backside bus

THE MPC7445 ADDS:

- Address parity on L2
- 150/166 MHz 60x/MPX*
- 8 I-BAT and 8 D-BAT

THE MPC7447 ADDS:

- 512 KB on-chip L2
- 166/200 MHz 60x/MPX


| DEVICE | DATE | OPER. SPEC | VOLTAGE |  |  | $\frac{\text { FREQ }}{\mathrm{MHz}}$ | $\begin{aligned} & \mathrm{BUS} \\ & \hline \mathrm{MHz} \end{aligned}$ | $\frac{\text { POWER }}{W}$ | DOCUMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Core | Bus | BSB |  |  |  |  |
| XPC7451 | Now <br> Now | L | 1.6 | 2.5/1.8 | 2.5/1.8/1.5 | $\begin{aligned} & 667 \\ & 600 \end{aligned}$ | $\begin{aligned} & 133 \\ & 133 \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 11.7 \end{aligned}$ | MPC7451EC/D <br> Rev. 0.1, 11/01 |
| XPC7441 | Now <br> Now | N | 1.5 | 2.5/1.8 | N/A | $\begin{aligned} & 700 \\ & 600 \end{aligned}$ | $\begin{aligned} & 133 \\ & 133 \end{aligned}$ | $\begin{aligned} & 13.4 \\ & 11.5 \end{aligned}$ | MPC7441EC/D <br> Rev. 0, 10/01 |
| XPC7445/55 | Now Now | L | 1.6 | 2.5/1.8 | 2.5/1.8/1.5 | $\begin{aligned} & 933 \\ & 867 \\ & 800 \end{aligned}$ | $\begin{aligned} & 150 / 166^{*} \\ & 150 / 166^{*} \\ & 150 / 166^{*} \end{aligned}$ | $\begin{array}{r} 19.9 \\ 18.5 \\ 9.4 \end{array}$ | MPC7455EC/D <br> Feb 02 |
| XPC7445/55 | Now | N | 1.3 | 2.5/1.8 | 2.5/1.8/1.5 | 733 | 150/166* | 9.7 |  |
| XPC7445/55 | Now |  | 1.3 | 2.5/1.8 | 2.5/1.8/1.5 | 600 | 150/166* | 8.0 |  |
| XC7445/55 <br> (Node 5) <br> (Rev 3.3) | $\begin{aligned} & \text { Oct }(S) \\ & \operatorname{Dec}(P) \end{aligned}$ | L | 1.3 | 2.5/1.8 | 2.5/1.8/1.5 | $\begin{aligned} & 1067 \\ & 933 \\ & 867 \\ & 800 \\ & 733 \\ & 600 \end{aligned}$ | $\begin{aligned} & \hline 150 / 166^{*} \\ & 150 / 166^{*} \\ & 150 / 166^{*} \\ & 150 / 166^{*} \\ & 150 / 166^{*} \\ & 150 / 166^{*} \end{aligned}$ | $\begin{array}{r} 15.0 \\ 13.0 \\ 12.2 \\ 11.2 \\ 10.3 \\ 8.4 \end{array}$ | Review hardware specifications for final numbers. |
| XPC7447/57 | $\begin{aligned} & 20-03 \\ & 20-03 \end{aligned}$ | L | 1.3 | 2.5/1.8 | 2.5/1.8/1.5 | $\begin{aligned} & 1300 \\ & 1200 \end{aligned}$ | $\begin{aligned} & 166 / 200 \\ & 166 / 200 \end{aligned}$ | $\begin{aligned} & 16.6 \\ & 15.4 \end{aligned}$ | TBD |
| XPC7447/57 | $\begin{aligned} & 20-03 \\ & 20-03 \\ & 20-03 \end{aligned}$ | N | 1.0 | 2.5/1.8 | 2.5/1.8/1.5 | $\begin{aligned} & \hline 1067 \\ & 933 \\ & 867 \end{aligned}$ | $\begin{aligned} & 166 / 200 \\ & 166 / 200 \\ & 166 / 200 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 6.5 \\ & 6.1 \end{aligned}$ | TBD |
| * Initial product offered at 133 MHz |  |  |  |  |  |  |  |  |  |

## Benchmarking Data

EEMBC ${ }^{\circledR}$ RESULTS: NETWORKING—PRODUCTION SILICON


MPC7455 at $1 \mathrm{GHz} / 133$ is $3.4 x$ published NEC VR5500 score at $400 / 100 \mathrm{MHz}$.

For More Information
Customer URL: www.freescale.com
Additional Tech Questions: www.freescale.com

www.eembc.org

www.ebenchmarks.com

The EEMBC Certification Laboratories, LLC (ECL) has certified these scores according to the rules established by the EEMBC Board of Directors and ECL. These scores are repeatable and the disclosure information on the EEMBC Web site has all been verified. EEMBC is a registered trademark of the Embedded Microprocessor Benchmark Consortium.


[^0]:    Except for historical information, all of the expectations and assumptions contained in the foregoing are forward-looking statements involving risk and uncertainties. Important factors that could cause actual results to differ materially from such forward-looking statements include, but are not limited to, the competitive environment for our products, changes of rates of all related services and legislation that may affect the industry. For additional information regarding these and other risks associated with Company's business, refer to the Company's reports with the SEC.

