

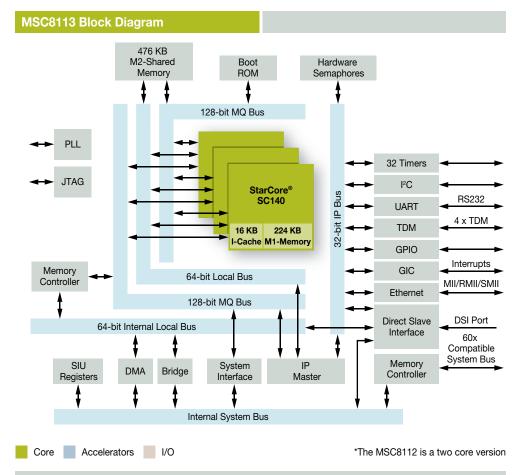


## MSC8112 and MSC8113

# The High-Performance DSP with Ethernet

Taking full advantage of the scalable StarCore® architecture, the MSC8112 and MSC8113 offer a DSP farm-on-a-chip level of performance integration. These highly integrated System-on-Chip (SoC) devices enable developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability and upgradability. As a two- and three-core version of MSC8122, the successful quad-core "work horse" DSP, the MSC8112 and MSC8113 deliver the same high level of integration along with a seamless, pin-compatible transition for mid-to-low performance designs. Both chips are well suited for computation-intensive infrastructure DSP applications such as including packet telephony media gateways, multi-channel modem banks and third-generation wireless systems. For systems supporting the true convergence of circuit-switched voice, fax, modem and packet-based protocols, the MSC8112 and MSC8113 multicore DSPs are an ideal fit. Aimed at delivering competitive channel density and scalable, low-power and cost-optimized design, the MSC8112 is offered at core speed levels of 300 MHz and the MSC8113 is offered at 300 MHz/400 MHz.

With two DSP extended cores, the MS8112 can deliver up to 2400 MMACS at 300 MHz, yielding an effective performance equal to 600 MHz. The three-core MSC8113 can deliver up to 4800 MMACS at 400 MHz, yielding an effective performance equal to 1.2 GHZ. The MSC8112 and MSC8113 comprise four time



division multiplexing (TDM) serial interfaces, 32 general-purpose timers, a flexible system interface unit (SIU), a fully featured multichannel DMA controller, a sophisticated multilevel memory hierarchy with large on-chip SRAM, a high-speed Ethernet interface for different types of external memories, and high-speed host port and serial communication interfaces.

## Why Ethernet?

Ethernet has become the de facto costeffective, pervasive packet network interface
between the DSP array, host processors and
the network. The MII, RMII and SMII Ethernet
interfaces for the MSC8112 and MSC8113
provide direct access to packet networks
and use a low pin count, providing a glueless
interface to onboard Ethernet switches and
PHYs that enables scalable, distributed,
uncomplicated and cost-effective board
architecture.





MSC8112 and MSC8113—A Comparison		
Features	MSC8112	MSC8113
Core voltage	1.1V ± -0.5V (300 MHz)	$1.1V \pm -0.5V$ (300 MHz/400 MHz)
Target operating frequency	300 MHz	300 MHz and 400 MHz

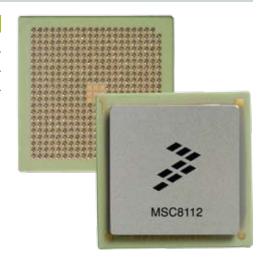
#### **Features**

- MSC8112: Two 300 MHz SC140 extended cores
- MSC8113: Three 300 MHz/400 MHz sc140 extended cores
- 224 KB of dedicated M1 memory for each extended core
- 16 KB, 16-way instruction cache in each extended core
- 476 KB of shared M2 memory between all extended cores
- 4 KB bootstrap ROM
- Ethernet interface designed to comply with IEEE® Std. 802.3, Std. 802.3u, Std. 802.3x and Std. 802.3ac
- · Configurable dual bus architecture
- 32- or 64-bit industry-standard external 60x-compatible bus interface at up to 166 MHz
- 32- or 64-bit, high-performance, direct slave interface
- 476 KB of shared M2, four independent time division multiplexing interfaces (256 channels each)
- Flexible memory controller for various external memory types

- 16-channel DMA engine that facilitates independent data transfers
- 32 16-bit timers with watchdog mode support
- 1.1V extended core; 3.3V I/O
- 0.8 mm pitch 20 mm x 20 mm Flip-Chip Plastic Ball-Grid Array (FC-PBGA)
- I<sup>2</sup>C port compatible with I<sup>2</sup>C bus standard and widespread I<sup>2</sup>C serial EEPROM access protocol

#### **Benefits**

- MSC8112: 2400 MMACS of DSP performance capability
- MSC8113: up to 4800 MMACS of DSP performance capability
- Ethernet interface that provides direct access to internal memories
- · Excellent channel and power density ratio
- Code-compatible with the existing MSC8102, MSC8101, MSC8103 and MSC8122
- Pin-compatible with the MSC8122
- C programming that helps speed time to market
- High code density that results in low system costs



### **Software Development Tools**

- Tools integrated in an integrated development environment
- Real-time debug capability for each extended core
- Optimized C compiler generates efficient control and DSP code
- Real-time operating system that fully supports device architecture (multicore, memory, hierarchy, I-Cache, timers, DMA, interrupts, peripherals)

Learn More:

For current information about Freescale products and documentation, please visit **www.freescale.com**.

