Datapath Switch

Errata to
XC92501 ATM Cell Processor

This document describes errata of the XC92501 ATM Cell Processor and its related versions:

- XC92501GC, August, 1998
- XC92501GCA, Rev. A, September, 1999

1.1 Summary Table

Table 1-1 provides a summary ofXC92501 errata.

Table 1-1Summary of XC92501 Errata

Errata #	Problem	Impact	Work Around	Silicon Revisions Affected	
				GC	GCA
1	The MDC bit of the MPCONR register cannot be read.	The MDC bit cannot be read.	MPCONR(MDC) can be written and the XC92501 cell processor will function according to the specification.	✔	✔

Table 1-1Summary of XC92501 Errata

Errata #	Problem	Impact	Work Around	Silicon Revisions Affected	
				GC	GCA
2	The per-connection and per-link ingress billing counters do not count when egress UPC is set.	Cells are not counted at ingress.	None	✔	✔
3	An ingress cell is removed during egress UPC.	Cells are lost at ingress.	None	✔	✔
4	The JTAG boundary scan register bit definition is updated.	The backward compatibility of the 92501 to the 92500 is marginally reduced.	None	✔	✔
5	I/O pins are not 5V tolerant		As a workaround Motorola recommends using buffers which are 5V tolerant and whose output is 3V for driving the RXPHYID(0->3) signals.	✔	

1.2 Errata Details

Following are the details of the errata that apply to the XC92501 ATM Cell Processor:

Errata #1: The MPCONR(MPC) bit cannot be read

Description: Even when a new value has been placed in the MDC bit of the MPCONR register it cannot be read.

Projected Impact: The MDC bit cannot be read.

Solution: A fix is planned for the XC92501.

Work Around: The MPCONR(MDC) bit can be written, however, and the XC92501 cell processor will function according to the specification.

Errata Applies To: XC92501GC,

XC92501GCA

Errata #2: Billing counters do not count

Description: When the egress UPC is set, the per-connection and per-link ingress billing counters do not count.

Projected Impact: Cells are not counted at ingress.

Solution: A fix is planned for the XC92501.

Work Around: None

Errata Applies To: XC92501GC,

XC92501GCA

Errata #3: Removal of an ingress cell during egress UPC

Description: In egress UPC mode, when an egress cell is removed because it does not conform to UPC, one cell slot later an ingress cell is removed.

Projected Impact: Cells are lost from the ingress cell flow.

Solution: The XC92501 will be fixed in the next revision.

Work Around: None

Errata Applies To: XC92501GC,

XC92501GCA

Errata #4: JTAG boundary scan register bit definition is updated

Description: Because the XC92501 contains some additional signals that the MC92500 does not have, the JTAG boundary scan register bit definition of the XC92501 is updated, is changed from the MC92500.

Projected Impact: The backward compatibility of the 92501 to the 92500 is marginally reduced.

Solution: A fix is planned for the XC92501.

Work Around: None

Errata Applies To: XC92501GC,

XC92501GCA

Errata #5: I/O pins are not 5V tolerant

Description: The RXPHYID(0->3) pins of the 92501 are not 5V tolerant.

Projected Impact:

Solution: This errata will be fixed in the next version of the processor.

Work Around: As a workaround Motorola recommends using buffers which are 5V tolerant and whose output is 3V for driving the RXPHYID(0->3) signals.

Errata Applies To: XC92501GC,

1.3 Revision History

Table 1-2 contains a brief description of the technical updates made to this document.

Table 1-2Revision History Table

Date	Document Revision	Substantive Changes
14 October, 1999	Rev 1.1	Errata 1, 2, and 4: Changed “No fix is planned for the MC92501” to “A fix is planned for the MC92501.”
15 December, 1999	Rev 1.2	Changed all occurences of MC92501 to XC92501 to reflect the true name of the silicon. Added the word “Silicon” to “Revisions Affected” in Table 1.

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