Freescale Semiconductor
Mask Set Errata

PXR40_3M17W
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Mask Set Errata for Mask 3M17W

Introduction

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- PXR40

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e3521: DECFIL: Soft reset failures at the end of filtering

Errata type: Errata

Description: If a software reset of a decimation filter is made exactly at the time it finishes filtering, several registers reset for one clock, but have their values updated by the filtering on the next clock,

including (but not limited to) the integrator current value register DECFIL_CINTVAL and

the tap registers DECFILTER_TAPn.

Workaround: Before making the soft reset write (DECFIL_MCR bit SRES=1), perform the procedure below:

1- disable filter inputs, writing DECFIL_MCR bit IDIS = 1.

2- read the register DECFIL_MSR and repeat the read until the bit BSY is 0.

3- repeat the loop of step 2; this is necessary to cover the case when a sample is left in the input buffer.

e818: EMIOS/ETPU: Global timebases not synchronized

Errata type: Errata

Description: The eTPU and eMIOS timebases can be started synchronously by asserting the Global Time Base Enable (GTBE) bit in either the eTPU Module Configuration Register (eTPUMCR) or the eMIOS Module Configuration Register (eMIOS_MCR). GTBE bits from the eMIOS and eTPU are ORed together such that asserting either of them allows both eMIOS and eTPU timebases to start running simultaneously.

When the timebases are running and GTBE is cleared, the timebase and eTPU Angle Counter (EAC) prescalers can stop at any count. When GTBE is reasserted, the prescalers must have a determined initialization value so that the timebases will remain in sync with each other.

Workaround: Perform the following steps in sequence to synchronize the time base between the eTPU and the eMIOS:

1- Clear the Global Time Base Enable (GTBE) bit in the eTPU Module Configuration Register (ETPUMCR[GTBE] = 0).

2- Clear the Global Time Base Enable (GTBE) and Global Prescaler Enable (GPREN) bits in the eMIOS Module Configuration Register (EMIOS_MCR[GTBE] = 0, EMIOS_MCR[GPREN] = 0) to stop the Global Clock Prescaler (GCP) from counting.

3- Write the desired counter values to the eTPU Time Counter Registers 1 and 2 (TCR1 and TCR2) with eTPU microcode (these registers cannot be written by the CPU). This step is required even if the values in TCR1 and TCR2 are not changed.

4- Clear the Unified Channel Prescaler Enable (UCPREN) bit in the eMIOS Channel Control Register (EMIOS_CCRn) for each of the eMIOS channels (EMIOS_CCRn[UCPREN] = 0).

5- If it is necessary to set the eMIOS counters to known values, configure each eMIOS channel for General Purpose Input (GPI) mode (EMIOS_CCRn[MODE] = 0000000), write the desired counter values, and restore the desired operational mode (EMIOS_CCRn[MODE] = xxxxxxx).

6- Set the UCPREN bit in the EMIOS_CCRn register for each of the eMIOS channels (EMIOS_CCRn[UCPREN] = 1) to re-enable the unified channel prescaler.

7- Set the GTBE and GPREN bits in the eMIOS MCR simultaneously with a single write operation(EMIOS_MCR = EMIOS_MCR | 0x14000000).

Note: This works only for eTPU and single eMIOS module synchronization. For more than one eMIOS module there is no workaround, since their GPREN bits cannot be written at the same time.

e3378: EQADC: Pull devices on differential pins may be enabled for a short period of time during and just after POR

Errata type: Errata

Description: The programmable pull devices (up and down) on the analog differential inputs of the eQADC may randomly be enabled during the internal Power On Reset (POR) and until the 1st clock edge propagates through the device. After the first clock edge, the pull resistors will be disabled until software enables them.

Workaround: Protect any external devices connected to the differential analog inputs. The worst case condition is with a 1.4K ohm resistor to VDDA (5K pull-up enabled) or VSSA (5K pull-down enabled). This may also cause temporary additional current requirements on the VDDA supply of each eQADC module, up to 15 mA on each eQADC if both the pull up and pull down resistors are enabled simultaneously on all of the differential analog pins.

e2382: FLASH: Flash Array Integrity Check

Errata type: Errata

Description: The Flash Array Integrity Check (AIC) which may be enabled during the flash user test (UTest) mode does not return the expected UMn[MISR] values for some flash PFCRPn[RWSC] read wait state configurations. For PFCRPn[RWSC] values of 3-6, the UMn[MISR] signature computation during AIC does not include the data read from the very last address in the selected address sequence and thus the UMn[MISR] value is not as expected. For PFCRPn[RWSC] values of 7, the UMn[MISR] signature computation during AIC will not be correct as well.

Workaround: The Flash Array Integrity Check is correct for PFCRPn[RWSC] values of 0-2. For PFCRPn[RWSC] values of 3-6, the expected UMn[MISR] values will not include the data read from the very last address and thus the value expected should be for the data read up to the 2nd-last address in the selected address sequence. For a PFCRPn[RWSC] value of 7, the Array Integrity Check should not be used at all.

e1312: FLASH: MCR[DONE] bit may be set before high voltage operation completes when executing a suspend sequence

Errata type: Errata

Description: The program and erase sequence of the flash may be suspended to allow read and program access to the flash core. An suspend operation is initiated by setting the Erase Suspend (ESUS) bit or Program Suspend (PSUS) bit in the flash Module Configuration Register (MCR). Setting a suspend bit causes the flash module to start the sequence which places it in the suspended state. The user must then wait until the MCR[DONE] bit is set before a read or program to the flash is initiated, as the high voltage operation needs to be complete to avoid errors.

However, during normal read to the same partition, following a suspend sequence, (setting MCR bit and waiting for MCR[DONE] bit to be set) can result in read fails that will return multiple bit ECC errors. The error is due to the MCR[DONE] bit being set before the internal high voltage operation is complete.

Workaround: Because the MCR[DONE] flag can be set too soon, a delay needs to be inserted between setting the MCR[ESUS] or MCR[PSUS] and reading the same flash partition. The minimum duration of the delay should be 40us to guarantee correct operation. The Freescale flash programming driver includes this workaround.

e3659: FLASH: Resuming after a suspend during an Erase may prevent the erase from completing.

Errata type: Errata

Description: If an erase suspend (including the flash put into sleep or disabled mode) is done on any block in the low Address Space (LAS) or the Mid-Address Space (MAS) except the 16KB blocks, or if a suspend is done with multiple non-adjacent blocks (including the High Address Space [HAS]), the flash state machine may not set the FLASH_MCR[DONE] bit in the flash Module Control Register. This condition only occurs if the suspend occurs during certain internal flash erase operations. The likelihood of an issue occurring is reduced by limiting the frequency of suspending the erase operation.

Workaround: If the suspend feature (including disable and sleep modes) of the flash is used, then software should ensure that if the maximum time allowed for an erase operation occurs without a valid completion flag from the flash (FLASH_MCR[DONE] = 1), the software should abort the erase operation (by first clearing the Enable High Voltage (FLASH_MCR[EHV]) bit, then clearing the Erase read/Write bit (FLASH_MCR[ERS] bit) and the erase operation should be restarted.

Note: The cycle count of the sector is increased by this abort and restart operation.

e2424: FlexCAN: switching CAN protocol interface (CPI) to system clock has very small chance of causing the CPI to enter an indeterminate state

Errata type: Errata

Description: The reset value for the clock source of the CAN protocol interface (CPI) is the oscillator clock. If the CPI clock source is switched to the system clock while the FlexCAN is not in freeze mode, then the CPI has a very small chance of entering an indeterminate state.

Workaround: Switch the clock source while the FlexCAN is in a halted state by setting HALT bit in the FlexCAN Module Configuration Register (CANx_MCR[HALT]=1). If the write to the CAN Control Register to change the clock source (CANx_CR[CLK_SRC]=1) is done in the same oscillator clock period as the write to CANx_MCR[HALT], then chance of the CPI entering an indeterminate state is extremely small. If those writes are done on different oscillator clock periods, then the corruption is impossible. Even if the writes happen back-to-back, as long as the system clock to oscillator clock frequency ratio is less than three, then the writes will happen on different oscillator clock periods.

e1364: FlexRay : Message Buffer Slot Status corrupted after system memory access timeout or illegal address access

Errata type: Errata

Description: If the system memory read access that retrieves the first message buffer header data from a FlexRay transmit buffer fails due to a system memory access timeout or illegal address access, it is possible that the slot status information for the previous slot is written into the currently used transmit message buffer. In this case, the slot status information is not written into the message buffer assigned to the last slot.

Thus, both the message buffer assigned to the last slot, and the currently used transmit message buffer contain incorrect slot status information.

However, if this occurs, either the System Bus Communication Failure Error Flag (SBCF_EF) or the Illegal System Bus Address Error Flag (ILSA_EF) will be set in the Controller Host Interface Error Flag Register (CHIERFR).

Workaround: The FlexRay module and the system memory subsystem should be configured to avoid the occurrence of system memory access timeouts and illegal address accesses.

In case that one of the error flags CHIERFR[SBCF_EF] or CHIERFR[ILSA_EF] is set, the application should not use the slot status information of the message buffers.

e1369: FlexRay : Message Buffer Status, Slot Status, and Data not updated after system memory access timeout or illegal address access

Errata type: Errata

Description: If a message buffer is assigned to the last slot in a FlexyRay communication cycle and a system memory access timeout or illegal address access occurs during the system memory access in this slot, it is possible that for all future communication 1) no slot status information will be written, 2) the message buffer status will not be updated, and 3) no message frames will be received. If this happens, several message buffers can never be locked by the application.

However, if this occurs, either the System Bus Communication Failure Error Flag (SBCF_EF) or the Illegal System Bus Address Error Flag (ILSA_EF) will be set in the Controller Host Interface Error Flag Register (CHIERFR).

Workaround: The FlexRay module and the system memory subsystem should be configured to avoid the occurrence of system memory access timeouts and illegal address accesses.

In case that one of the error flags CHIERFR[SBCF_EF] or CHIERFR[ILSA_EF] is set, the application should stop the FlexRay controller via a FREEZE or HALT command and subsequently restart the controller.

e2302: FlexRay: Message Buffer can not be disabled and not locked after CHI command FREEZE

Errata type: Errata

Description: If a complete message was transmitted from a transmit message buffer or received into a message buffer and the controller host interface (CHI) command FREEZE is issued by the application before the end of the current slot, then this message buffer can not be disabled and locked until the module has entered the protocol state normal active.

Consequently, this message buffer can not be disabled and locked by the application in the protocol config state, which prevents the application from clearing the commit bit CMT and the module from clearing the status bits. The configuration bits in the Message Buffer Configuration, Control, Status Registers (MBCCSRn) and the message buffer configuration registers MBCCFRn, MBFIDRn, and MBIDXRn are not affected.

At most one message buffer per channel is affected.

Workaround: There are two types of workaround.

1) The application should not send the CHI command FREEZE and use the CHI command HALT instead.

2) Before sending the CHI command FREEZE the application should repeatedly try to disable all message buffers until all message buffers are disabled. This maximum duration of this task is three static or three dynamic slots.

e3553: NXFR: Flexray databus translates into unexpected data format on the Nexus interface

Errata type: Errata

Description: The data format for Nexus Flexray messages is in little-endian (least significant byte first) order. This is not currently documented and may be unexpected for users of Power Architecture devices.

For example, in the case of a Flexray System Memory write within the address space determined by Data Trace Start and Data Trace End Addresses (DTSAx/DTEAx) with the data: 0x1122, the Flexray Nexus interface generates Data Trace Messages (DTM) containing the data: 0x2211.

Workaround: The user must be aware of the data format. This will be documented in a future release of the device reference manual.

e2696: PBRIDGE: Write buffer may cause overflow/underflow of DMA transfers

Errata type: Errata

Description: Peripheral-paced DMA transfers are controlled by a hardware handshake protocol: when the peripheral requires a data transfer, it asserts a request to the DMA. The DMA recognizes the request, activates the corresponding channel and performs the data transfer, reading from the source and writing to the destination. As the write is being processed, the DMA sends an acknowledge back to the peripheral so it can negate its request.

If buffered writes are enabled in the PBRIDGE, there are certain conditions where the DMA's acknowledge is asserted before the actual write operation to the peripheral has occurred. The net effect is the DMA request is not negated properly, causing the DMA to reactivate the channel, overwriting the last transferred data value before it is transferred to the peripheral.

Workaround: Do not enable buffered writes for the eDMA in the Peripheral Bridge Master Privilege Control registers (PBRIDGE_A_MPCR and PBRIDGE_B_MPCR), by leaving the MBW4 (eDMA A master) and MBW5 (eDMA B master) bits cleared. This is the default state of these bits, which disables buffered writes to the peripherals from both eDMA masters.

e2322: PMC: LVREH/LVREA/LVRE50 may exit LVI triggered reset with LVI condition still existing

Errata type: Information

Description: After asserting the Low Voltage Reset Enables PMC_CFGR[LVREH], PMC_CFGR[LVREA], PMC_CFGR[LVRE50] bits in the PMC, if the voltage ramps down below the LVI voltage on VDDEHx, VDDA or VDDREG respectively, the part will go to a short power on reset (POR). After the reset counter has expired, the device will go into normal operation, even though one or more of the affected supplies may still be below the specified LVI voltage.

Workaround: The part will recover into normal operation, however software should check the status of the LVIs for those segments that are required for further operation.

e3377: Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge

Errata type: Errata

Description: The Nexus Output pins (Message Data outputs 0:15 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance driver (when used as a general purpose input [GPI] in the application).

Workaround: 1. Do not tie the Nexus output pins directly to ground or a power supply.

2. If these pins are used as GPI, limit the current to the ability of the regulator supply to guarantee correct start up of the power supply. Each pin may draw upwards of 150mA.

If not used, the pins may be left unconnected.

e1419: SIU: Reverting ENGCLK source to the system clock has a very small chance of causing the ENGCLK generator to enter an indeterminate state

Errata type: Errata

Description: The reset value for the Engineering Clock (ENGCLK) source is the system clock. If the clock source is switched to the external clock (buffered crystal frequency or external clock input) by setting Engineering Clock Source Select bit in the External Clock Control Register (SIU_ECCR[ECSS]=1) and then reverted to the system clock, then the ENGCLK generator has a very small chance of entering an indeterminate state.

Workaround: Do not change the ENGCLK source back to the System clock after changing it to the external clock.

e4396: e200z7: Erroneous Address Fetch

Errata type: Errata

Description: Under certain conditions, if a static branch prediction and a dynamic return prediction (which uses the subroutine return address stack) occur simultaneously in the Branch Target Buffer (BTB), the e200z7 core can issue an errant fetch address to the memory system (instruction fetched from wrong address).

This can only happen when the static branch prediction is "taken" but the branch actually resolves to "not taken". If the branch resolves to taken, correct fetching occurs for this branch path and no issue is seen.

If Branch Unit Control and Status Register (BUCSR) Branch Prediction Control Static (BPRED) = 0b00, 0b01, or 0b10, then static branch prediction is configured as "taken". The issue can occur with these settings.

If BUSCR[BPRED] = 0b11, then static branch prediction is configured as "not taken". The issue does not occur with this setting.

The issue does not appear in applications compiled with VLE.

Workaround: To prevent the issue from occurring, confirgure static branch prediction to "not taken" by setting the Branch Unit Control and Status Register (BUCSR) Branch Prediction Control Static (BPRED) to 0b11.

For customers using VLE, there is no workaround required, the issue will not be seen.

e3419: e200z: Exceptions generated on speculative prefetch

Errata type: Errata

Description: The e200z7 core can prefetch up to 2 cache lines (64 bytes total) beyond the current instruction execution point. If a bus error occurs when reading any of these prefetch locations, the machine check exception will be taken. For example, executing code within the last 64 bytes of a memory region such as internal SRAM, may cause a bus error when the core pre-fetches past the end of memory. An ECC exception can occur if the core prefetches locations that are valid, but not yet initialized for ECC.

The Boot Assist Monitor (BAM) is located at the end of the address space and so may cause instruction pre-fetches to wrap-around to address 0 in internal flash memory. If this first block of flash memory contains ECC errors, such as from an aborted program or erase operation, a machine-check exception will be asserted. At this point in the boot procedure, exceptions are disabled, but the machine-check will remain pending and the exception vector will be taken if user application code subsequently enables the machine check interrupt.

Workaround: Do not place code to be executed within the last 64 bytes of a memory region. When executing code from internal ECC SRAM, initialize memory beyond the end of the code until the next 32-byte aligned address and then an additional 64 bytes to ensure that prefetches cannot land in uninitialized SRAM.

To guard against the possibility of the BAM causing a machine-check exception to be taken, as noted in the errata description, user application code should check and clear the Machine Check Syndrome Register (MCSR) in the core before enabling the machine check interrupt. This can be done by writing all 1s to MCSR.

e4480: eQADC: Differential conversions with 4x gain may halt command processing

Errata type: Errata

Description: If the four times amplifier is enabled for a differential analog-to-digital conversion in the Enhanced Queued Analog to Digital Converter (eQADC) and the ADC clock prescaler is set to divide by 12 or greater, then the ADC will stop processing commands if a conversion command is executed immediately after a differential, gain 4x conversion.

Workaround: 1) Do not use a prescaler divide factor greater than or equal to 12 (11 can be used on devices that support odd prescalers).

2) Insert a dummy write command to any internal ADC register after every 4x conversion command.

Note 1: If the command FIFO preemption feature is used and it is possible to preempt a FIFO which contains the 4x conversion + dummy write workaround, then the preempting command FIFO must be loaded FIRST with a dummy write command and then the desired preempting conversion command in order to avoid the possibility of following a 4x conversion command with another conversion command in the same ADC.

Note 2: The level sensitive triggers (when in Low/High Level Gated External Trigger, Single/Continuous Scan modes) can interrupt the command sequence at any point in time, potentially breaking the safe sequence 4x conversion command -> dummy write command.

Note 3: When using an odd prescaler (ADCx_CLK_ODD = 1), the duty cycle setting (ADCxCLK_DTY) must be kept at the default setting of 0.

e2386: eSCI : No LIN frame reception after leaving stop mode

Errata type: Errata

Description: When the eSCI module is in LIN mode and transmits or receives an LIN frame, if the CPU requests Stop Mode, and the Stop Mode is left, an subsequent triggered LIN RX Frame reception may hang. The module will never assert the eSCI_IFSR2[RXRDY] and eSCI_IFSR2[TXRDY] flags.

Workaround: The application should ensure that no LIN transmission is running before it requests Stop Mode by checking the status of the eSCI_IFSR1[TACT] and eSCI_IFSR1[RACT] status flags.

e1171: eSCI : DMA stalled after return from stop or doze mode

Errata type: Errata

Description: If the eSCI module enters stop or doze mode while the transmit DMA is enabled and messages are being transmitted, when the CPU exits stop or doze mode, it is possible that DMA requests will not be generated by the eSCI module.

Workaround: The application should ensure that the eSCI module is idle before entering the stop mode.

The eSCI module is idle when both transmitter and receiver active status bits in the Interrupt Flag and Status Register 1 (eSCI_IFSR1) are not set.

The application should not trigger a new transmission on the eSCI module if the application is preparing for the stop mode.

e2396: eSCI : Stop Mode not entered in LIN mode

Errata type: Errata

Description: When the eSCI module is in LIN mode and transmits the Header of an LIN RX frame, if the CPU requests Stop Mode, the eSCI module may not acknowledge the Stop Mode request and will stay in Normal Operating Mode (not in lower power stop mode).

Workaround: The application should ensure that no LIN transmission is running before it requests Stop Mode by checking the Transmit Active and Receive Active status bits in the eSCI Interrupt Flag and Status Register (eSCI_IFSR1[TACT] and eSCI_IFSR1[RACT]).

e1297: eSCI : reads of the SCI Data Register, which clears the RDRF flag, may cause loss of frame if read occurs during reception of the STOP bit

Errata type: Errata

Description: A received SCI frame is not written into the SCI Data Registers and the Overrun (OR) flag is not set in the SCI Status Register 1 (SCISR1), if:

1.) The eSCI has received the last data bit of an SCI frame n

2.) and the Receive Data Register Full (RDRF) flag is still set in the SCISR1 after the reception of SCI frame n-1

3.) and during the reception of the STOP bit of frame n the host reads the SCI Data Registers, and clears the RDRF flag

In this case the RDRF flag is erroneously set again by the controller instead of the OR flag. Thus, the host reads the data of frame n-1 a second time, and the data of frame n is lost.

Workaround: The application should ensure that the data of the foregoing frame is read out from the SCI Data Registers before the last data bit of the actual frame is received.

e1381: eSCI: LIN Wakeup flag set after aborted LIN frame transmission

Errata type: Errata

Description: If the eSCI module is transmitting a LIN frame and the application sets and clears the LIN Finite State Machine Resync bit in the LIN Control Register 1 (eSCI_LCR1[LRES]) to abort the transmission, the LIN Wakeup Receive Flag in the LIN Status Register may be set (LWAKE=1).

Workaround: If the application has triggered LIN Protocol Engine Reset via the eSCI_LCR1[LRES], it should wait for the duration of a frame and clear the eSCI_IFSR2[LWAKE] flag before waiting for a wakeup.

e1221: eSCI: LIN bit error indicated at start of transmission after LIN reset

Errata type: Errata

Description: If the eSCI module is in LIN mode and is transmitting a LIN frame, and the application sets and subsequently clears the LIN reset bit (LRES) in the LIN Control register 1 (ESCI_LCR1), the next LIN frame transmission might incorrectly signal the occurrence of bit errors (ESCI_IFSR1[BERR]) and frame error (ESCI_IFSR1[FE]), and the transmitted frame might be incorrect.

Workaround: There is no generic work around. The implementation of a suitable workaround is highly dependent on the application and a workaround may not be possible for all applications.

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