

Mask Set Errata

MSE9S08JM60\_0M36H Rev. 1, 4/2008

# Mask Set Errata for Mask 0M36H

## Introduction

This report applies to mask 0M36H for these products:

• MC9S08JM60

## MCU device mask set identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

# MCU device date codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

# MCU device part number prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

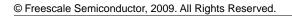
## SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type: Silic	con
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Affected component: ADC

Description:

If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction







is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

**Workaround:** It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

# SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type:	Silicon			
Affected component:	ADC			
Description:	In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.			
	In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.			
	In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.			
	The errata does not impact 8-bit operation.			
	Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock, and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.			
Workaround:	Using the device in 8-bit mode will eliminate the possibility of the errata occuring.			
	Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.			
	Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.			



## SE133-FLASH: Unexpected Flash Block Protection Errors

Errata type:	Silicon			
Affected component:	Flash			
Description:	flash block protect v occur during an atte that are not block p potential problem. T multiple nonvolatile	violation (FPVIO empt to program protected. Softwa The problem is m blocks, including	ry (NVM) is block protected, unexpected L) errors can result. These errors can or erase locations in areas of the NVM re methods can be used to avoid this ore likely to be seen on devices that have g devices with two or more separate flash f block protection is not enabled, no errors	
	to an internally latch reset, at the end of a location in NVM. If immediately before command, the error can cause a false in instructions can be	thed address. The most flash comm f a read access to the write to unp pheous address t ndication of a pro- performed before	mpares current block protection settings is internal address is written (latched) at mands, and whenever there is a write to o the partially protected NVM is performed rotected memory that starts a new flash hat was previously in the internal latch otection violation. A short sequence of re starting normal flash commands to nal latch is not a protected address.	
Workaround:	The preferred workaround starts a command to a known unprotected address (which internally latches the known-unprotected address), forces an access error to abort that command, and then clears the resulting error flags before starting any new flash command. This workaround assumes the H:X index register points to the location or sector you want to program or erase, and accumulator A has the data value you plan to write to that location. Start your program or erase routine with the following instructions.			
		NOP to start	protected address from H:X ;brief delay to allow the command	
	error to abort t		;intentionally cause an access	
		PSHA LDA #\$30	;temporarily save data value ;1's in PVIOL and ACCERR bit	
		STA FSTAT PULA	;clear any error flags ;restore data value	
		STA ,X	STEP 1 write data to start new	
	command			
	The only new instructions compared to the normal routine for flash commands			

The only new instructions compared to the normal routine for flash commands are the first three instructions, which take three bytes of code space and five bus cycles. These instructions may be located anywhere in memory, including in the protected area of the flash memory.



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