Silicon Errata for the MSC8101 Processor, Mask 1K87M

This document presents the errata for the 1K87M mask of the Freescale MSC8101 device. The errata are classified and numbered, and each erratum is provided with a description and workarounds. **Table 1** lists the mask numbers and the corresponding versions of the MSC8101 device.

Table 1. MSC8101 Mask Numbers and Revisions

MASK NUMBER	REVISION
0K40A	Rev0
1K42A	Rev0.1
2K42A	Rev0.2
1K87M	RevA
2K87M	RevA.2

Table 2. Silicon Errata

Errata Number	Errata Description	Applies to Mask
SIU13	**SDAMUX not Valid in Single-MSC8101 Mode** **Date Added:** 3/14/2002 **Description:** SDAMUX signal is disabled (stuck at'0')when SDRAM machine handles the memory access and the chip is programmed to single-MSC8101 mode (BCR[EBM]=0). **Workaround:** None. **System Number:** **Fix Plan:** TBD	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SIU16	**Bus Busy Disable Mode Can Hang 60X Bus in Multi-Master Systems** **Date Added:** 5/21/2002 **Description:** The bus busy disable mode (SIUMCR[BBD=1]) can not be used if the MSC8101 is not the only master on the 60X bus. Using this mode in such a system can cause the 60X bus to hang. **Workaround:** **1.** If the external master supports the $\overline{\text{ABB}}$ signal, do not use the bus busy disable mode and connect this signal to the MSC8101. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. **2.** If the external master does not support the $\overline{\text{ABB}}$ signal do one of the following: a. Do not use the bus busy disable mode and generate the $\overline{\text{ABB}}$ signal externally. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. The following external $\overline{\text{ABB}}$ implementation should be sufficient to work around the problem: Assert the $\overline{\text{ABB}}$ signal whenever a qualified bus grant for the external master is sampled (Bus grant asserted while $\overline{\text{ARTRY}}$ and $\overline{\text{ABB}}$ are negated). Negate the $\overline{\text{ABB}}$ signal when there is no qualified bus grant. The negation of $\overline{\text{ABB}}$ should be as follows: Drive $\overline{\text{ABB}}$ to VDD for half a clock cycle and then stop driving it (HIGH-Z). b. If using the internal arbiter and up to two external masters, connect the external bus grants (through an AND gate if more than one) to an available external bus request and define the priority for that request to be the highest in the PPC_ALRH register. The $\overline{\text{DBB}}$ signal can either be connected or can be pulled up. **Fix Plan:** TBD	1K87M
SIU18	**ARTRY Assertion When Using Pipeline Depth of Zero** **Date Added:** 10/15/2002 **Description:** Internal (60x) slave maintains a pipeline depth of zero by asserting AACK only after TA. When ARTRY is asserted the 60x bus access will be terminated and TA will not be asserted. Therefore the Internal (60x) slave will not assert AACK since TA was not asserted. **Workaround:** Use a pipeline depth of one (BCR[PLDP]=0) for applications that require memory coherency. **Fix Plan:** TBD	1K87M
SIU19	**Bus Monitor Timeout When Using External Slave** **Date Added:** 10/15/2002 **Description:** When using an external 60x bus slave with the bus monitor activated, PSDVAL is not asserted when the external slave is accessed, which could cause the bus monitor to time-out and TEA to be asserted. **Workaround:** The following workarounds **1.** Use pipeline depth of zero (BCR[PLDP]=1) when using an external 60x bus slave. **2.** Disable 60X bus monitor, SYPCR[PBME]=0. **3.** If the external 60x bus slave is another 810x or 826x device, connect the PSDVAL signals together. **Fix Plan:** TDB	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
QSIU4	**Extended Mode on the Local Bus** **Date Added:** 6/13/2000: **Description:** Using Extended mode on the local bus can generate incorrect transactions in certain combinations of consecutive reads and writes. **Workaround:** Do not use Extended mode on the local bus. **System Number:** 5959 **Fix Plan:** Not currently scheduled	1K87M
EFC1	**Inaccurate EFCOP IIR Outputs For Two or Fewer Coefficients** **Date Added:** 2/19/2002 **Description:** When using normal (dual) DMA or fly-by DMA transfers which have maximum transfer size greater than 32-bits with the EFCOP to perform IIR filtering with two or less IIR coefficients, the first output of IIR filter will be lost. The rest of the outputs will be shifted and inaccurate. Use only DMA 32-bit maximum transfer size for both input and output channels. **Fix Plan:** Not currently scheduled.	1K87M
SC4	**SC140 May Hang After Write To PCTL0 Register.** **Date Added:** 2/19/2002 **Description:** Write to PCTL0 immediately freezes the core for 150-900 cycles. If the system is busy (e.g. pre-fetch transactions), the core may not exit the freeze state. **Workaround:** Option A: 1. Ensure that the EFCOP is not working. 2. Ensure that the local bus to L1 memory is not working. 3. The program that writes to PCTL0 is in internal memory. 4. Write to PCTL0 immediately after reset before any external data accesses. Option B: Do not write to PCTL0. **System Number:** 7560 **Fix Plan:** TBD	1K87M
SC5	**SC140 CORE May Hang After Illegal Execution Set** **Date Added:** 2/19/2002 **Description:** Upon receipt of an illegal execution set the SC140 CORE may enter a freeze state that can only be released by reset. **Workaround:** No workaround available. **System Number:** 7541 **Fix Plan:** TBD	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SC6	**Incorrect Data on Trace Buffer Read During Core Freeze** **Date Added:** 2/19/2002 **Description:** After writing data to the Trace Buffer, the TB is disabled, in order to read from it. There are 2 options to read the TB and the problem occurs in both: **1.** Reading the TB by software. If, While reading the TB by SW into a core register, there is a core freeze, One data over-write the previous data. **2.** Reading the TB from the JTAG. If the JTAG reads the TB while there is a core freeze, the data will not be correctly sampled. **Workaround:** **1.** Software: Read the TB by software, when there is no core freeze: a. The program will be in internal memory b. Make sure the EFCOP is not working. c. Make sure the local bus to L1 memory is not working. d. The Write-Buffer is empty. e. There are no other move commands except for the TB read. **2.** JTAG: a. Read the TB from JTAG only when the core is in DEBUG mode. b. Before reading the TB, flush the Write-Buffer. **System Number:** 7604 **Fix Plan:** TBD	1K87M
SC7	**Change of Flow May Cause Incorrect Trace-Buffer Data** **Date Added:** 2/19/2002 **Description:** When programing the EOnCE for tracing events of change of flow (TCHOF) and interrupts (TINT), the Trace-Buffer will be updated on every event by the source and destination addresses. In the event of a CHOF (change of flow) to another CHOF with an interrupt request in between, the Trace-Buffer is updated with additional data, which is incorrect and is not needed for the trace. **Workaround:** Perform post-processing after reading the Trace-Buffer. Search in the data for a source address and the destination before it should be the destination of that source. That means there is a destination which came before its source. Delete the source and the previous data. **System Number:** 7794 **Fix Plan:** TBD	1K87M
SC8	**Debug Exception Request Form JTAG is Not Accepted During Core Freeze** **Date Added:** 5/21/2002 **Description:** JTAG debug exception request is not accepted by the Core during freeze. If the request is asserted and negated during core freeze, the request is discarded. **Workaround:** Assert Debug request from JTAG. When entering the exception routine, assert by software an external pin (EE pin for example), to signal the exception Service Routine is now executed. After that, a new JTAG instruction can be written. **System Number:** **Fix Plan:** TBD	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
SC9	**EE Pins Do Not Enable Different EOnCE Modules During Core Freeze** **Date Added:** 5/21/2002 **Description:** If EE pins are asserted to enable events in EOnCE during core freeze and the request is negated during the same core freeze, the event is not enabled. **Workaround:** Poll on Core status from JTAG. Assert the EE pin(s) until the Core is not in freeze for at least 3 cycles. **System Number:** **Fix Plan:** TBD	1K87M
CPM94	**FCC $\overline{\text{RTS}}$ Signal Not Asserted Correctly** **Date Added:** 2/25/2003 **Description:** At the beginning of an HDLC frame transmission which is preceded by more than one opening flag, $\overline{\text{RTS}}$ will not be asserted if $\overline{\text{CTS}}$ is negated. This may cause a deadlock if the modem waits for the assertion of $\overline{\text{RTS}}$ before asserting $\overline{\text{CTS}}$. **Workaround:** Implement one of the following: 1. Transmit no flags between or before frames. 2. Clear FPSMR[NOF] bit. Set GFMR[RTSM]=1 to ensure RTS/ is asserted when FCC is enabled. However no hand shaking activities with the modem will occur for all the proceeding frames. **System Number:** **Fix Plan:** TBD	1K87M
CPM96	**ATM Performance Monitoring with AAL1 CES** **Date Added:** 2/25/2003 **Description:** ATM Performance Monitoring with AAL1 CES Data in DPRAM is corrupted when performance monitoring is enabled in the receiver. **Workaround:** Implement one of the following: 1. Disable Receive Performance Monitoring RCT[PMT]=0. 2. Use microcode patch available from Freescale. **System Number:** **Fix Plan:** TBD	1K87M
CPM97	**MCC SS7 - No SUERM interrupt generated after an ABORT** **Date Added:** 2/25/2003 **Description:** Octet Count Mode is not entered properly when idles are received after an ABORT. Therefore N_Cnt is not decremented and no SUERM interrupt will be generated. This problem only affects the SS7 micro code in ITU-T / ANSI mode (SS7_OPT[STD]=0). **Workaround:** Use the latest RAM based SS7 micro code package available from Freescale. **Fix Plan:** TBD	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM98	**I^2C Erratic Behavior Can Occur if Extra Clock Pulse is Detected on SCL** **Date Added:** 8/25/2003 **Description:** The I^2C controller has an internal counter that counts the number of bits sent. This counter is reset when the I2C controller detects a START condition. When an extra SCL clock pulse is inserted between transactions (before START and after STOP conditions), the internal counter may not get reset correctly. This could generate partial frames (less than 8 bits) in the next transaction. **Workaround:** Do not generate extra SCL pulses on the I^2C bus. In a noisy environment, the digital filter I2MOD[FLT] and additional filtering capacitors should be used on SCL to eliminate clock spikes that may be misinterpreted as clock pulses. **System Number:** MSIls09133 **Fix Plan:**	1K87M
CPM99	**CPM 99: ABR TCTE[ER-TA] Corruption** **Date Added:** 8/25/2003 **Description:** When the AAL5 ABR ROM microcode is in use, the TCTE[ER-TA] field can be overwritten with an erroneous value. This, in turn, causes the TCTE[ER-BRM] to be updated with this value. Because TCTE[ER-BRM] holds the maximum explicit rate value allowed for B-RM cells, an erroneous value in this field could have a detrimental effect on the network performance. **Workaround:** Use the microcode patch available from Freescale.	1K87M

Table 2. Silicon Errata (Continued)

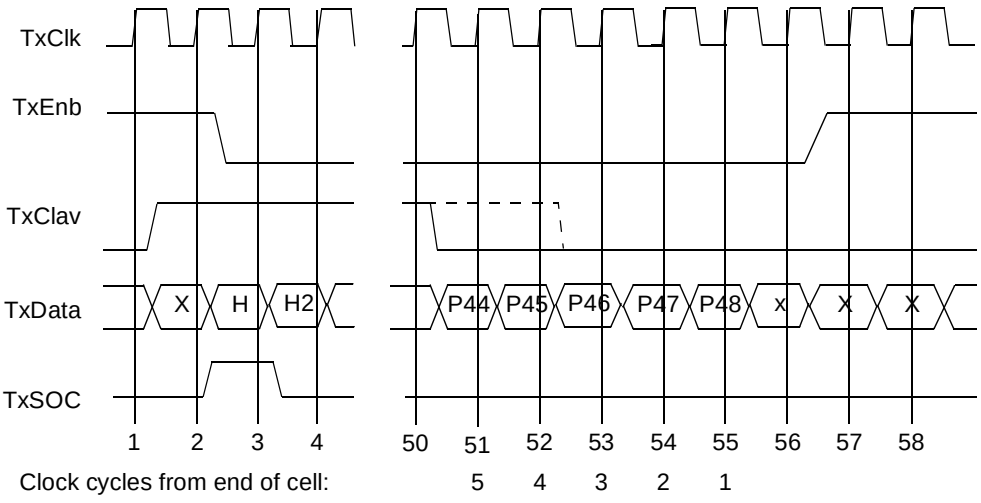
Errata Number	Errata Description	Applies to Mask
CPM101	**FCC RxClav Timing Violation (Slave)** **Date Added:** 1/15/2004 **Date Revised:** 11/05/2004 **Description:** FCC ATM Receive UTOPIA slave mode. When the RxFIFO is full, RxClav is negated 2 cycles before the end of the cell transfer, instead of 4. A master that polls RxClav or pauses 3 or 4 cycles before the end of the cell transfer may sample a false RxClav, and an overrun condition may occur. The dashed line in the timing diagram below depicts the actual RxClav negation (two cycles before the end of the cell transfer instead of four cycles). The signals in the timing diagram are with respect to the master, so the Tx interface is shown. **Workaround:** 1. The master should not poll RxClav or pause a cell transfer 4 cycles before the end of a cell transfer. The master should poll 2 cycles before the end of the current cell or later. This can be achieved by introducing cell-to-cell polling (and transfer) delay, which is equal or larger than one cell transfer time. If this can be achieved, the impact on performance is minimal. 2. Configuring ATM only on FCC1 and setting FPSMR[TPRI] ensures the highest priority to FCC1 Rx. In addition, for CPM usage lower then 80 percent (as reported by the CPM performance tool based on UTOPIA maximal bus rate), the CPM performance is enough to guarantee that the RxFIFO does not fill up. 	1K87M
CPM111	**FCC Missing Reset** **Date Added:** 1/15/2004 **Description:** The TxBD may not close for the FCC in Half-Duplex 10BaseT Ethernet. There may be a mismatch between the actual transmitted BD and the BD for which the status is updated. As a result, the status of one to three BDs may not be updated. They appear to be "ready" although the associated frames have been transmitted (assuming a frame per BD). **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11064 **Fix Plan:**	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM112	**FCC Missing Reset at OverRun** **Date Added:** 12/19/2003 **Description:** TxBD may not be closed for FCC in Half-duplex 10BaseT Ethernet. There may be a mismatch between the actual transmitted BD and the BD for which status is updated. As a result, the status of one to three BDs may not be updated, and they would appear "Ready", although the associated frames have been transmitted (assuming a frame per BD). **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11064, 11067 **Fix Plan:** N/A	1K87M
CPM113	**Incorrect Return Value from Event Register Read (SCC, SPI, I^2C, and SMC)** **Date Added:** 12/19/2003 **Description:** When the Event Register is read while the SCC, SPI, I^2C, or SMC is active, it is sometimes read as 0, even though it has some bits set. **Workaround:** **System Number:** 11068 **Fix Plan:**	1K87M
CPM115	**APC Transmits Unwanted Idle Cells** **Date Added:** 12/19/2003 **Description:** In heavily loaded ATM applications, if the ATM pace controller (APC) is configured for multiple priority levels and a burst of traffic for transmission is sustained long enough on the highest priority APC table, then an unwanted idle cell can be trasmitted on the lower priority APC tables when there are cells available in lower priority APC scheduling table for transmission. The transmission of the unwanted idles could cause the valid ATM cells on lower-priority APC scheduling tables not to be transmitted. This transmission of unwanted idles can affect all ATM channels that are not located in the highest-priority APC scheduling table. **Workaround:** Increase the size of lower-priority APC scheduling tables so they are large enough to absorb any burst or back-to-back bursts on the highest-priority APC scheduling table. Otherwise, use the microcode patch available from Freescale. **System Number:** 11069 **Fix Plan:**	1K87M
CPM116	**Pointer 93 in Partially Filled (PFM) Mode** **Date Added:** 1/15/2004 **Description:** In PFM mode, the pointer value of 93 is not generated, causing the loss of synchronization at the far end. Also, when the pointer value of 93 is received, the synchronization is lost, which causes a loss of data and the resynchronization routine. **Workaround:** Use microcode patch provided by Freescale. **System Number:** 11912 **Fix Plan:**	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM117	**False Address Compression** **Date Added:** 11/05/2004 **Description:** If there are active AAL0 channels and a CRC-10 error has been received, VP-level address compression might have false results, which could lead to one of the following: • Wrong calculation of a VP pointer address • Cells might be falsely discarded as misinserted cells • Misidentification of misinserted cells (in CUAB mode) This is a statistical error, which is conditional on the reception of AAL0 cells with a CRC-10 error. The probability of false address compression is directly correlated with higher CPM bit rate and longer system bus latency. While the false address compression is possible only if there are active AAL0 channels, it may have an impact on all AAL types. However, it cannot occur unless AAL0 cells with CRC-10 error have been received beforehand. **Workaround:** Use the microcode patch supplied by Freescale. **System Number:** 17129	1K87M
CPM118	**Aborted HDLC Frame Followed by a Good Frame** **Date Added:** 7/11/2004 **Description:** When an aborted HDLC frame is followed by a good frame, the receive data buffer may contain the data of the aborted frame followed by the data of the good frame. **Workaround:** Use the microcode patch provided by Motorola. **System Number:** 15906 **Fix Plan:**	1K87M
CPM119	**Ethernet Collision Occurs on the Line 125 Clocks after TX_EN Assertion** **Date Added:** 7/11/2004 **Description:** When an ethernet collision occurs on the line 125 clocks after TX_EN assertion, late collision will be reported even though this is only 63 bytes into the frame instead of 64. When a collision occurs 124 cycles after TX_EN assertion, no event is reported, the TxBD is not closed, and transmission halts. Retransmission behavior is correct for collisions occurring between assertion of TX_EN and 123 clocks. **Workaround:** Use the microcode patch provided by Motorola. **System Number:** 15908 **Fix Plan:**	1K87M
CPM120	**SS7_OPT[FISU_PAD] Parameter has no Effect on the Number of Flags between FISUs** **Date Added:** 12/22/2004 **Description:** The SS7_OPT[FISU_PAD] parameter has no effect on the number of flags between FISUs. Regardless of the value of this field, one flag will be present between back-to-back FISUs. **Workaround:** Use the latest SS7 microcode package provided by Freescale. **System Number:** 18767 **Fix Plan:** None at this time.	1K87M

Table 2. Silicon Errata (Continued)

Errata Number	Errata Description	Applies to Mask
CPM121	**TDM Data Frame Corruption** **Date Added:** 11/05/2004 **Description:** During a write to one of the SI registers (GMR, AMR, BMR, CMR, DMR) while one or more TDMs are working, one data frame of a working TDM may become corrupted. **Workaround:** Work with the shadow RAM when changing data and do not disable and then enable the TDM. **System Number:** 17460	1K87M
GEN3	**Device Withstands ESD CDM Stress of 400V Instead of 500V** **Date Added:** 10/31/2003 **Description:** Device meets the ESD specifications for Human Body Model (HBM) of 1000V and Machine Model (MM) of 100V but does not withstand the Charged Device Model (CDM) of 500V. All pins guaranteed to `withstand CDM 400V.` **Workaround:** N/A **System Number:**	1K87M

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