

# Advance Information

MPC2605CE/D Rev. 0.1, 5/2003

MPC2605 Integrated Secondary Cache Chip Errata





This document details all known silicon errata for the MPC2605. Table 1 provides a revision history for this chip errata document.

**Table 1. Document Revision History** 

Revision No.	Significant Changes
0	Initial release.
0.1	Removed the table, "Revision Level to Part Marking Cross-Reference." Removed the silicon revisions subheading from the table, "Summary of Silicon Errata and Applicable Revision."

This document pertains to all revisions and part markings of the MPC2605.

Table 2 summarizes all known errata and lists the corresponding silicon revision levels to which the errata applies.



Table 2. Summary of Silicon Errata and Applicable Revision

Problem	Description	Impact	Work Around	Silicon Revision Levels
Flush Corruption	Asserting ARTRY during a L2 Flush sequence will cause chip failure.	Memory corruption during an L2 None Flush	None	ALL

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# Error No. 1: L2 Flush Corruption

### Overview:

Asserting ARTRY during a L2 Flush sequence will cause chip failure.

# **Detailed Description:**

An ARTRY asserted during the L2 Flush sequence will cause a corruption of memory write-back data and address.

# **Projected Impact:**

Corrupted Memory

### **Work Around:**

None.

### **Projected Solution:**

When initiating a L2 Flush sequence, or during a L2 Flush sequence, all other 60x bus transactions should be ceased.



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