MCXW71_2P43C

Mask Set Errata

Rev. 2.0 — 1 July 2025 Errata

1 Mask Set Errata for Mask 2P43C

1.1 Revision History

This report applies to mask 2P43C for these products:

- MCXW71
- MCXW716CMFxAx
- MCXW716AMFxAx

Table 1. Revision History

Revision	Release Date	Significant Changes
2.0	6/2025	The following errata were added. • ERR052558 • ERR052438 • ERR052403 • ERR052742
1.1	9/2024	The following errata were added. • ERR052407
1.1	9/2024	Initial Revision

1.2 Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR050500	Core: Group priority of a Non-secure interrupt might be incorrect when AIRCR.PRIS is set
ERR050501	Core: DFSR.EXTERNAL is not set correctly when waking up from sleep
ERR050502	Core: Execution priority might be wrong for one cycle after AIRCR is changed
ERR050503	Core: Non-secure HardFault exception might preempt when disabled by AIRCR.BFHFNMINS
ERR050504	Core: Sorting of pending interrupts might be wrong when high latency IRQs are pending
ERR050505	Core: Access permission faults are prioritized over unaligned Device memory faults
ERR050810	I3C: t(CPB) & t(CPSr) , t(CASr) parameter different from standard
ERR050811	I3C: tSU_STO and tSU_STA do not met for I3C legacy mode Fm+
ERR051051	Core: A partially completed VLLDM might leave Secure floating-point data unprotected
ERR051118	LPI2C: Aborting a multiple byte receive transfer will cause subsequent transfer to hang
ERR051119	LPI2C: NACK Detect Flag can be set when IGNACK=1
ERR051120	I3C: The Not Acknowledge Error bit in the Master Errors and Warnings register (MERRWARN[NACK]) is not set when slave does not acknowledge High Data Rate - Double Data Rate (HDR-DDR) read.

Table 2. Errata and Information Summary*...continued*

Erratum ID	Erratum Title
ERR051135	RF RAM Retention increases power consumption in Power Down modes
ERR051136	Read Stall: flash read/write operation causes error during program/erase
ERR052403	FlexCAN: CAN frame drops in Enhanced RX FIFO when message buffer (MB) is locked for more than 1 CAN frame time (33 us)
ERR052407	DCDC: Failure changing to Low drive-strength mode
ERR052438	FlexCAN: CAN frame may drop when using Enhanced RX FIFO
ERR052558	FlexCAN: Message buffer (MB) overrun status is cleared when reading Enhanced RX FIFO (ERF)
ERR052742	FRO6M clock is not stable

2 Known Errata

ERR050500: Core: Group priority of a Non-secure interrupt might be incorrect when AIRCR.PRIS is set

Description

Cortex-M33 1113997-C:

When the processor is configured with Security extension and AIRCR.PRIS is 1, the Armv8-M architecture requires that the priorities of Non-secure interrupts are modified to ensure that Secure interrupts are prioritized over Non-secure interrupts. The Armv8-M architecture requires that lower priority numbers take precedence over higher priority numbers. Because of this erratum, a Non-secure interrupt with higher priority number might be handled in the wrong order compared to another Non-secure or Secure interrupt.

Workaround

There is no workaround for this erratum.

ERR050501: Core: DFSR.EXTERNAL is not set correctly when waking up from sleep

Description

Cortex-M33 1367266-C:

An external debug event which causes the processor to enter Debug state or the debug monitor should set DFSR.EXTERNAL. It has been found that this field is not set if the event occurs while the processor is asleep.

Workaround

There is no workaround.

ERR050502: Core: Execution priority might be wrong for one cycle after AIRCR is changed

Description

Cortex-M33 1435973-C:

AIRCR is used in the NVIC active tree to calculate the execution priority, which in turn is used to determine fault escalation, exception preemption, and other NVIC-related behaviors. When the active tree is pipelined and there are high latency IRQs active, there might be a glitch in the active tree output for one cycle after AIRCR is changed. The glitch results in NVIC producing wrong execution priority that is neither based on the old AIRCR value nor the new one.

Workaround

There is no workaround for this erratum.

ERR050503: Core: Non-secure HardFault exception might preempt when disabled by AIRCR.BFHFNMINS

Description

Cortex-M33 1453380-C:

When the processor implements the Security Extension and AIRCR.BFHFNMINS is 1, the Non-secure banked version of SHCSR.HARDFAULTPENDED can be set to 1. This Non-secure pended HardFault might not preempt per architecture because it does not have enough priority (that is, the processor is in HardFault handler mode). If AIRCR.BFHFNMINS is subsequently changed to 0 with the Non-secure HardFault still pending, then the architecture requires that the Nonsecure HardFault should never preempt regardless of execution priority. Because of this erratum, the pended Non-secure HardFault exception preempts when AIRCR.BFHFNMINS is 0 and current execution priority is larger than -1 (Non-secure HardFault having higher priority).

Workaround

There is no workaround for this erratum.

ERR050504: Core: Sorting of pending interrupts might be wrong when high latency IRQs are pending

Description

Cortex-M33 1540599-C:

The NVIC contains a pending tree which sorts all pending and enabled interrupts based on priorities. If DHCSR.C_DEBUGEN and DHCSR.C_MASKINTS are 1, DHCSR.S_SDE is 0 and halting debug is allowed, then Nonsecure PendSV, Non-secure SysTick, and Non-secure IRQs should be masked off and they should not affect the sorting of pending and enabled secure interrupts. If multiple high latency IRQs are pending and enabled with different security targets and priorities, then Non-secure IRQs which should be masked off might cause the pending tree output to be a pending Secure nterrupt without highest priority. This is because of incorrect masking before doing priority comparisons in the tree.

Workaround

There is no workaround for this erratum.

ERR050505: Core: Access permission faults are prioritized over unaligned Device memory faults

Description

Cortex-M33 1080541-C :

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

Workaround

There is no workaround.

However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.

ERR050810: I3C: t(CPB) & t(CPSr) , t(CASr) parameter different from standard

Description

1. tCBP parameter defines the minimum timing for clock before stop Tcbp (I3C Spec V1.1.1 Table 122) in I3C push-pull mode and may not meet the value in the standard 17.2ns .

The value observed for FCLK 160MHz is 6.26ns and for 120MHz is 8.34ns respectively .

IMPACT : No Functional Impact .The actual I3C devices are not expected to have any issues at all, as the behavior around STOP is only verifying SCL is High when SDA rises, so plenty of setup time (tSU_OD (I3C Spec V1.1.1 Table 122) - 3ns) .

2. tCBSr parameter defines the minimum timing for clock before repeated start TCBSr(I3C Spec V1.1.1 Table 123) in I3C push-pull mode and may not meet the value in the standard 17.2ns .

The value observed for FCLK 160MHz is 9.39ns and for120Mhz is 12.51 ns respectively .

IMPACT : No Functional Impact .For Repeated start The actual behavior of Targets will be to detect that SDA is low on the following SCL Falling edge , for which there is plenty of setup (tSU_OD (I3C Spec V1.1.1 Table 122) - 3ns) . Even if a Target has an SDA rise detector which checks if SCL is High, there is plenty of setup time (tSU_OD (I3C Spec V1.1.1 Table 122) - 3ns).

3. tCASr parameter defines the minimum timing for clock after repeated start (tCASr) (I3C Spec V1.1.1 Table 123) in I3C push-pull mode and may not meet the value in the standard 17.2ns .

The value observed for FCLK 48MHz is 10.42 ns .

IMPACT : No Functional Impact .For Repeated start The actual behavior of Targets will be to detect that SDA is low on the following SCL Falling edge , for which there is plenty of setup (tSU_OD (I3C Spec V1.1.1 Table 122) - 3ns) . Even if a Target has an SDA rise detector which checks if SCL is High, there is plenty of setup time (tSU_OD (I3C Spec V1.1.1 Table 122) - 3ns).

Workaround

User needs to skip conformance timing checks for tCBP , tCBSr , tCASr

ERR050811: I3C: tSU_STO and tSU_STA do not met for I3C legacy mode Fm+

Description

Minimum timing for clock before stop tSU_STO (I3C Spec V1.1.1 Table 121) is not met in I3C legacy Fm+ mode . Standard expected minimum 260ns .

For Different FCLKs tSU_STO observed is in range of (94ns - 125ns)

This conformance violation will not cause functional issue as the behavior around STOP is only verifying SCL is High when SDA rises, so plenty of setup time (tSU_DAT (I3C Spec V1.1.1 Table 121) - 50ns) .

Minimum timing for clock before repeated start tSU_STA(I3C Spec V1.1.1 Table 121) is not met in I3C legacy Fm+ mode . Standard expected minimum 260ns

For different FCLKs tSU_STA observed is (92 - 145ns) .

This conformance violation will not cause functional issue as the behavior around Repeated Start is only verifying SCL is High when SDA falls, so plenty of setup time (tSU_DAT (I3C Spec V1.1.1 Table 121) - 50ns) .

Workaround

User needs to skip conformance timing checks for tSU_STA and tSU_STO.

ERR051051: Core: A partially completed VLLDM might leave Secure floating-point data unprotected

Description

Arm errata 2219175

Affects: Cortex-M33

Fault Type: Programmer Category B

Fault Status: Present in r0p0, r0p1, r0p2, r0p3, r0p4, r1p0. Open.

The VLLDM instruction allows Secure software to restore a floating-point context from memory. Due to this erratum, if this instruction is interrupted or it faults before it completes, then Secure data might be left unprotected in the floating point register file, including the FPSCR.

Configurations affected:

This erratum affects all configurations of the Cortex-M33 processor configured with the Armv8-M Security Extension and the Floating-point Extension.

Conditions:

This erratum occurs when all the following conditions are met:

- There is no active floating-point context, (CONTROL.FPCA==0)

- Secure lazy floating-point state preservation is not active, (FPCCR_S.LSPACT==0)

- The floating-point registers are treated as Secure (FPCCR_S.TS==1)

- Secure floating-point state needs to be restored, (CONTROL_S.SFPA == 1)

- Non-secure state is permitted to access to the floating-point registers, (NSACR.CP10 == 1)

- A VLLDM instruction has loaded at least one register from memory and does not complete due to an interrupt or fault

Implications:

If the floating-point registers contain Secure data, a VLSTM instruction is usually executed before calling a Non-secure function to protect the Secure data. This might cause the data to be transferred to memory (either directly by the VLSTM or indirectly by the triggering of a subsequent lazy state preservation operation). If the data has been transferred to memory, it is restored using VLLDM on return to Secure state. If the VLLDM is interrupted or it faults before it completes and enters a Non-secure handler, the partial register state which has been loaded will be accessible to Non-secure state.

Workaround

To avoid this erratum, software can ensure a floating-point context is active before executing the VLLDM instruction by performing the following sequence:

- Read CONTROL_S.SFPA

- If CONTROL_S.SFPA==1 then execute an instruction which has no functional effect apart from causing context creation (such as VMOV S0, S0)

ERR051118: LPI2C: Aborting a multiple byte receive transfer will cause subsequent transfer to hang

Description

If the MCFGR0[ABORT] register bit is used to abort a receive transfer that consists of multiple bytes, then the subsequent transfer after the abort completes will hang.

Workaround

If MCFGR0[ABORT] is set by software, first wait for the LPI2C to go idle (MSR[MBF] = 0) and then issue a software reset (MCR[RST] = 1) before initiating the next transfer.

ERR051119: LPI2C: NACK Detect Flag can be set when IGNACK=1

Description

When MCFG1[IGNACK] is set any received NACK should be ignored, but under some conditions the NACK Detect Flag (NDF) can still be set.

However, the LPI2C will not automatically generate a STOP or Repeated START if the NACK Detect Flag is set when IGNACK=1 and the transfer will continue as if the NDF had not been set.

The LPI2C will continue to block a new START condition if the NDF is set.

Workaround

When IGNACK=1, the NDF must be cleared by software to allow new I2C transfers to start.

ERR051120: I3C: The Not Acknowledge Error bit in the Master Errors and Warnings register (MERRWARN[NACK]) is not set when slave does not acknowledge High Data Rate - Double Data Rate (HDR-DDR) read.

Description

I3C: The Master Errors and Warnings register (MERRWARN) is used to debug I3C/I2C errors and warnings in Master mode. The MERRWARN[NACK] bit does not set when slave does not accept read while HDR-DDR mode is used. This bit is set to 1 in Single Data Rate (SDR) mode when slave does not acknowledge.

Workaround

If a slave does not accept HDR-DDR read and master side is not able to debug, the slave availability/readiness can be checked by sending SDR read request. The MERRWARN[NACK] will reflect the slave response.

ERR051135: RF RAM Retention increases power consumption in Power Down modes

Description

When the RF RAM is retained by using the RF_CMC[RAM_PWR] registers in Power Down mode, the power consumption is around 2uA higher than when using Deep Sleep mode.

Workaround

Turn off the RF RAM manually using the RF_CMC[RAM_PWR] registers before entering in Power Down modes.

ERR051136: Read Stall: flash read/write operation causes error during program/erase

Description

The Program Flash Controller (PFC) provides access to the flash memory from the AHB bus masters. If a master does a flash memory access to a flash array while that array is busy, the access is terminated with an AHB bus error. The PFC implements an optional "flash read stall" mechanism to avoid this situation. This mechanism is enabled by a control bit in the Secure Miscellaneous System Control Module (SMSCM). If enabled, the flash read stall logic will hold any flash memory access to a flash array while that array is busy. The access will "stall" (be held in its AHB bus data phase) until the target flash array is not busy. Once the busy flag has been negated, the access will be complete.

This device has a PFC for the primary flash attached to the main processor and a PFC for the flash in the radio subsystem. The primary flash and the radio subsystem flash each have three flash arrays - a main program flash array, an IFR flash array, and an IFR1 flash array. Each PFC can access the three flash arrays of its attached flash. The flash read stall should work for access to any of these arrays. Due to a logic error, the flash read stall mechanism only works correctly for accesses to a busy program flash array. Even when the flash read stall mechanism is enabled, access to busy IFR or IFR1 flash arrays is not stalled and terminates with an AHB bus error.

Workaround

Do not access IFR or IFR1 flash arrays when they may be busy due to a flash erase or program operation. When performing Flash erase/program operations, execute from SRAM or ROM.

ERR052403: FlexCAN: CAN frame drops in Enhanced RX FIFO when message buffer (MB) is locked for more than 1 CAN frame time (33 us)

Description

If Message Buffer (MB) and Enhanced RX FIFO both are configured for reception, and FlexCAN Message Buffer is locked for a long time (more than 1 CAN frame, 33us), FlexCAN receives some frames in FIFO and then start dropping the frames.

Workaround

There are two possible workarounds:

1) Core must read the message buffer within the 33 us after locking the MB.

2) Avoid using a few specific Message Buffers (MBs) as listed below:

ERR052407: DCDC: Failure changing to Low drive-strength mode

Description

The DCDC output may fail when transitioning from Normal to Low drive-strength, resulting in the DCDC output voltage dropping to the point it is not able to adequately power the VDD_CORE supply, or causes temporary brown-out conditions. This failure may occur when both of these conditions occur:

1) The transition from Normal drive strength (DCDC_VDD_DS = 10b) to Low drive-strength (DCDC_VDD_DS = 01b) occurs when the DCDC is actively switching the output.

2) The voltage level set in the bitfield SPC->LP_CFG[DCDC_VDD_LVL] is greater than or equal to the current output voltage of the DCDC.

Because this failure requires a specific timing to manifest, it may fail very infrequently in an application. The greater the load current of the DCDC, the more likely the failure will occur because the DCDC will spend more time in the active switching period. A higher rate of transitioning to Low drive-strength will also see a higher failure rate.

There are two scenarios when the DCDC drive-strength can transition from Normal to Low drive-strength, and this failure may occur:

1) While the MCU is in Active power mode, and the application changes the drive-strength setting by writing 01b to the bitfield SPC->ACTIVE_CFG[DCDC_VDD_DS]. Writing this bitfield will start the transition to Low drive-strength.

2) When the MCU enters a low-power mode (Deep Sleep, Power Down, or Deep Power Down), and Active mode uses Normal drive-strength with ACTIVE_CFG[DCDC_VDD_DS] = 10b, while the low-power mode uses Low drive-strength with LP_CFG[DCDC_VDD_DS] = 01b.

Workaround

This issue will always be avoided when the voltage level at the low-power low drive-strength is lower than the current output voltage of the DCDC. Before transitioning to Low drive-strength, ensure the voltage level in LP_CFG[DCDC_VDD_LVL] is lower than the voltage level in Normal drive-strength configured by ACTIVE_CFG[DCDC_VDD_LVL].

If the desired voltage level in LP_CFG[DCDC_VDD_LVL] is the same as the level currently set in ACTIVE_CFG[DCDC_VDD_LVL], a workaround is to temporarily increase the voltage level in ACTIVE_CFG[DCDC_VDD_LVL], and then transition to Low drive-strength with the lower level in LP_CFG[DCDC_VDD_LVL]. Here is the sequence for this workaround:

1) Ensure LP_CFG is configured for Low drive-strength and the desired voltage level in Low drive-strength mode

2) Wait for the SPC bit SC[BUSY] to be clear.

3) Write ACTIVE_CFG[DCDC_VDD_LVL] with the value for the voltage level one step higher than the desired level in LP_CFG[DCDC_VDD_LVL].

4) Start the transition to Low drive-strength

If the workaround sequence above is used when the MCU enters a low-power mode, then when the MCU wakes the DCDC will return to Normal drive-strength with the output voltage level configured in SPC->ACTIVE_CFG[DCDC_VDD_LVL]. If a lower voltage level is preferred, the application can lower DCDC voltage by waiting for the bit SC[BUSY] to be clear and writing the new voltage level to SPC->ACTIVE_CFG[DCDC_VDD_LVL].

ERR052438: FlexCAN: CAN frame may drop when using Enhanced RX FIFO

Description

An incoming CAN frame will be lost (i.e not latched into its expected Enhanced Rx FIFO data element), if both following two conditions are met simultaneously. There will be no indication that the frame was lost.

Conditions:

1. A write access is made to the message buffer Control and Status word (MB_CS) of a specific message buffer corresponding to the expected Enhanced Rx FIFO data element. Each Enhanced Rx FIFO data element corresponds to different message buffers impacted by this erratum and cannot be determined by software.

2. Depending on the timestamp configuration, the write access is made when receiving a frame at one certain Controller Host Interface (CHI) clock cycle either:

a. Around the time between the seventh bit of EOF and the second bit of IFS if timestamp is disabled (CTRL2[TSTAMPCAP] = 00b) or

b. Around the time between the fifth bit of EOF and seventh bit of EOF if timestamp is enabled (CTRL2[TSTAMPCAP] = 01b or 10b or 11b)

Workaround

To avoid the potential for dropped CAN frames, one of the following options may be implemented:

Workaround #1 : Disable Enhanced RX FIFO feature.

Workaround #2 : If the Enhanced RX FIFO feature is enabled, restrictions apply to certain Message Buffer (MB) numbers for both RX and TX. Either do not use these MB’s at all or at minimum, avoid updating the Control and Status word of these MBs when any reception to the Enhanced Rx FIFO could occur. This means, it would be safe to update the Control and Status word of these MBs when the FlexCAN is for example in Freeze mode or when it is ensured against frame reception from the CAN bus. Below are the MB numbers that have these restrictions:

ERR052558: FlexCAN: Message buffer (MB) overrun status is cleared when reading Enhanced RX FIFO (ERF)

Description

Message buffer status becomes "full" when a frame arrives, and status becomes "overrun" when a second message arrives in the same message buffer, if first message has still not been read. If frame reception is happening in ERF and the frame is being read from ERF, these reads could incorrectly clear the MB overrun status. As a result, the overrun event can be missed by the application.

Workaround

Use one of the following workarounds:

Workaround #1: Don’t use Enhanced RX FIFO (ERF).

Workaround #2: Don’t use any of the message buffers from MB0 to MB7 for reception if ERF is enabled. MB0 to MB7 can be used for transmission.

ERR052742: FRO6M clock is not stable

Description

The FRO6M clock is not stable on some parts. FRO6M outputs lower frequency signal instead of 6MHz when device is reset or wakes up from low power. It can impact peripherals using it as a clock source.

Workaround

1) Use clock source other than the FRO6M. For example, use FRO192M instead of FRO6M as clock source for peripherals.

2) If the application must use FRO6M clock. Signal Frequency Analyzer (SFA) can be used to measure FRO6M frequency and adjust accordingly. Please refer to the following community article for more details on this procedure: https://community.nxp.com/t5/Wireless-Connectivity-Knowledge/Clock-Measuring-using-the-Signal-Frequency-Analyzer-SFA-module/ta-p/2103732

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