MOTOROLA

Communications and Advanced Consumer Technologies Group

MCF5202/03

Chip Errata to MCF5202/03

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MCF5202/03 Errata for mask set 1G94F, 2G94F

Specification Change

S1 - Make HALT a user-mode opcode under Background Debug Module control. The definition of the Configuration/Status Register bit 10 (CSR[10]) will be changed from Reserved for Future Use (RFU) to User Halt Enable (UHE). The new definition will require that CSR[10] be asserted (logic 1) to allow the execution of the HALT opcode while in user mode. Fixed on 2G94F.

Instruction Processing

I1 - During the address phase of a line transfer, AD(1:0) may be improperly driven to a non-zero value. This error potentially affects the byte select logic equations for memory spaces designated as either word or byte port sizes. The workaround is for byte select logic to ignore AD(1:0) during line transfers and to use the binary value 00 instead.

Workaround:

Externally force AD[1:0] low during the address phase of a line size transfer.

I2 - The MOVEC opcode to load the Vector Base Register (VBR) does not function correctly.

Workaround:

Use the following code to load the VBR:

```
MOVE.W#$2700, SR# disable interrupts
MOVE.La7,<mem># save current stack pointer
MOVE.LVBR, a7# load desired VBR into A7
MOVE.La7, vbr # load the Vector Base Register
MOVE.L<mem>, a7# restore the stack pointer
MOVE.W#$2000, SR# enable interrupts
```

Bus Operation

B1 - If reset is asserted when the MCF5202/03 is the bus master, control signals (ts, dtip, and rw) are not driven high (pulled up) before tristating potentially causing external system logic to see invalid logic levels that could result in errorous operation.

Workaround:

Place pullup resistors on TS, R/W and DTIP.

B2 - Double bus faults don't halt the processor. The processor instead loops on the exception stacking and address fetch.

B3 - During the address phase of a BDM-initiated write cycle, when the attributes have been explicitly set to indicate a supervisor or user code access, the atm pin is not asserted (to indicate instruction), as it should be.

Cache Operation

C1 - The cache replacement counter is implemented as a two-bit counter. To ease tracking of where allocated cache entries will reside, this counter will be enhanced to clear on system reset or invalidation of the cache.

C2 - If a region of memory has been designated as read-only (by way of setting bit 2 in either of the ACRs, or by setting bit 10 in the CACR [for default memory space]), and the cache is disabled (bit 31 of the CACR is 0), an attempted write to such a region will be allowed instead of reporting a "read-only" bus error condition to the core. If the cache is enabled (by setting bit 31 in the CACR), an attempted access to a read-only region will not be allowed. The appropriate error response will be sent to the core.

Workaround:

Enable the cache (set bit 31 in the CACR), or

Configure the bus termination logic to assert Xtea on attempted writes to such a write-protected region.

Background Debug Mode

BDM1- When using a pulsed mode DSCLK, execution of a GO instruction will ignorecause subsequent HALT events (Halt instruction, Hardware Breakpoint, Single Step, ...). The next rising edge of DSCLK will return the part to normal Background Debug Mode operation. Fixed on 2G94F.

Workaround:

To minimize the window when HALT events are ignored, you can issue another BDM command (e.g., NOP) immediately following the GO instruction.

BDM2- If an emulator tries to place the procesor core in single-step mode after execution of a HALT instruction, the mode will not be entered correctly. As a result, the procesor will execute normally after being restarted.

Workaround:

As a workaround, after the CSR[4] bit has been asserted, the BKPTx pin can be asserted, then negated while halted. When the processor is restarted, it will correctly execute in single-step mode. A second workaround is to use the PC trigger mechanism instead of the HALT opcode.

BDM3- If the processor is halted for any reason, a read of the CSR does not clear the 4-bit halt status field in CSR[27:24]. Rather, the status defining the given halt condition remains asserted until the processor is either reset or restarted.

BDM4- While in single-step mode (CSR[4]=1), all interrupts are ignored, regardless of the state of CSR[5].

Timing

T1 - For 25MHz operation, sp19 (DAX, TEAX, TBIX, AVECX, BGX, AAX, IPLX, RSTX, BKPTX, DSCLK, DSI valid to CLK (Input Setup) must be relaxed from 8ns to 11ns.

T2 - For 25MHz operation, sp13 (CLK to A/D-Out Valid) from 25ns to 26ns.

T3 - JTAG spJ11 (TCK Falling Edge to Boundary Scan Data Valid) must be relaxed from 30ns to 35ns.

Specification Changes (These anomalies will NOT be changed in future mask sets)

Background Debug Mode

SBDM1 - When a BDM command is serially shifted into a ColdFire microprocessor, the debug module requests the use of the KBus to perform the required operation. Under certain conditions, the processor may never grant the KBus to the debug module, resulting in the BDM command never executing.

Specifically, the KBus grant may be withheld from the debug module if the processor is executing a tight loop where the entire loop is contained within one aligned longword.

Examples include:

```
        align  4
label1: nop
        bra.b    label1

        align  4
label2: bra.w    label2
```

Workaround:

The workaround is to force the loop to be aligned across two longwords. Given this alignment, the processor will correctly grant the KBUS to the debug module.

MCF5202/03 Errata Change History:

- Rev 1.0:Initial xxxx Errata with I1 and B1. 12/20/95
- Rev 1.1:Added Specification change S1 and Errata BDM1. 2/12/96
- Rev 1.2:Updated S1 and BMD1 as fixed on 2G94F. Added C1, B2, and BDM2-4. 6/18/96
- Rev 1.4:Added I2 (RAS). 08/19/96
- Rev 1.5:Added B3, C2,T1, T2, T3. 12/05/96
- Rev 1.6:Added SBDM1. 1/3/97

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