MC9328MXL Integrated Processor (i.MXL)

Chip Errata for Masks 0L45N, 1L45N, and 2L45N

This document covers silicon errata information that relates to the 0L45N, 1L45N, and 2L45N masks of the MC9328MXL (i.MXL).

Rev. 12 adds Erratum 21 to this document.

Table 1. Silicon Errata to MC9328MXL

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
1.	**Module:** MMA **Failure:** Internal pipeline data operations are not completely stored into the FIFO.	**Impact**: Internal pipeline data operations are not completely stored in the FIFO if a DMA request is asserted and begins to move data out of the FIFO. When this happens, the last data sent as part of the pipeline operation is lost. *For example:* When only one access to the memory remains for the next burst, a DMA request is asserted before the last access is completed. *Illustration:* If there are 28 accesses required and the burst is set to 9, after 3 bursts, only one access will remain. **Workaround:** Ensure that the data pipeline operation is complete before a DMA is asserted. The programmer must add one additional count to the MMA_MAC_MULT register to create an additional single MAC operation that ensures the last data is stored in the FIFO before the DMA is asserted. The performance impact for this additional access is minimal because a MAC operation is used predominately for large MAC calculations. *For example:* an MP3 uses 512 MAC operations for DCT, therefore the impact of adding one more is negligible. **Fix Status:** No metal-fix solution planned.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
2.	**Module:** SDRAMC **Failure:** It is necessary to use a separate timer to prevent access to the SyncFlash immediately after the SyncFlash is re-enabled from deep low-power mode.	**Impact**: If SyncFlash channel is disabled, the SDRAMC puts the syncflash into a mode called deep low-power mode. When the SyncFlash is re-enabled, it requires a 100 μs period to initialize before allowing any access to it. The current design does not have a built-in timer to prevent access before 100 μs has passed. Therefore, an access occurring during this time period could return invalid data from the SyncFlash. **Workaround:** Use the TIMER register to count 100 μs to determine the time period during which the user is not allowed to access the SyncFlash. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
3.	**Module:** SDHC **Failure:** SDHC FIFO is not available to be written after Status Register bit[6] is set.	**Impact**: The inner FIFO ready operation remains active 3 MMCCLK cycles after the status bit[6] is set. Because of this delay, the user could possibly overwrite the FIFO before it is completely cleared, that results in a corrupt data pattern being sent. **Workaround:** To avoid FIFO corruption, the user can either increase the MMCCLK frequency to 8 MHz or higher, or insert a software delay of 3 MMCCLK cycles. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
4.	**Module:** SDHC **Failure:** Status register bit[13] is not updated until 3 MMCCLK cycles after the End Command Response interrupt is generated to AITC.	**Impact**: The End Command Response interrupt generation remains active for 3 MMCCLK cycles before the status bit[13] is set. If the user reads the status register to correlate the generated interrupt by SDHC, the late response on the STATUS may mislead the interrupt handler. **Workaround:** To avoid the late response on STATUS, the user can either increase the MMCCLK frequency to 8 MHz or higher, or insert a software delay of 3 MMCCLK cycles. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
5.	**Module:** CSI **Failure:** Signal Race exists between HSYNC and pixel clock in CSI.	**Impact**: A signal race can exist between the HSYNC and pixel clock during the input stage of the CSI module when the HSYNC is toggled to high a short time before the falling edge of the pixel clock and the gated clock mode is enabled. An unwanted glitch results that causes an extra pixel to latch in the first column. **Workaround:** To avoid the signal race, the timing of the HSYNC or pixel clock must be adjusted so that the HSYNC is toggled to high after the falling edge of the pixel clock. Insert a dedicated delay buffer at the CMOS sensor HSYNC output before it is input to the i.MXL chip. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
6.	**Module:** CSI **Failure:** Invalid data latching in CSI.	**Impact**: A signal race can occur between HSYNC and the pixel clock in the input stage of the CSI module when the HSYNC is toggled to high a short time before the falling edge of the pixel clock and the gated clock mode is enabled. When this occurs it results in an unwanted pixel data to be latched. **Workaround:** Always tie the pixel clock low when the gated clock mode is enabled to prevent latching invalid pixel data. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
7.	**Module**: LCDC **Failure**: The Memory Controller arbiter (MEMC) does not break and release the ARM™ core's back-to-back burst access to the other (for example, LCDC, DMA, and MMA) bus masters. In this situation, the ARM core's back-to-back access does not use an IDLE cycle as a separator.	**Impact**: Typically, the back-to-back burst access that does not use the IDLE cycle as a separator occurs for operations such as cache fill, miss, and burst operations by the ARM processor. In cases such as this, the MEMC arbiter incorrectly treats the back-to-back sequence as a single instruction process that causes the other bus masters to wait longer to access the bus. On the AHB bus, only the LCDC and MMA modules are affected. Because the MMA is not a periodic and time critical module with regards to requesting the grant of the bus, the impact of this issue is minimal, although the LCDC frame buffer refresh can be greatly impacted. **Workaround:** Use a dummy DMA transfer to and from a dummy memory space to force the MEMC to release the bus for other bus masters. For more detailed information and code example, please visit our website www.freescale.com/imx. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
8.	**Module:** USB Device Port **Failure:** Limitation on using DMA for USBD IN data transfer. There is a limitation on using DMA to transfer continuous data from memory to a 64-byte USBD FIFO (FIFO1 and FIFO2) when using a short packet (<37 bytes) followed by a long packet (> 32 bytes). *For example:* A 6 byte packet followed by a 64 byte packet, or a 32 byte packet followed by a 40 byte packet such that the short packet length + the long packet length is greater than 64 bytes (FIFO depth).	**Impact**: The DMA request does not clear after the reception of a short packet, causing a long packet to start filling in the FIFO before the data in the short packet is moved out of the FIFO. This causes the USBD FIFO to overflow and generate an error that prevents a DMA interrupt DMA_ISR from being generated. This occurs because the ALARM bit (DMA request) being cleared is based on the setting of the 4*GR[2:0] granularity bits in USB_EPn_FCTRL register. The ALARM bit for IN transfer is set when the amount of data bytes that remain in the FIFO is below the alarm value (ALARM[5:0] in the USB_Epn_FALARM register and cleared when there is less than 4*GR[2:0] of free bytes that remain in the FIFO. The Granularity bits GR[2:0] are fixed at 3 bits regardless of the FIFO depth. For IN transfer, DMA requests are cleared when FREE data bytes are 4*GR[3:0]. Because GR[2:0]=3 * 111 as a maximum value, there can only be 28 free bytes. Therefore, a 6 byte short packet in the 64-byte FIFO will not dessert the DMA request. **Workaround:** Two methods are used to prevent this limitation depending on the data packet size: 1. *For data packet sizes of less than 5 bytes:* After the short packet data transfer, software must poll the USBD BYTE_COUNT==0 before initiating the next DMA transfer. This ensures that FIFO can accept the next long data packet of 64-bytes. 2. *For data packet sizes of 5 bytes and greater:* Use a 32-byte FIFO instead of a 64-byte FIFO to ensure that the DMA request is cleared. The granularity bits GR[2:0] must be set to 111. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
9.	**Module:** RTC **Failure:** An alarm set to an odd number of seconds results in a false interrupt one second before the actual alarm time, followed by the actual interrupt.	**Impact**: This double interrupt is the result of a glitch produced by the seconds counter bits 1 and 0. Bit 0 of the seconds counter has greater loading than bit position 1. Upon receiving a clock signal to update the seconds counter, the seconds counter bit 0 changes state to be slower than counter bit 1. This glitch causes the alarm to see a momentary match, triggering the interrupt one second early. When the seconds counter actually does match the alarm value, another interrupt is triggered (if it has not been disabled following the previous interrupt) at the correct time. *For example:* If you set the alarm to “xx : xx : xx : 15 sec”, when the second counter changes from 13(1101) to14(1110), the bit position 1 changes faster than bit position 0. The result is 13(1101) to 15(1111) to 14(1110). This 15(1111), the glitch, matches the alarm setting and triggers the interrupt. **Workaround:** Either set the seconds alarm register to an even value or, if set to an odd value, when the interrupt occurs, check the current time against the alarm time. If it does not match, then clear the interrupt and return. The actual interrupt will occur one second later. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
10.	**Modules:** IOPAD **Failure:** Power-up leakage during the recommended power-up sequence, NVDD>AVDD>QVDD. In the normal configuration, the maximum current leakage occurring during the power-up period can be up to 600mA.	**Impact:** Using the workaround, the power-up current can be minimized to less than maximum specified operating current. **Workaround:** Attach a 1 KΩ series resistor to each tied-low input pin. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
11.	**Modules:** MEMC/AHBC **Failure:** The LCD flicker issue is not completely resolved by the use of dummy DMA transfer (See Erratum number 7). The LCDC DMA high/low setting does not ensure that the next bus request is triggered in the event the current DMA burst is not completed. The problem occurs when the next bus request is initiated while the LCDC is waiting for the last data in the current DMA burst. This is because when the LCDC is waiting for the last data, it only expects an HREADY signal to be asserted. So, if the next bus request is triggered while the LCDC is waiting, the bus request will be missed. A data fetch can not be initiated while data in FIFO is being continuously drained so an under-run will eventually occur. *In Summary:* If the next bus request is issued when the LCDC is waiting for the last data in the current DMA burst it will not be recognized.	**Impact:** The low mark must never be set higher than 10 and the high mark must be set at 3. **Workaround:** For a bus that is heavily loaded and that requires SDRAM access, a dynamic burst length is recommended: • fixed burst length = 0 • high mark = 3 • low mark = 8 For a very heavily loaded system, increasing the low mark value increases the chance of a bus grant of the system bus, at the expense of more frequent bus requests. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

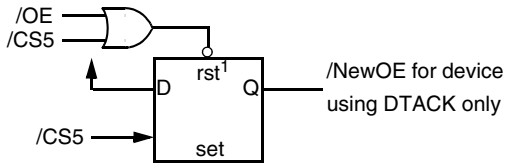
Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
12.	**Modules:** EIM **Failure:** CS5 fails read operation when using the DTACK function.	**Impact**: When CS5 is configured to an external input DTACK signal to terminate the bus cycle (for example WSC = 0x3F), using either DTACK mode (DTACK_SEL = 0) or WAIT mode (DTACK_SEL = 1), the CPU or DMA read cycles in CS5 memory space may terminate incorrectly. CS5 can function normally by using wait state control bus termination—that is, WSC is not set to 0x3F. All write cycles will function correctly. **Workaround:** *DTACK mode (DTACK_SEL = 0):* No workaround. *WAIT mode (DTACK_SEL=1):* In Wait mode the OE signal for read cycle is negated up to 1 system clock before a data latch occurs at the end of bus cycle, possibly causing incorrect data to be latched by the i.MXL because the external device releases the data bus after OE negates. The workaround is to use external logic (one D-flip flop and one OR-gate) to extend OE negation time until the CS cycle is completed (after or at CS5 rising edge). D-FF connection must be D=1, RST= /OE OR /CS5, CLK= CS5, Q=NewOE for DTACK device only. To avoid disrupting other devices using /OE, the NewOE signal only replaces the /OE signal going to a DTACK device. See Figure 1.  1. If using LCX logic from ON Semiconductor, expect propagation delays from /OE and /CS assertion to /newOE of 3.0 to 12.5 ns. Freescale Semiconductor cannot recommend one supplier over another and in no way suggests that ON Semiconductor is the only supplier of logic devices. **Figure 1. D-FF Connection Workaround** **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N
13.	**Modules:** EIM **Failure:** Port A pin 17 (multiplexed with DTACK) inadvertently affects other chip-select functions when DTACK is not used.	**Impact**: When the DTACK signal is not used, toggling the GPIO pin PA17 will adversely affect the other EIM chip-select functions. **Workaround:** PA17 is restricted for the DTACK functionality only. Thus, in any other situation when DTACK is not used, this pin must be pulled up or tied high (may be done by simply setting the corresponding PUEN bit, configuring it as an input, and leaving the pin unconnected). If the DTACK functionality is used, the pin will only toggle during CS5 accesses and should not toggle during any non-CS5 access. **Fix Status:** No metal-fix solution.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
14.	**Modules:** SDHC **Failure:** SDIO does not work in 1-bit and 4-bit modes.	**Impact**: No support in SDIO mode. Memory mode in 1-bit and 4-bit modes are supported. **Workaround:** Use SDIO SPI mode with the SPI module on chip i.MX1/ i.MXL processor. For more information, refer to the application note AN2689. **Fix Status:** No silicon fix is planned.	0L45N 1L45N 2L45N
15.	**Modules:** SDRAMC **Failure:** Cannot support SDRAMs with less than 1kilobyte page size.	**Impact**: Not able to support single chip 4M x 16-bit (8 Mbyte total size) SDRAM devices or devices with a page size of less than 1 kilobyte. A page size is defined as the number of bits in a row in the SDRAM device. **Workaround:** Must use SDRAM devices with 1 kilobyte or greater page sizes. **Fix Status:** No metal fix is planned.	0L45N 1L45N 2L45N
16.	**Modules:** SDRAMC **Failure:** Cannot support SDRAMs with column address sizes of 10.	**Impact**: Not able to support single chip 32M x 16-bit (64 Mbyte total size) SDRAM devices or devices with a column address size of 10. **Workaround:** For 64 Mbyte SDRAM devices the configuration of 16 M x 32 or two 16M x 16-bit must be used to form a 32-bit data bus, where either configuration contains only 9 column addresses. **Fix Status:** No metal fix is planned.	0L45N 1L45N 2L45N
17.	**Modules:** SDRAMC **Failure:** In 16-bit mode, only SDRAM device with 9 Cols are supported.	**Impact**: In 16-bit mode, burst access is not guaranteed for SDRAM with number of columns not equal to 9. Known impact is failure to support following devices in 16-bit mode: a. SDRAM with 12 Rows and 8 Cols (4Mx16-bit, 8MB total size) b. SDRAM with 13 Rows and 10 Cols (32Mx16-bit, 64 Mbyte total size) **Workaround:** No workaround is available. Recommend system designer to use 32-bit SDRAM if 8 Mbyte or 64 Mbyte memory configuration is desired. **Fix Status:** No metal fix is planned.	0L45N 1L45N 2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks

18.	**Modules:** ARM920T AHB Wrapper
	Failure: LDM instruction fails to load non-cached data from memory.
		Impact:
		When a load multiple (LDM) instruction is used to load two specific registers from an un-cached region of memory, and the load instruction begins immediately after a delayed buffered write, then the LDM will not load the second register correctly.
		Workaround:
		The ARM Realview 3.0 SP1 Build 617 compiler and linker have a patch that addresses this issue. With this patch applied, the compiler will not generate this LDM instruction. The Build 617 patch is available to download from the ARM website.
		
		To use the patch, users must insert
		"--branchpatch 920t-ldm2"
		to the compiler and linker command lines.
		
		For code compiled by a compiler other than the above stated tool, a manual search and replace for the LDM instruction of two values in assembly code can be done with multiple options for equivalent code replacements.
		
		Example 1:
		LDMIA r0, {r1, r2}
		is functionally IDENTICAL to:
		LDR r1, [r0]
		LDR r2, [r0, #4]
		
		Example 2:
		If updating the base register to a new value, such as:
		LDMIA r0!, {r1, r2}
		then this is functionally IDENTICAL to:
		LDR r1, [r0], #4
		LDR r2, [r0], #4
		Fix Status:
		No hardware fix planned.
			0L45N
			1L45N
			2L45N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks
19.	**Module:** UART **Failure:** Parity bug in UART transmitter	**Impact**: A parity error in UART character transmissions may occur. TxFIFO data being shifted out is not alterable after the start bit is issued. However, the parity bit can change after the start bit is issued and is not fixed until data Bit0 is issued. If the TxFIFO is overwritten by the CPU during the interval from the end of the start bit to the end of the data Bit0, there will be a mismatch between the data shifted out and the parity bit. In this case, a parity error may occur. **Workaround:** The following software solutions are recommended to be used in Interrupt Service Routines (ISRs) to avoid the parity bug. Polling can also be used instead of interrupts. 1. A maximum of 32 bytes can be written into the TxFIFO when transmission is complete (USR2.TXDC = 1). 2. A maximum of 31 bytes can be written into the TxFIFO when the TxFIFO is empty (USR2.TXFE = 1). 3. A maximum of 32 - n bytes, where n = UFCR.TXTL, can be written into the TxFIFO when the data level in the TxFIFO falls below the selected threshold (when USR1.TRDY = 1). **Fix Status:** No hardware fix planned.	0L45N 1L45N 2L45N
20.	**Module:** CSI **Failure:** When 1, 2, or 3 bytes are loaded into the CSI Rx FIFO, the DRDY bit sets and requires multiple reads of the RxFIFO to clear	**Impact:** The DRDY bit in the CSI Status Register is set before at least one data word is ready in the RxFIFO. However, the DRDY bit is set after a single byte is clocked into the RxFIFO. If 1, 2, or 3 bytes have been clocked into the RxFIFO, it takes 32 reads of the RxFIFO before DRDY clears. If a word of data has been clocked into the RxFIFO, reading the RxFIFO register one time clears DRDY as expected. **Workaround:** The RxFIFO Full Level of the CSI Control Register (CSICR[RXFF_LEVEL]) and the RxFIFO Full Interrupt of the CSI Status Register (CSISR[RXFF_INT]) may be used in order to define if the appropriate amount of image data is already latched. Otherwise, if less than a word of data has been clocked into the RxFIFO, the RxFIFO must be read 32 times to clear the DRDY bit. **Fix Status:** No metal-fix solution planned.	0L44N 1L44N 2L44N

Table 1. Silicon Errata to MC9328MXL (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status	Applies to Masks

21.	**Module:**
	SSI
	
	Failure:
	In word-wide frame-sync mode, if SSI_EN and TX/RX_EN are set near new frame start, SSI Receive and Transmit does not function properly and there is a chance of words getting missed/shifted or transmit data line being driven low for 1/2 clock cycles during the first frame.
		Impact:
		Receive malfunction: Rx data is usually taken with the period of FS=H. However, in some special use cases, it is changed to period of FS=L. Once this occurs, this period never returns to the period of FS=H.
		The issue occurs in the following conditions:
		Normal mode
		Sync mode
		Slave mode
		Some additional conditions of this scenario are:
		TX and RX are used at the same time (full duplex)
		SYN=1,RXDIR=0,TXDIR=0,TFDIR=0
		External clock is 2.048MHz
		Frame frequency is 8kHz
		Frame pulse width is 1 word (8 clock)
		SSI_EN and RE is set to 1 within latter 4 clocks of FS=H period (8 clocks)
		Transmit malfunction: TxData is changed to different value at only the first time of transmitting when TE bit is set just before FS signal or within FS timing.
		
		Workaround:
		To ensure a gap of at least 2 bit-clock cycles between SSI_EN and TX/RX bit setting (only for External word-wide frame-sync patterns), here is an example code for this workaround.
		void ssi_transmit_receive_test()
		{
		//parameters defined here
		Statement1 ();
		//clock configuration here
		Statement2();
		//AUDMUX configuration here
		Statement3();
		//SSI configuration here
		Statement4();
		//Enable SSI by programming SSI_SCR
		MEMWD(SSI2_SCR,scr_mask1);
		//delay some time for the SSI state machine to function
		//properly
		for(i=0;i<=5;i++);
		//Enable transmit and receive of SSI by programming
		//SSI_SCR
		MEMWD(SSI2_SCR,scr_mask2);
		……
		}
		
		Fix Status:
		No metal-fix solution planned.
			0L45N
			1L45N
			2L45N

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