Chip Errata

MC68SZ328CE3L57D/D
Rev. 1, 3/2004

MC68SZ328 Integrated Processor (DragonBall™): 3L57D Mask

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This document details silicon errata information for the 3L57D mask of the MC68SZ328 (DragonBall™ Super VZ) integrated processor.

Errata Number 26 through Number 28 have been updated since the last release of this document (Rev 0).

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
1.	**Module: eSRAM** Only 98K instead of 100K eSRAM is provided.	**Impact:** There is not enough internal memory (2Kbyte short) available for supporting double 160 × 160 × 16-bit frames or a single 320 × 320 × 8-bit frame. **Workaround:** Use external memory for LCD display memory if more than 98K display memory is required. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
2.	**Module: DRAM Controller** The DRAM controller fails to support CAS Latency 1 option: Program the SCL bits (bits 9–8 of CSE/CSF SDRAM Control register (Low word) to 1). If this option is selected, arbitration deadlock occurs, causing the system to hang during 68K/DMA writes to SDRAM and LCDC reads of display data.	**Impact:** Using CAS Latency 2 inserts one more clock cycle only during the read cycle. Write cycles are not affected. The SCL bits (CAS latency) determine the latency between a read command and the availability of data on the bus only. They have no effect on other timings. **Workaround:** It is advised to use CAS Latency 2. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
3.	**Module: CGM** The WIDTH bits in the CPU Power Control register do not function. Writes to them have no effect on the power control module: They always appear as zero to the internal duty cycle counter for controlling a CPUCLK burst. Therefore, burst mode cannot be supported. Only Doze mode can be used.	**Impact:** Burst mode is seldom used in a typical application for controlling power consumption of the CPU core. **Workaround:** Doze mode can be used to replace burst mode for low power management. It has no performance or power consumption impact to the system. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
4.	**Module: Chip-Select Module** The unprotected size in B, C, D, E, and F does not match with the defined size when the UPSIZ bit is enabled and when BUPS2, CUPS2, DUPS2, EUPS2, and FUPS2 bits are being used. The actual unprotected size is now found to be the original size divided by 16 when the extra UPSIZ bit is enabled.	**Impact:** When the EUPEN bit is enabled, the specified size is different than the example shown in the *MC68SZ328 Integrated Processor Reference Manual*: Original specified size: Unprotected size= Chip-Select Size/ $(2^{(7-UPSIZ)})$ Now, testing has confirmed that: Unprotected size= Chip Select Size/ $(2^{(11-UPSIZ)})$ Therefore, the actual unprotected memory area is one-sixteenth of the specified size. This may impact the memory areas designed for the operating system and supervisor usage. **Workaround:** There is no workaround for this issue. Caution is advised when partitioning protected and unprotected memory spaces. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
5.	**Module: 16-bit SRAM and LCDC** LCDC fails during use of external 16-bit SRAM when the SR16 bit is enabled.	**Impact:** 16-bit SRAM cannot be used for LCDC display memory. It does not affect the normal operation of 68K and DMA controller. There is no impact to the system using SDRAM or eSRAM as LCDC display memory. **Workaround:** A simple external interface circuit that uses the *UWE, *LWE, and *OE signals from MC68SZ328 can be built to interface with external 16-bit SRAM. Reference can be taken from the application note: *MC68EZ328 16bit SRAM Interface* (MC68EZ328SRAM16.pdf), which is available at: www.motorola.com/dragonball. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
6.	**Module: PWM2** After the PWM16 period register is programmed with #$0001 and the first PWM period rolls over, the period of PWMOUT for PWM2 cannot be changed, and the PWMIRQ bit in the PWM16 control register (0xFFFFF510) will not be set until PWM2 module is disabled and re-enabled.	**Impact:** There is no impact if PWM2 is properly programmed. PWM16 period = #$0001 is normally not used. **Workaround:** There is no workaround for this issue. Caution is advised when writing values to the PWM16 period register. **Fix status:** Because PWM16 period = #$0001 is normally not used, this bug will not be fixed.
7.	**Module: UART2** The baud rate in UART 2 does not match with the programmed value when the integer prescaler is being used and the PRESCALER value in the UART 2 Baud Control register (0xFFFFF912) is set to one of the following values: 0x08, 0x10, 0x18, 0x20, 0x28, 0x30, or 0x38. The actual baud rate is double the original programmed value when these PRESCALER values are used.	**Impact:** Only a minor software impact is expected, because this problem can be solved by using another set of PRESCALER values. **Workaround:** Use the following divider and prescaler values to replace those suggested by the “Selected Baud Rate Settings” table in the *MC68SZ328 Integrated Processor Reference Manual*. (This table assumes 33.16 MHz system clock.) **Baud Rate / DIVIDE / PRESCALER** 115200 / 0 / 0x2F 57600 / 1 / 0x2F 28800 / 2 / 0x2F 14400 / 3 / 0x2F 38400 / 1 / 0x26 19200 / 2 / 0x26 9600 / 3 / 0x26 4800 / 4 / 0x26 2400 / 5 / 0x26 1200 / 6 / 0x26 600 / 7 / 0x26 **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
8.	**Module: CGM** **Wrong MPFSR1 and UPFSR1 registers reset values** The reset values of the MPFSR1 and UPFSR1 registers in the Clock Generation Module (CGM) should be 0x18ff and 0x0000 instead of 0x1900 and 0x0001, respectively.	**Impact:** The default values of SYS_CLK and USB_CLK are 16.573213 MHz and 44.0 MHz instead of the intended 16.580608 MHz and 48.0 MHz, respectively. **Workaround:** Because the output frequency of MCUPLL and USBPLL are configurable, the SYS_CLK and USB_CLK can be re-programmed easily to other desired frequencies after system boot-up. Contact Motorola for example routines. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
9.	**Module: DMAC** **DMAC burst time-out** The DMA internal burst time-out counter set by the DMA Burst Time-out Control Register is not reloaded in each DMA burst. Therefore, the burst time-out value is counted from the beginning of the DMA transfer instead of the beginning of each burst.	**Impact:** Because time-out is now counted on a transfer basis instead of a burst basis, the programmable time-out counter might not be long enough to cover a whole DMA transfer. If the burst time-out function is disabled, the system can hang during DMA transfers when the external DTACK option is used in chip-select. The reason is that the burst time-out is designed to provide bus termination during DMA cycles when the burst cannot be ended after a certain amount of time. **Workaround:** If the External DTACK is not used, it is advised not to enable the DMA burst time-out function. Otherwise, make sure the burst time-out is longer than the time required for the whole DMA transfer. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
10.	**Module: DRAMC** Address signal A20 is not output in SDRAMC cycles. It remains at zero. However, multiplexed A20 via MA9/10/11 can function properly.	**Impact:** 64 Mbit SDRAM using non-interleaved (IAM bit=0) address mode cannot be supported. Other memory sizes are not affected. **Workaround:** Use interleaved address mode for supporting 64 Mbit SDRAM. Otherwise, use SDRAMs with larger memory, sizes such as 128 Mbits. Both non-interleaved and interleaved mode can be supported with this size. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
11.	**Module: DMA, MS** **4-word DMA burst cannot be used in Memory stick host controller (MSHC)** An incorrect data read may occur in MSHC's 4-word DMA burst transfer operation (DAKEN bit = 1 [MSCS register] and RFF bit = 1 [MSDRQC register]) when a DMA request generated by RxFIFO of MSHC cannot be served immediately by the DMAC.	**Impact:** A 4-word DMA burst cannot be supported with MSHC if more than one DMA requests are required to be used at the same time. **Workaround:** It is advised to program the DMA controller MSHC to use a 1-word DMA burst with the following configuration: DAKEN bit =0 (MSCS register) RFF bit = 0 (MSDRQC register) **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
12.	**Module: MMC/SD Host Controller** The RCRCERR bit (bit 5) of the MMC/SD status register, used for checking the CRC response status, reads inverted value after a command CMD2, 9, or 10 is issued from the MMC/SD Host Controller.	**Impact:** There is no hardware impact. **Workaround**: It is advised to invert the meaning of the RCRCERR bit when handling the CRC response status after issuing command 2, 9, or 10. The original setting for RCRCERR bit is: 0 = Response CRC error occurred 1 = No error After issuing command 2, 9, or 10, it becomes: 1 = Response CRC error occurred 0 = No error **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
13.	**Module: LCD Controller** The register bits VWAIT1[7:0] in the LCD Vertical Configuration Register 0 (0xFFFE081A), and the register bits PASS_DIV[7:0] in the LCD Vertical Configuration Register 1(0xFFFE081C) that are used for programming the delay between the last line of HSYN and the positive edge of VSYN for supporting Color STN panel do not function properly.	**Impact:** There is no hardware impact. **Workaround:** It is advised to set HWAIT2 to 0 in LCD Horizontal Configuration register 0 (0xFFFE0816). This setting will disable the delay setting option. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
14.	**Module: CGM** **The 16MHz crystal oscillator (OSC16M)** The 16 MHz crystal oscillator occasionally fails to start oscillation at QVDD=1.8 V.	**Impact:** There is no hardware impact. The 32.768 kHz crystal oscillator does NOT exhibit a similar problem because of a different design approach. **Workaround:** The 32.768 kHz crystal oscillator (OSC32K) can be programmed as the clock source for USBPLL. Refer to the *MC68SZ328 Integrated Processor Reference Manual* for corresponding register settings. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
15.	**Module: SDRAMC Controller** When *two* SDRAM chip-selects (CSE and CSF) are used and the SREFR[1:0] bits of CSE control register (Low word) (0xFFFFFC02) are programmed to 1 (1 row per refresh clock), the SDRAM cycle might halt and the system might hang.	**Impact:** The power consumption of SDRAM will be increased when using the workaround of doubling the refresh rate. **Workaround:** It is advised to use 2 or 4 rows per refresh clock in CSE and double the SDRAM refresh rate specified on SDRAM datasheet. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
16.	**Module: MMC/SD Host controller** The CRC Read Error (CRCRDERR) bit (bit 3 of MMC/SD Status Register) shows incorrect status during MMC/SD data write operation. During a write operation, the status bit “Read CRC Error” is incorrectly on. The flag is only valid during read operations and is invalid only during write operations.	**Impact:** There is no impact because the CRC read error bit is not used in data write operations. **Workaround:** It is advised to ignore this bit during the MMC/SD write operation. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
17.	**Module: USB** **CMD Over bit** CMD_OVER bit can be incorrectly cleared by another address (device) SETUP packet. This situation causes the USBD to send a NACK signal to the Host in the control transfer status phase even though the device is ready to acknowledge the HOST. The problem occurs during the standard requests: GET_DESCRIPTOR, SET_DESCRIPTOR, or SYNTH_FRAME. Others requests are handled automatically by the UDC and will acknowledge correctly.	**Impact:** The impact is minimal in that it only takes more time to end the standard request in the USBD. **Workaround:** Set the CMD_OVER bit after receiving the standard request (GET_DESCRIPTOR, SET_DESCRIPTOR, or SYNTH_FRAME) from the Host and continue setting it until the device receives another command from host. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
18.	**Module: Chip select** **Early Cycle Detection function for Dynamic Memory (SDRAM and EDO DRAM)** The chip-select module fails to support the early cycle detection function for Dynamic Memory: Program the ECDD bit of chip-select control register 2 (0xFFFFF10C) to 1. In this case, SDRAM and EDO memory access cycles cannot be further reduced by one wait state.	**Impact:** There is no impact. This function is originally designed to further enhance the DRAM access performance. **Workaround:** There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.
19.	**Module: UART 1 and 2** **CTS Delta interrupt status** The CTS1 DELTA and CTS2 DELTA bits in the UART1 Transmitter register (0xFFFFF906) and UART2 Transmitter register (0xFFFFF916), respectively, are always set after the first CTS Delta interrupt is generated. Clearing the bits by writing 1 has no effect, and CTS Delta interrupt continues to wait.	**Impact:** There is no impact. The CTS DELTA interrupt function designed for signal status monitoring is normally not used in a serial port data transfer. **Workaround:** There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
20.	**Module: DMA** **The flyby feature provided by DMA cannot be supported.** The flyby function provided for I/O channels in DMA cannot guarantee data integrity.	**Impact:** There is no impact. This function is originally designed to further enhance the DMA transfer performance of I/O channels. **Workaround:** The flyby function selected in the FLYBY bit—bit 11 in I/O Channel Control register (0xFFFE00CC, 0xFFFE010C, 0xFFFE014C, 0xFFFE018C)—should always be programmed to 0 (Disable Flyby) for proper operation of DMA transfer. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
21.	**Module: SDRAM** **System clock is stopped before Self Refresh Entry command is issued.** The Self Refresh Entry command cannot be issued before the system clock is stopped if the instruction to disable MCUPLL for entering sleep mode is placed and executed in SDRAM. This is because SDRAMC counts 32 clocks from the last access before issuing the Self Refresh Entry command, while MCUPLL shuts down its clock output 31 clock cycles after the DISPLL bit is set.	**Impact:** Data cannot be retained in sleep mode if the Self Refresh Entry command cannot be issued. However, normal application usually places the driver for shutting down MCUPLL in Flash/ROM. Therefore, no impact is expected. **Workaround:** Ensure that no SDRAM access occurs 32 clock cycles before the system clock is stopped. A possible solution is to run the driver to shut down the MCUPLL in Flash/ROM. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
22.	**Module: ASP** **ASP module cannot support touch panel application due to the following failures:** 1. Bit accuracy of the ASP PEN ADC cannot be maintained and guaranteed across temperatures. 2. Bias voltage at R2a may jump to a wrong level at ASP startup, or at very low temperature when manual mode is selected.	**Impact:** An offset will be seen on the touchpoint when the temperature or bias voltage level at R2a changes. The variation percentage cannot be guaranteed. **Workaround:** No workaround is available. **Fix status:** The root cause of this design bug has been identified. All layer silicon fixes for achieving temperature compensation with software and solving the wrong bias level problem are being investigated.
23.	**Module: ASP** **The maximum input voltage of U analog input cannot be higher than QVDD (Typical: 1.8 V).** If U input is higher than QVDD, it introduces unexpected current offset to Pen ADC during X and Y sampling, and affects the accuracy of digital data output.	**Impact:** Some applications such as battery measurement cannot be implemented by using direct connection of voltage output to U input. A potential divider is needed to limit the voltage range. **Workaround:** It is advised to limit the U channel input voltage to the range from 0 V to QVDD. This can be done by using a potential divider circuitry. **Fix status:** The root cause of this design bug has been identified. No solution is available.

Table 1. Chip Errata to the MC68SZ328 (3L57D Mask) (Continued)

Erratum Number	Erratum Description	Impact, Workaround, Fix Status
24.	**Module: ASP** **Auto-Zero value given from AZ,X and AZ,Y data formats in Manual mode is incorrect** Due to Sw1 to Sw8 of ASP not all being opened automatically when data format AZ,X (Mode=01 and AZE=1) or AZ, Y (Mode=10 and AZE=1) is selected in manual mode (Auto=0), the AZ data returned from the Auto-Zero measurement is incorrect and cannot be used in computation for compensating the A/D conversion offset due to process drift and temperature changes.	**Impact:** There is minimal impact. One additional step is necessary to read the Auto-Zero value in manual mode. **Workaround:** Use the Read X option in manual mode (Mode=01 and AZE=0); however, program SW[8:1] = 0000 0000 to open all switches manually. This setting returns an Auto-Zero value instead of an X sample. **Fix status:** The root cause of this design bug has been identified. No metal layer solution is available. All silicon layer solutions for this problem are being investigated.
25.	**Module UART1** **Erratum#7 also exists in UART1.**	**Impact and workaround are same as those described in erratum#7.**
26.	**Module: LCDC** **VGA resolution cannot be supported.**	**Impact:** Flickering may be noticed when running an image at 640 x 480 resolution. **Workaround**: There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.
27.	**Module: SDRAMC** **Failure to send a self refresh command to the SDRAM before the processor goes into sleep mode.**	**Impact:** At times the SDRAM controller will not send self-refresh commands to the SDRAM before the processor goes into sleep mode. This will cause data loss since the SDRAM will not be able to refresh. **Workaround**: A software workaround has been implemented to bypass this issue. Refer the application note, AN2550, for details on a workaround. **Fix status:** The root cause of this design bug has been identified. No solution is available.
28.	**Module: ASP** **The Enhanced ADC is dependant on ambient temperature.**	**Impact:** The accuracy of the EADC can be compromised since it cannot compensate over temperature. **Workaround**: There is no workaround for this issue. **Fix status:** The root cause of this design bug has been identified. No solution is available.

NOTES

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