Device Errata

MC68DP356

Revision A.1. Mask 1E60C, 2E60C.

October 25, 1995

These errata items are only valid on A.1 silicon. This silicon is being shipped with this errata attached.

IMP Errata

1. Missing Pull-Ups on IMP I/O on WDOG_ TXD2 and TXD3 Pins.
(Work-around: Place external pull-ups if PCMCIA exists or otherwise necessary)
Also the pull-ups for the PCMCIA address and data busses should be pull downs according to the PCMCIA standard. This will be fixed in future revisions.

2. When the PC reads an empty FIFO (receive) in 16550 mode it should read the same value as the last value read even though it has already been read. In the 68356 reading an empty FIFO gives different data than the last byte read.

3. In DISCPU mode the IMP part of the 68356 is not able to enter low power.

4. In ENCPU mode BG_ and BGACK_ does not reset the 16 clocks counter, therefore the STOP instruction execution cannot be guaranteed if an external master acquires the 68000 bus just after writing to the low power reigister ($FB).

5. PCMCIA interrupts generated from the PCMCIA controller operate as follows:
The PCMCIA controller will set the INTR bit if the PTIE or BERR bit in the PCHER register is set. The IREQ pin will also be asserted for the corresponding event if the PTIEn or BERRIE bit is also set in the PCMR.
This does not comply with the PCMCIA spec. which requires that the IREQ pin should reflect the INTR bit in the CCSR in I/O mode at all times.

6. The PCMCIA Protection Register (PPR) and all the features controlled by it are not implemented in this revision. This includes the PCMCIA security features and ability to drive the 68000 address and data lines during low power mode.

7. Port A,B, and C pins are not guaranteed to be in the input state until CLKO starts to toggle (the PLL is locked).

8. In low power STOP, DOZE or STAND-BY mode, the IMP current consumption is higher than described in the 68356 User's Manual by up to 4mA .

9. When CD1_ and CTS1_ pins are used for PCMCIA (PC_A11, PC_A10), internally the signals CD1_ and CTS1_ to the SCC are pulled up (inactive).This is inconsistent with the IMP, where on other SCC2/3, those functions are by default turned active when their pin is configured as PIO. Because of this bug, the SCC cannot work in transparent mode with EXTSYNC enabled.
Workarounds:
a. Set the IPIN bit in the PCMR register which will reassign the PC_A11 pin to another pin and allow access to _CD1.
b. Initially set SCM1 register to loopback mode (DIAG=01) and set the DSR register to FFFF to achieve synchronization. Once the first character has been received switch to software operation (DIAG =11).

10. MRW (Mask Read Write) bit (in OR3-0) should not be set to a 1 in the
following configuration: Dchip with PC Enabled and with DSP Direct Access operating.

In this configuration, if the MRW bit is set, the DSP read accesses to the Direct Access Port (to the 68k bus) are unreliable.

11. In the JTAG port, when performing the HIGHZ instruction, DSO is at tri-state. and not by-passed as defined in the spec..

12. If the TRST_ pin is asserted (low), the DSP data bus pins (DD0:23) and the SCK pin are not forced to be inputs (HIGHZ).

Workaround:
After asserting TRST_, the user must insert through the JTAG scan the needed sequence to place these pins into an input state.

13. When executing CAPTURE_DR, and SCAN_OUT, 4 pins may output wrong value: DRESET_, CKOUT, RD_, WR_.

Patch: Ignore them when they appear at DSO.

14. There are no pullups on JTAG port as shown in figure 13-1 of the 68356 manual.

DSP Errata

1. DSP to IMP Direct access is not reliable if DSP executes accesses to any memory space with more than 3 DSP bus wait states.