68840 IFDDI B.1 ERRATA
Mask 2E59C

(June 14, 1995)

The IFDDI revision B.1 conforms with the full specification of the 68840, with the following exceptions.

1. Internal Cipher Loopback with non-Motorola Clock Generation and Recovery devices

RSCLK input is still used by the ELM receive clock, despite being in internal cipher loopback mode.

Workaround:

• Do not enable ciphering when using the loopback provided in the cipher control register.

• Use the external loopback provided in the clock recovery devices when implementing a cipher-enabled loopback.

2. 68840 PNOP to NOP transition drives data bus

When the bus controller changes the CNTL lines from a PNOP to a NOP, switching the operating mode from pipeline to normal mode, on the first cycle after this transition, the 840 will drive the data and parity buses for one clock regardless of the state of the R/W line.

Option 1:

The first bus cycle in which the CNTL lines transition from PNOP to NOP must be a "dummy" read cycle with the R/W line set equal to 1 assuring that any other device that might drive the data bus is forced into a tristate position during the first NOP cycle.

Option 2:

Using this workaround, it is assumed that the default mode when using both pipemode and normal mode in the same implementation is normal mode.

Each time the controller receives a request from the IFDDI, the controller moves to pipemode via PNOP, and then issues the burst.

When the REQ lines have negated, the design then returns to normal mode via a NOP access. At this time, the IFDDI drives the bus due to this errata, but the processor does not since the controller returns the bus to the processor (bus grant) only after the transfer cycle to normal mode has been completed. At this point the processor can read/write the IFDDI registers until the next DMA burst is requested.

The advantage of Option 2, is that only the controller hardware is affected by the errata

while the software remains the same.
The PNOP to NOP cycle is a lost cycle, but occurs for 1 or multiple data bursts, and not on register accesses. This workaround will work with the fixed revision as well.

3. Revision Register Change

The 840 Revision B registers were:

IREV - 0001_0000
REV - IFDDI_011_0000

The 840 Revision B.1 registers are :

IREV - 0001_0001
REV - IFDDI_011_0001

4. Erroneous SI_ERR Interrupt in MAC

If MAC_ON is asserted while the MACIF is attempting to transmit frames, the SI_ERR interrupt may be erroneously set. All other operations function correctly since there is no interface error, in spite of the interrupt. This situation can occur whether the PSF is used or bypassed, but the probability that it will occur is larger if the PSF is used (non-bypass).

Workarounds

Option 1:
Mask out the SI_ERR bit as there is no bus between the FSI and MAC cores which is visable to the user

Option 2:
Mask out the SI_ERR bit before asserting MAC_ON if the MACIF transmission is enabled (TE bit in MTR is set.)

Option 3:
Disable the MACIF transmission when MAC_ON is reset, and enable the tranmission only after MAC_ON has been set. Note that this option has ramifications at the system level since leaving the MACIF enabled aborts each frame continuously clearing the transmit ring. If the MACIF is disabled, the transmit frames will remain in the transmit ring and will be transmitted later.