MOTOROLA

Chip Errata
DSP96002 Digital Signal Processor
Mask: C15T/D12C

ERRATA

Errata Description	Applies to Mask
1. The maximum V_{ILM} value (Input Low Voltage) for MODA, MODB, and MODC pins must be 1.0 Volt instead of 2.0 Volts as indicated in the Data Sheet.	C15T D12C
2. The INT instruction does not operate correctly in Round-to-Nearest-Even and Round-Toward-Plus-Infinity modes. Round-To-Zero and Round-Toward-Minus-Infinity modes work correctly. The work-around solutions are: a. Use INTRZ instead of INT, if Round-Toward-Zero is acceptable. b. Use FINT with the rounding mode of choice, followed by INTRZ.	C15T D12C

3. The system Stack Pointer, SP, remains unchanged and is not postdecremented in the following instruction:
`BTST #N, SSH (Bit Test on Stack High)`
Use other combinations of instructions to test the SSH such as:
`MOVE SSH, register/memory (MOVE SSH,d0.l)`
`BTST #N, register/memory (BTST #N,d0.l)`
	C15T D12C

4. The status register (SR) remains unchanged and does not correctly reflect in the carry bit the value of the tested bit in the following instruction:
`BTST #N, SR (Bit Test on Status Register)`
Use other combinations of instructions to test the SR such as:
`MOVE SR, register/memory (MOVE SR, y:(R6))`
`BTST #N, register/memory (BTST #N, y:(R6))`
	C15T D12C

5. The value contained in the X data ROM for COS(PI/2) is 6.125742227e-17 instead of 0.0.	C15T D12C
6. When entering the DEBUG mode and the following instruction is RESET, the peripherals will still be reset although the RESET instruction was not supposed to be executed.	C15T D12C

Errata Description	Applies to Mask
7. In some border cases, on entering the debug mode, the OnCE Status Register (OSCR) may contain incorrect values.	C15T D12C
a. [Breakpoint/Trace Counter = 0] followed by [$\overline{DR}$ or DEBUGCC = True] If one of the breakpoint or trace counters reaches zero (indicating that at the next occurrence of the breakpoint/trace condition the chip should enter the debug mode) and the chip enters the debug mode due to another cause ($\overline{DR}$ assertion or execution of DEBUGCC with condition true), the OSCR will show that the debug mode has been entered due to $\overline{DR}$ or DEBUGCC (correctly) and breakpoint/trace (incorrectly)	
b. [96002 has just entered the debug mode] followed by [DEBUGCC = True] If the following instruction after entering DEBUG mode is DEBUGCC and the CC condition evaluated as true, the OnCE Status Register (OSCR) will show both the hardware and software causes for entering the DEBUG mode.	
8. If the 96002 cannot enter the debug mode because there is a pending bus access and the core is waiting for $\overline{TA}$ to be asserted, [OS0 = 0, OS1 = 0] will be indicated, instead of [OS0 = 1, OS1 = 1] which should be the case.	C15T D12C
9. The Program Memory Breakpoint Counter does not decrement when tracing (single-stepping) through a program with Program Memory Breakpoints enabled, and the breakpoint condition is met.	C15T D12C

Errata Description	Applies to Mask
10. In the DMA transfer modes triggered by DMA request (DTM1-DTM0 = 01, 10, and 11) if the requesting pulse on $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, or $\overline{\text{IRQC}}$ occurs during the period of time in which the chip is in its T wait (Tw) state (as a result of wait states in port A or port B) or when the chip computes denormalized results in the "IEEE mode" and the pulse is generated in the following manner: a. the request signal was previously asserted b. the request signal is deasserted c. the request signal is asserted (to generate the required edge) then the deassertion edge on the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ or $\overline{\text{IRQC}}$ pins will not be detected and the DMA transfer will not be triggered. Work-a-round: To ensure proper behavior of the DMA in the transfer modes that use external DMA request trigger, one shall ensure that the requesting line is normally deasserted and after the assertion it will be deasserted again within one CLK cycle. In the case where the DMA request trigger is the Host Interface Interrupt, the designer must guarantee that the trigger does not occur during a period of time in which the chip is in its T wait (Tw) state (as a result of wait states in port A or port B) or when the chip computes denormalized results in the "IEEE mode".	C15T D12C
11. When the 96002 is executing a Read-Modify-Write (RMW) instruction to an external memory location and is not master of the external bus during the cycle immediately preceding the read cycle of the RMW instruction, then the $\overline{\text{BL}}$ (bus lock) signal will be deasserted at the end of the read bus cycle and not at the end of the write bus cycle (as it should be according to the specifications). Note that this behavior will only affect multiple bus (dual-port) memory systems since the Bus Acknowledge ($\overline{\text{BA}}$) arbitration mechanism still behaves correctly.	C15T D12C

12. The SPLITB instruction does not operate correctly when bit 15 of the source operand is zero. Use other combinations of instructions such as:
`LSR #8,Dn`
`EXTB Dn`
If Dn should be left unchanged, then the sequence should be:
`MOVE Dn,Dm`
`LSR #8,Dm`
`EXTB Dm`
	C15T D12C

Errata Description	Applies to Mask
13. If a Host Processor writes two data words to the 96000 TX register such as both TX and HRX are full and the 96002 is executing a floating point instruction with denormalized results in IEEE mode (FREEZE condition) which is immediately followed by a read of the HRX, this read will be performed more than one time thus reading both the first and the second data word written by the Host Processor. The first data word will be lost and only the second data word will be available. There will be no indication that such an event occurred neither for the Host Processor nor for the 96002. Such an event cannot occur in the more common case of fast arithmetic mode (flush-to-zero). The work-a-round is to disable the IEEE mode when using the Host Interface.	C15T D12C

14. Sign extension instruction, EXTB, does not work correctly when bit 7 in the register is one.
 	
The work-a-round is to execute the following instruction sequence:
 	
`MOVE  #$FF,d0.l`
`AND  d0,d1 d1.l,d2.l`
`ORC  d0,d2 d1.l,d0.l`
`LSL  #$19,d0.l`
`JCC <  ENDEXT`
`MOVE  d2.l,d1.l`
 	
`ENDEXT`
 	
Assume d1.l contains input and output values whereas d0.l and d2.l contain temporary data.
	C15T D12C

NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP96002 mask numbers apply.

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