

DSP56720

Silicon Revision: 0M78E

[Table 1](#) defines Severity values for errata described in this document.

Table 1. Definitions of Errata Severity

Severity	Errata Type	Meaning	Workaround
1	Critical	Failure mode that severely inhibits the use of the device for all or a majority of intended applications	Unavailable
2	High	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications	Generally available
3	Moderate	Unexpected behavior that does not cause significant problems for the intended applications of the device	Generally available

[Table 3](#) lists known chip errata affecting the versions of DSP56720 identified in the final column. [Table 2](#) summarizes the errata described in more detail in [Table 3](#).

Table 2. Chip Errata Summary for DSP56720

Severity	Erratum ID	Title	Silicon Revision
3	ES153	Clearing Individual ESAI Interrupt Enable Bits	0M78E
3	ES154	Port A Data Register When Configured For External Memory Controller	0M78E

Table 3. Chip Errata for DSP56720

Severity	Erratum ID	Summary	Details	Silicon Revision
3	ES153	<p>Module Affected: ESAI/ESAI_1/ESAI_2/ ESAI_3</p> <p>Title: Clearing Individual ESAI Interrupt Enable Bits</p> <p>Release Date: September 2007</p>	<p>Description: If an ESAI transmit interrupt enable bit (TEIE, TEDIE, TIE, TLIE) or an ESAI receive interrupt enable bit (REIE, REDIE, RIE, RLIE) is cleared by software while that same interrupt is asserted then the interrupt vector received by the DSP56300 core may be for the ESAI Receive Data interrupt if no other ESAI interrupts are pending.</p> <p>This only occurs if the interrupt is disabled before the interrupt vector is calculated but after the DSP56300 core has accepted that interrupt as the highest priority pending interrupt. The ESAI Receive Data interrupt does not need to be enabled for this to happen.</p> <p>This errata also applies to ESAI_1, ESAI_2 and ESAI_3.</p> <p>Workaround: Mask the ESAI interrupt in the IPRP register while clearing an individual ESAI interrupt enable bit. It is also valid to globally mask all interrupts while the individual ESAI interrupt is disabled, but this is not required.</p> <p>Fix Plan/Status: Not fixed.</p>	0M78E
3	ES154	<p>Module Affected: GPIO</p> <p>Title: Port A Data Register When Configured For External Memory Controller</p> <p>Release Date: September 2007</p>	<p>Description: If Port A Control and Direction Register bits are configured to enable the External Memory Controller (PCRA[x] = PRRA[x] = 1) then the corresponding Port A Data Register bit must be kept clear (PCDA[x] = 0) otherwise the LAD[x] pin may be driven with an incorrect value.</p> <p>Workaround: For each bit in the Port A Data Register, ensure PCDA[x] = 0 whenever PCRA[x] = PRRA[x] = 1.</p> <p>Fix Plan/Status: Not fixed.</p>	0M78E

NOTES

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