MOTOROLA

Chip Errata
DSP56004 Digital Signal Processor
Mask: D40G

ERRATA

	Errata Description	Applies to Mask
1.	In SHI, I2C Master mode and $\overline{\text{HREQ}}$ enabled (i.e. HRQE[1:0] ≠ 00), receiving data is not functional. Workaround: In I2C master mode, use $\overline{\text{HREQ}}$ disabled (i.e. HRQE[1:0] = 00) for data receive.	D40G
2.	In SHI, I2C Master mode and $\overline{\text{HREQ}}$ enabled (i.e. HRQE[1:0] ≠ 00), when transmitting data, if the shift register contains data, clock pulses are halted as long as $\overline{\text{HREQ}}$ is negated. However, if HIDLE is now set, regardless of $\overline{\text{HREQ}}$, this last word will be transmitted and afterward a STOP event will be generated. This may cause an overrun condition in the slave's side and the last data word might be lost. Workaround: None.	D40G
3.	In SHI, Slave mode, after an overrun error has occurred (HROE=1) or even after clearing HROE by reading HCSR and then HRX, if the receive path handshake is then enabled (i.e. HRQE0=1) the $\overline{\text{HREQ}}$ output pin will not be re-asserted until after receiving another word and writing it into the FIFO. Workaround: A proper handshake operation is normally set prior to data word transmission. Enabling a slave receive path handshake after personal reset overcomes the problem.	D40G
4.	In SHI, SPI Slave mode with CPHA=0, if the SHI exits the personal reset state when $\overline{\text{SS}}$ is already asserted, an underrun condition is generated (HTUE is set). An attempt to clear HTUE by reading HCSR and then writing HTX may not clear HTUE. Workaround: When programmed in the SPI Slave mode with CPHA=0, the SHI should be activated (i.e. exit the personal reset state) when $\overline{\text{SS}}$ is negated. $\overline{\text{SS}}$ can be then asserted by the master device to initiate a word transfer.	D40G

Errata Description	Applies to Mask
5. In SAI, the transmit data empty status bit TLDE (TRDE) is cleared by writing data to the last enabled transmitter. If a read from the transmit control/status (TCS) register immediately follows, TLDE (TRDE) is read as set. Workaround: The TCS read instruction should not immediately follow the write instruction to the last enabled transmitter. At least one instruction cycle of pipeline delay is required.	D40G
6. In SAI, when a long interrupt routine is being served as a result of a status bit set, if the instruction that clears the status bit immediately precedes the RTI instruction, an undesired interrupt request is generated when exiting the long interrupt routine. Workaround: At least one instruction cycle of pipeline delay is required between the instruction that clears the status bit and RTI. At most, inserting a "NOP" before RTI solves the problem.	D40G
7. In EMI, if the port is currently programmed in one of the SRAM modes (EAM2=0), and it is then activated into the slow DRAM mode (i.e. ECSR is written with EME=1, EDTM=1 and EAM2=1) and an EMI access is triggered at the immediately following Icyc (usually using a one Icyc instruction), then the external access actually commences one Icyc later, i.e. three Icyc's after the trigger. The only implication of this statement is that the EMI pipeline is moved one Icyc ahead. Workaround: Not required.	D40G
8. In SHI, SPI Slave mode with CPHA=1, negation of $\overline{SS}$ between successive word transfers empties the shift register. If HTX is written before $\overline{SS}$ is negated, the data transferred from HTX to the shift register will be lost. Workaround: Keep $\overline{SS}$ asserted until after the Slave has transmitted the last word.	D40G

	Errata Description	Applies to Mask
9.	In EMI, SAI and SHI, interrupt requests can be generated when an interrupt bit is set. If the interrupts are disabled (i.e. the interrupt bits are cleared) after at least one interrupt was enabled, a previously generated interrupt request might be served by an erroneous interrupt routine (which differs from the routine associated with the request). Workaround: Disable the interrupts by first clearing the appropriate bits in IPR, and then clearing the interrupt enable bits.	D40G
10.	In SHI, the noise reduction filter in the narrow and wide modes is not functional.	D40G
11.	EMI write operations are performed according to base address only. The ability to execute write operations according to “BASE minus OFFSET” addresses is not functional.	D40G
12.	EMI Read/Write accesses do not operate properly during WAIT instruction. Workaround: The EMI should enter the personal reset state before executing the WAIT instruction.	D40G
13.	In SHI, the I2C General Call address (all zero address) is not recognized by the I2C slave.	D40G
14.	EMI write interrupts, in certain cases, might be serviced one instruction cycle later as compared to DSP56004 Rev B.	D40G
15.	The timing of the acknowledge pulse (timing 240 in the data sheet) on the OnCE DSO line is too short by 3Tc. The correct timing should be 4Tc+Th-3 ns (min) and 5Tc+7 ns (max).	D40G

Errata Description	Applies to Mask
16. If a DSP56004 is connected as one of the I^2C slaves in a multiple-slave I^2C system, and the I^2C master performs an I^2C transaction with another slave, the DSP56004 will be erroneously activated for receive or transmit if any data byte passing on the I^2C bus corresponds to its slave address.	D40G
17. In SAI, slave mode, TREL(RREL) = 0, after initialization, there is a possibility that the first bit in each data word will appear one serial clock cycle after WST(WSR) transition - as if TREL(RREL) was programmed to be set. Workaround: After enabling the transmitter(receiver) there should be at least four serial clock cycles free of any transition of WST(WSR).	D40G

NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56004 mask numbers apply.
3. Manuals and data sheets may also have errata that is documented on the appropriate errata sheet as discovered.

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