68HC05PV8AMSE1 Rev 0
October 31, 2001

Mask Set Errata 1

M68HC05PV8A Microcontroller Unit

INTRODUCTION

This mask-set errata provides information pertaining to the following MC68HC05PV8A MCU mask set devices:

- 0K20R

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter, for example K20R. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 1K20R.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code “0115” would indicate the 15th week of the year 2001.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC, PC, ZC or XC prefix. An SC, PC or ZC prefix denotes special/custom device. An XC prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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AEC HBM PERFORMANCE

The device passed ESD testing with the exception of a failing window at 1.3KV. In all cases the fail mode was a shift in the PortC1 or PortC3 total resistance threshold for contact monitor to ground marginally below the specification limit. The specification limit for resistance to ground is 2.5KΩ to 10KΩ with a typical result of 4KΩ. The failing parts had a resistance to ground of about 2.4KΩ.

By using substitution method the stress combination causing the failure was narrowed down to a positive ESD zap when V_{sup} was the zap return path to GND.

ULTRA LOW POWER MODE INTERRUPT

The Ultra Low Power Mode wakeup interrupts from either Port A (KWI) or from Port C could be masked if either a core-timer or 16-bit timer interrupt is being requested while the MCU is going into stop-mode.

Root cause

1. If an interrupt from either the core-timer or the 16-bit timer is requested at the same bus cycle, the CPU fetches the STOP instruction. The CPU will assert an internal STOP signal for only 1/2 bus cycle
2. If the ultra low power mode is enabled and the internal STOP signal is asserted, the voltage regulator controller will block the oscillator until either a KWI, a Port C interrupt, an IRQ interrupt or reset is asserted

Effect

Due to a non-asserted STOP line the wakeup-input synchronizers are enabled, preventing the asynchronous assertion of the external interrupts. Due to (2) no clocks are provided to clock the synchronizers

Work-around

1. Disable all interrupts of the core-timer as well as the 16-bit timer by clearing the interrupt mask bits before going into stop-mode (only necessary if ultra low power mode is selected)
2. Insure that timer interrupts cannot occur during the STOP instruction fetch cycle
3. Do not use ultra low power stop mode

Additional mask set errata can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/index.html