NXP Semiconductors
Engineering Bulletin

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NXP Vehicle Network Processor S32G3 - Migration Considerations from Rev 1.0 to Rev 1.1

by: NXP Semiconductors

1. Introduction

The purpose of this Engineering Bulletin is to summarize the changes to the latest Revision of the S32G3.

S32G3 Rev 1.1 incorporates errata fixes and other design improvements as detailed in this document.

Contents

2. S32G3 part identification updates

Identifier	S32G3 Rev 1.0	S32G3 Rev 1.1
Mask number	0P72B	1P72B
MIDR->MINOR_MASK	0b0	0b1
JTAG ID -> PRN	4’b0	4’b1

Updated BSDL files with the modified ‘IDCODE_REGISTER’ should be used with S32G3 Rev 1.1.

3. S32G3 Rev 1.1 enhancements over Rev 1.0

The S32G3 Rev 1.1 implements errata fixes and security related updates over Rev 1.0.

The following errata are fixed on S32G3 Rev 1.1:

a) ERR051271 - BootROM: Serial boot may take more than expected time to initialize

b) ERR051257 - BootROM: The boot sequence can hang if the QSPI interrupt pin transitions low during boot.

c) ERR051166 - Core: A Cortex-M7 application core can enter a hung state if an interrupt is received shortly after execution of a wait instruction.

d) ERR051303 – XRDC: PFE assigned Domain IDs not as documented

Please refer to the ‘Mask Set Errata for Mask 0P72B’ for applicable errata on S32G3 Rev 1.0 and ‘Mask Set Errata for Mask 1P72B’ for applicable errata on S32G3 Rev 1.1.

Security related updates: In addition to these errata fixes, the S32G3 Rev 1.1 implements an improved authentication scheme over IVT, ST_DCD, DCD, AppBL and the device specific HSE firmware image.

4. S32G3 hardware design consideration

This section provides details about the hardware considerations of the fixes done on the S32G3 Rev 1.1.

- **ERR051271**: The workaround to this errata requires you to generate an INV_RESET_B (invert of RESET_B) signal and tie it to BOOTMOD2 pin for serial boot mode. In the new Rev of silicon, this is no longer necessary. Hence you can remove the circuit on S32G3 Rev 1.1, and simply tie this pin to HIGH. For existing hardware, in case the workaround is already implemented, the external circuit to generate INV_RESET_B signal becomes a do not care and even if the output of this circuit is tied to the BOOTMOD2 pin the serial boot mode works as expected.
- **ERR051257**: The hardware workaround to this errata requires the user to disconnect the external ECC reporting signal coming from the QSPI flash from the S32G3 QSPI interrupt pin. This mechanism leads to the application losing the capability to sense the signal and take corrective action based on it. In the new Rev of silicon this dependency is removed and new hardware

designs can now connect the ECC out signal from the QSPI flash to S32G3 QSPI interrupt input pin.
In case the QSPI flash does not support ECC out signal or application does not intend to use it, the workaround requires the QSPI interrupt pin to be pulled high. It is no longer required for the S32G3 Rev 1.1. You can remove the pull up or use the pin for other requirements. For existing hardware with the pin pulled high, keeping the connection as it is has no impact.

5. S32G3 software considerations

This section provides details about the software considerations of the fixes implemented on the S32G3 Rev 1.1.

- **ERR051257**: The software workaround for this errata requires you to input a DCD that configures the QSPI interrupt pin to the default GPIO functionality. The BootROM in S32G3 Rev 1.1 no longer configures the QSPI interrupt pin and leaves it in the default GPIO mode. As such, the DCD steps become redundant and can be removed. For applications that have implemented the workaround you can decide to leave the DCD implementation as is. The DCD instructions become redundant in this case.
- **ERR051166:** The errata workaround requires application software to follow a set of instructions before any Cotrex-M7® executes a WFI/WFE instruction. A complementary set of instructions are also implemented on the debugger side. For the S32G3 Rev 1.1, this workaround is not necessary. As such, a S32G3 Rev 1.1 compliant debugger must be used and the application should also remove steps related to the workaround. Leaving the steps as it is in the application with the debugger not implementing the workaround can lead to debugger connect issues.
- **ERR051303:** The DID values for PFE HIF have changed on S32G3 Rev 1.1. The user application now uses the new DID values for any XRDC based isolation on the PFE HIF.

Security related updates: In addition to the errata fixes, the S32G3 Rev 1.1 will also operate with an updated set of system images. It also requires a new HSE firmware version to create these images. The change is reflected in the HSE boot data image GMAC generation service structure (hseBootDataImageSignSrv_t).

The device-specific HSE FW image structure (aka “blue FW image”) is also changed, however there is no change to the NXP distributed HSE FW image format (aka “pink FW image”). It should also be noted that the S32G3 Rev 1.1 will not be able to install HSE FW older than *x.**2.**x.x*. These devices must only be used with the HSE FW version *x.**2.**x.x* or later. The new HSE FW version on the other hand will be backwards compatible and be able to support the S32G3 Rev 1.0 for existing development purpose. NXP plans to qualify only S32G3 Rev 1.1 for production.

You must always ensure to check the release notes of NXP provided software to confirm if the latest Rev is supported by the software. Refer to the document “S32G Software Offering” from My NXP > Secure Files to obtain information on compatible NXP SW releases. For errata impact on various NXP SW deliverables, refer to the document ‘Analysis of NXP software - S32G3 Errata’ available from My NXP > Secure Files.

6. S32G3 tools considerations

This section provides details about the tools considerations of the fixes implemented on the S32G3 Rev 1.1.

- **ERR051166**: Please check with your debugger tool vendor for the correct version of the tool that will work with S32G3 Revision 1.1.
- **Security related updates:** The new authentication scheme requires you to provide a random vector (IV) with the system images IVT, ST_DCD, DCD and AppBL. The HSE service that computes GMAC over these system images also returns a random vector. All this requires a new IVT tool that can support insertion of these random vector with different system images. The updated IVT Tool will be available as part of S32DS 3.5 Update 1. In case a different tool is being used, the user must adapt the tool to these changes.

7. Reuse of existing evaluation boards for S32G3 Rev 1.1

There is no impact to the use of the S32G-VNP-EVB3 with S32G3 Rev 1.1 Silicon. You can simply remove the older version of silicon from the EVB socket and replace with the new version.

A new version of the RDB3 will be released (S32G-VNP-RDB3 Rev F) with the S32G3 Rev 1.1 part mounted on the board.

8. References

1. S32G3 Reference Manual
2. S32G3 Data Sheet
3. S32G3 Hardware Design Guide
4. Mask Set Errata for Mask 0P72B
5. Mask Set Errata for Mask 1P72B

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