TJA1421

LIN commander/responder transceiver

Rev. 1.0 — 4 November 2025 Product data sheet

1 General description

The TJA1421 provides the interface between a Local Interconnect Network (LIN) commander/responder protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle subnetworks using bit rates up to 20 kbit/s and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602:2021. The TJA1421 is backward-compatible with the TJA1021 and MC33662(B).

The transmit data stream generated by the protocol controller is converted by the TJA1421 via pin TXD into optimized bus signals shaped to minimize electromagnetic emissions (EME). The LIN bus output pin is pulled HIGH via an internal responder termination resistor. For a commander application, an external resistor in series with a diode should be connected between pin INH or pin VBAT and pin LIN. The receiver detects the receive data stream on the LIN bus input pin and transfers it via pin RXD to the microcontroller.

Power consumption is very low in Sleep mode. However, mode selection (via pin SLP_N) and remote wake-up (via the LIN bus) remain active.

2 Features and benefits

2.1 General

- Compliant with:
  - LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A
  - ISO 17987-4:2016 (12 V LIN)
  - SAE J2602:2021
- Very low current consumption in Sleep mode with local and remote wake-up
- Bit rates up to 20 kbit/s with optimized bus signal shaping
- Very low electromagnetic emissions (EME)
- High electromagnetic immunity (EMI)
- Passive behavior on LIN pin in unpowered state
- Option to control an external voltage regulator and/or switch commander termination via the INH output
- Input levels compatible with 1.8 V, 3.3 V and 5 V devices
- Integrated termination resistor for LIN responder applications
- Wake-up source recognition (local or remote)
- Battery undervoltage detection
- K-line compatible
- Pin-to-pin compatible with TJA1021 and MC33662(B)
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Available in SO8 and leadless HVSON8 package (3.0 mm × 3.0 mm) supporting Automated Optical Inspection (AOI) capabilities

2.2 Protection

- High ESD robustness on LIN and VBAT pins

- Bus, WAKE_N and battery pins protected against transients in automotive environments
- Bus terminal short-circuit proof to battery and ground
- TXD dominant timeout function
- Thermal protection

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1421AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1421ATK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1

4 Block diagram

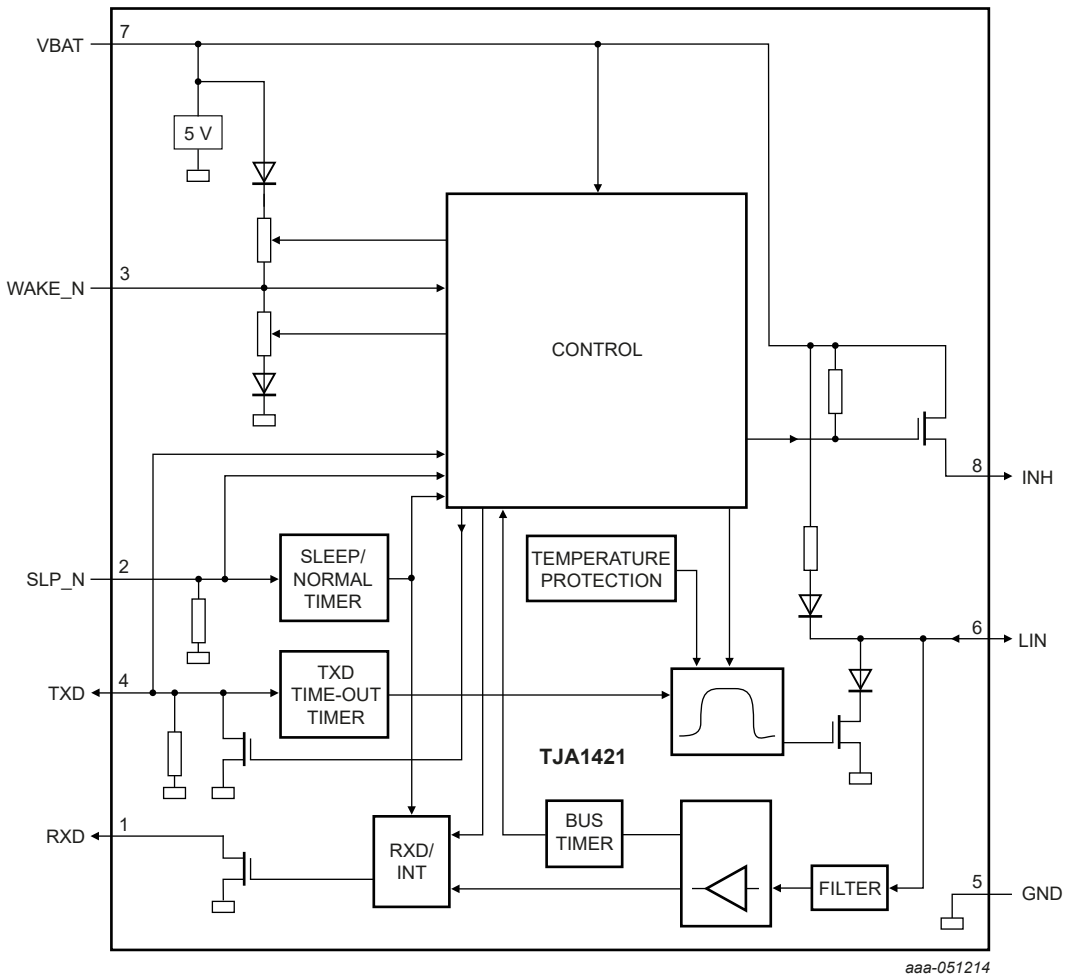


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

Figure 2. Pin configuration diagrams

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
RXD	1	O	receive data output; set LOW to signal a remote LIN wake-up event
SLP_N	2	I	sleep control input (active-LOW)
WAKE_N	3	AI	local wake-up input (active-LOW); negative edge triggered
TXD	4	IO	transmit data input; wake-up source flag output
GND	5[2]	G	ground
LIN	6	AIO	LIN bus line input/output
VBAT	7	P	battery supply voltage
INH	8	AO	inhibit output for controlling an external voltage regulator and/or switch commander termination; active-HIGH; activated in Normal and Standby modes

[1] Type description
- I: digital input
- O: digital output
- IO: digital input/output
- AI: analog input
- AI: analog input
- AO: analog output
- AIO: analog input/output
- P: power supply
- G: ground

[2] HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended solder the exposed center pad to board ground.

6 Functional description

6.1 LIN transceiver

The LIN transceiver (transmitter and receiver) is the interface between a LIN controller and the physical bus in a LIN network. In active state (Normal mode), a data stream fed to the TXD pin is converted into a LIN signal on the LIN pin. In the reverse direction, the LIN signal on the LIN pin is converted into a digital signal on pin RXD. The LIN transmitter and receiver conversion schemes are detailed in Table 3 and Table 4.

Table 3. LIN transmitter in Normal mode

pin TXD	pin LIN
HIGH	V_{LIN} recessive
LOW	V_{LIN} dominant[1]

[1] No exception or failure handling detected.

Table 4. LIN receiver in Normal mode

pin LIN	pin RXD
V_{LIN} recessive	HIGH
V_{LIN} dominant	LOW

6.2 Operating modes

Table 5 contains a summary of the available operating modes. A mode transition diagram is shown in Figure 3. When a mode change is initiated, it will be completed after transition time $t_{t(moch)}$. The terminology used in the mode transition diagram is defined in Table 6.

Table 5. LIN channel operating modes

Operating mode	Description
Reset	The device is deactivated
Standby	Standby mode is an intermediate state, entered after power on or in response to a local or remote wake-up request.
Sleep	Sleep mode is the low-power mode of the transceiver.
Normal	Normal mode provides full transmit and receive capabilities.

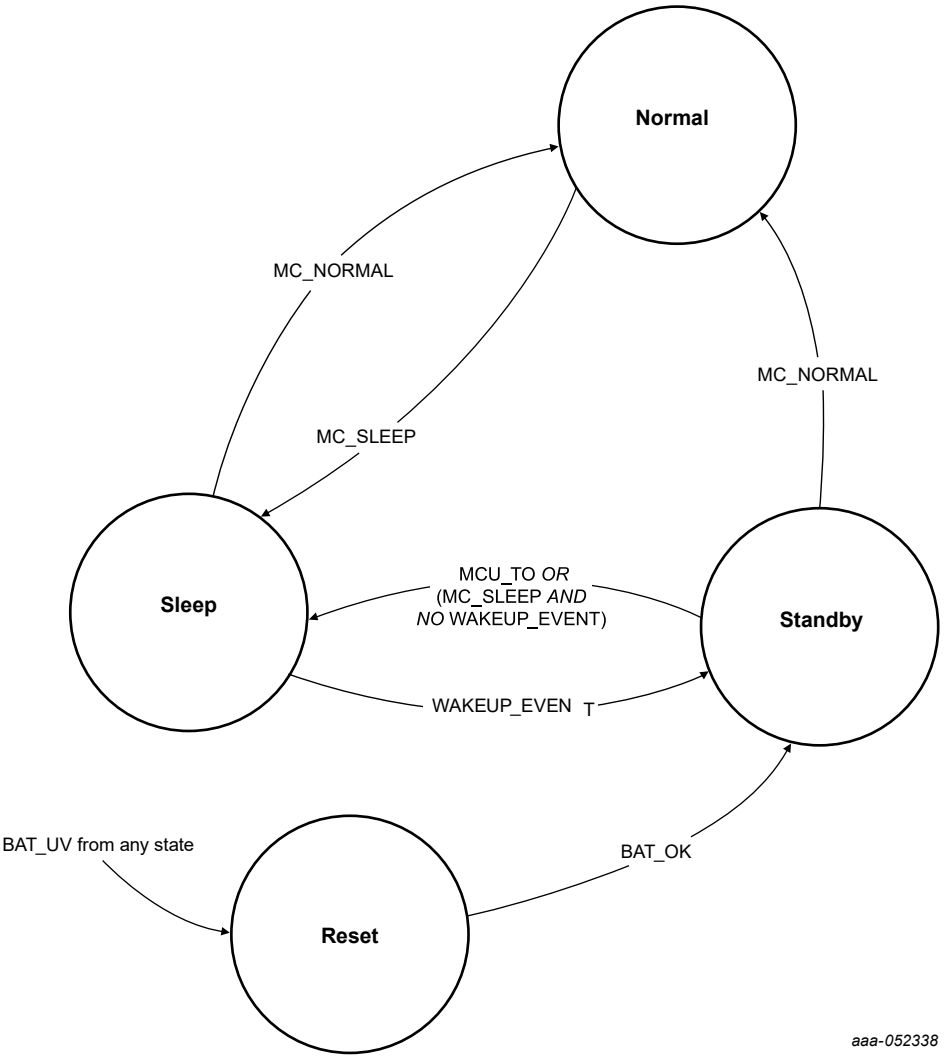


Figure 3. State transition diagram

Table 6. State diagram legend

Category	Abbreviation	Definition
VBAT pin status	BAT_UV	$V_{BAT} < V_{uvd(VBAT)}$ for $t > t_{det(uv)VBAT}$
	BAT_OK	($V_{BAT} > V_{uvd(VBAT)}$ for $t > t_{rec(uv)VBAT}$) for $t_{startup}$
Microcontroller timeout	MCU_TO	(SLP_N = LOW for $t > t_{fltr(IO)}$) for $t > t_{to(MCU)}$
Mode select	MC_NORMAL	(SLP_N = HIGH for $t > t_{fltr(IO)}$) for $t > t_{t(moch)}$
	MC_SLEEP	(SLP_N = LOW for $t > t_{fltr(IO)}$) for $t > t_{t(moch)}$
Wake-up	WAKEUP_EVENT	LIN bus wake-up pattern detected on LIN bus, local wake-up detected on pin WAKE_N, or power on

6.2.1 Pin and functional block states per operating mode

Table 7. Pin state per operating mode

Pin	Reset	Sleep	Standby	Normal
TXD	weak-pulldown	pull-down	pull-down if local wake-up; weak pull-down otherwise	pull-down
RXD	floating	floating	LOW	LOW if LIN bus dominant floating if LIN bus recessive
SLP_N	pull-down	pull-down	pull-down	pull-down
INH	floating	floating	HIGH	HIGH
LIN	$R_{responder}$	$R_{responder}$	$R_{responder}$	$R_{responder}$

Table 8. Functional state per System operating mode

Function	Reset	Sleep	Standby	Normal
LIN transceiver	off	off	off	on
LIN wake-up detection	off	on	off	off
Overtemperature detection	off	off	off	on
TXD dominant timeout	off	off	off	on
LIN short-circuit protection	off	off	off	on

6.3 LIN termination

Each node in a LIN network requires a termination network between the battery supply and the LIN pin. For the TJA1421, a fixed responder termination has been implemented.

6.4 INH pin

The TJA1421 contains an INH pin that indicates, when HIGH, that the device is in Standby or Normal mode (see Table 7). Pin INH could be used, for example, to control an external voltage regulator or commander termination (see Figure 6).

6.5 Mode control

The TJA1421 features a mode control pin, SLP_N:

- a LOW level on pin SLP_N triggers a transition from Normal mode to Sleep mode
- a HIGH level on pin SLP_N triggers a transition from Sleep or Standby mode to Normal mode

For further details, see Figure 3 and Table 6.

6.6 Wake-up detection

A wake-up event can be detected by the transceiver and reported to the host controller. The TJA1421 can detect the following wake-up events:

- battery power on: the supply voltage on pin VBAT exceeds the undervoltage detection threshold ($V_{uvd(VBAT)}$), causing the device to switch from Reset mode to Standby mode
- Local wake-up from Sleep mode via pin WAKE_N

- remote wake-up from Sleep mode via a dedicated wake-up pattern on the LIN bus

A wake-up event causes the device to enter (or remain in) Standby mode and to signal this event with a LOW level on pin RXD. Pin INH is HIGH. The wake-up event is cleared when the device enters Normal mode or in the event of a microcontroller timeout, MCU_TO (see Table 6).

6.6.1 Local wake-up via WAKE_N pin

A falling edge on pin WAKE_N followed by a LOW level lasting for a duration of at least t_{WAKE} triggers a local wake-up.

To minimize current consumption, the internal bias voltage follows the logic state on the pin after a delay of t_{WAKE}. A HIGH level on pin WAKE_N is followed by an internal pull-up to an internal 5 V regulator. A LOW level on pin WAKE_N is followed by an internal pull-down towards GND.

When the internal pull-up is active, pin WAKE_N sources a current, $I_{O(WAKE\_N)}$, that depends on the voltage on the pin. When the internal pull-down is active, pin WAKE_N sinks a current of $I_{I(WAKE\_N)}$, that depends on the voltage on the pin.

In applications that do not make use of the local wake-up facility, it is recommended to connect pin WAKE_N to GND for optimal EMI performance.

6.6.2 LIN bus wake-up pattern

The following LIN bus pattern is interpreted as a LIN bus wake-up request:

- a dominant phase of at least $t_{wake(dom)LIN}$ followed by
- a dominant-to-recessive edge

The wake-up pattern is shown in Figure 4.

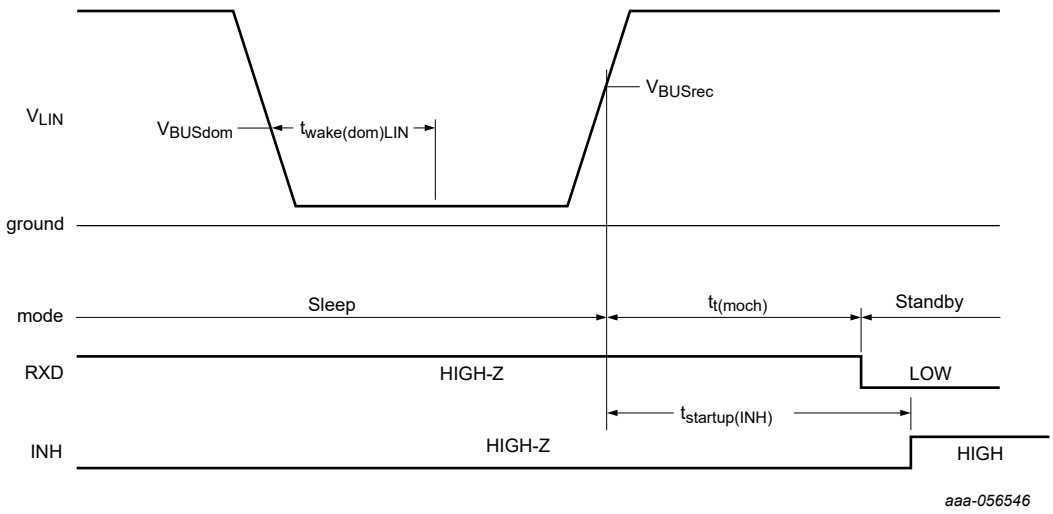


Figure 4. Principle of a LIN wake-up event via LIN bus

6.6.3 Wake-up source recognition

The TJA1421 can distinguish between a local wake-up request on pin WAKE_N and a remote wake-up request via a wake-up pattern (an internal wake-up source flag is set when a local wake-up request is detected). A weak pulldown on pin TXD indicates a remote wake-up request; a strong pulldown on pin TXD indicates a local wake-up request.

The wake-up request (signaled on pin RXD) and wake-up source flag are reset when the SLP_N is forced HIGH.

6.7 Exception and failure handling

6.7.1 TXD activation

To prevent uncontrolled transmission on the LIN bus after entering Normal mode or recovering from an overtemperature condition ($t_j < T_{rel(otp)}$), the LIN transmitter is not activated until a HIGH level is detected on the TXD pin.

6.7.2 TXD dominant timeout

A TXD dominant timeout timer is started when a falling edge is detected on pin TXD.

In Normal mode, a LOW level on pin TXD persisting longer than $t_{to(dom)TXD}$ releases the LIN bus to recessive state, allowing the bus to be used by other nodes. The timer is reset when TXD goes high again.

6.7.3 LIN shorted to battery supply

When a LIN pin is shorted to the battery supply, the transceiver is unable to drive the LIN bus dominant when pin TXD is set LOW in Normal mode. When this happens:

- the transmitter limits the current through pin LIN to GND to I_{BUS_LIM},
- if the LIN pin remains recessive for $t > t_{det(sc)LIN}$ while TXD is LOW, a failure is assumed and the transmitter is deactivated (and remains deactivated as long as TXD is LOW)

The transmitter is re-activated when TXD goes HIGH again.

6.7.4 V_{BAT} undervoltage

When the supply voltage on pin VBAT drops below the undervoltage detection threshold for $t > t_{det(uv)VBAT}$ (BAT_UV), the device is deactivated and enters Reset mode.

6.7.5 Loss of battery supply or GND

In the case of a loss of battery supply or GND, a BAT_UV (see Table 6) condition applies and the device enters Reset mode.

6.7.6 V_{BAT} overvoltage

Currents injected into the battery line in a low-power mode might charge the battery capacitor beyond the limiting value specified for pin VBAT. To mitigate the risk of an overvoltage, the device activates an additional load current ($I_{BAT(add)}$) when the voltage on pin VBAT exceeds the maximum specified operating voltage.

6.7.7 Overtemperature

When an overtemperature condition ($T_j > T_{sd(otp)}$) is detected, the LIN transmitter is deactivated and the bus is released to recessive state. When the device recovers from the overtemperature event ($T_j < T_{rel(otp)}$), the LIN transmitter is reactivated.

6.7.8 MCU reaction timeout

When the device enters Standby mode, a dedicated MCU reaction timeout timer is started. If a Normal mode command (SLP_N = HIGH) is not received within $t_{to(MCU)}$, the device clears the wake event, switches to Sleep mode and waits for the next wake-up request (see Figure 3). The MCU reaction timeout timer is reset when a Normal mode command is received.

7 Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pin VBAT	–0.3	+40	V
		pin INH	–0.3	V_{BAT} + 0.3[2]	V
		pin WAKE_N with respect to any other pin	–40	+40	V
		pins TXD, RXD, SLP_N	–0.3	+6[3]	V
		pin LIN with respect to any other pin	–40	+40	V
I_{INH}	output current on pin INH		–40	0	mA
V_{ESD}	electrostatic discharge voltage	IEC61000-4-2 (150 pF, 330 Ω) discharge circuit[4]			
		on pin LIN; on pin VBAT with 100 nF capacitor; on pin WAKE_N with 3 kΩ series resistor	–6	+6	kV
		Human Body Model (HBM)			
		on pins TXD, RXD, SLP_N[5]	–4	+4	kV
		on pins VBAT, INH, WAKE_N[6]	–4	+4	kV
		on pin LIN[7]	–8	+8	kV
		Charged Device Model[8]			
		on corner pins, only TJA1421AT	–750	+750	V
		on any other pin	–500	+500	V
T_{vj}	virtual junction temperature	[9]	–40	+150	°C
T_{stg}	storage temperature	[10]	–55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] Absolute maximum rating of 40 V.
[3] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.
[4] Verified by an external test house according to IEC TS 62228, Section 4.3.
[5] According to AEC-Q100-002.
[6] Pins stressed to reference group containing all grounds, emulating the application circuit (Figure 6). HBM pulse as specified in AEC-Q100-002 used.
[7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 6). HBM pulse as specified in AEC-Q100-002 used.
[8] According to AEC-Q100-011.
[9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[10] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8 Thermal characteristics

Table 10. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8	103	K/W
		HVSON8	59	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	HVSON8	20	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO8	17	K/W
		HVSON8	9	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer.

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

9 Static characteristics

Table 11. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.4 V to 40 V; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{BAT}	battery supply voltage		5.4	—	28	V
I_{BAT}	battery supply current	LIN channel active and recessive; Normal mode; $V_{INH} = V_{BAT}$; V_{TXD} = HIGH; $V_{LIN} = V_{BAT}$; V_{BAT} < 28 V [2]	—	—	3	mA
		LIN channel active and dominant; Normal mode; $V_{INH} = V_{BAT}$; V_{TXD} = LOW; V_{BAT} < 28 V [2]	—	—	4.5	mA
		Sleep or Standby mode; $V_{LIN} = V_{BAT}$; V_{BAT} < 28 V [2]				
		T_{vj} = -40 °C to +85 °C [2]	—	—	16	µA
		T_{vj} = -40 °C to +150 °C [2]	—	10	28	µA
$I_{BAT(add)}$	additional battery supply current	Sleep or Standby mode; $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; V_{BAT} > 28 V [2]	—	—	1.8	mA
Supply undervoltage; pin VBAT						
V_{uvd}	undervoltage detection voltage		4.8	—	5.4	V
Sleep control input: SLP_N						
$V_{th(sw)}$	switching threshold voltage	HIGH [2]	—	—	1.26	V
		LOW [2]	0.8	—	—	V

Table 11. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.4 V to 40 V; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(sw)hys}$	switching threshold voltage hysteresis	[2]	35	—	—	mV
R_{pd}	pull-down resistance	on pin SLP_N	20	—	80	kΩ
LIN transmit data input: TXD						
$V_{th(sw)}$	switching threshold voltage	HIGH	—	—	1.26	V
		LOW	0.8	—	—	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		35	—	—	mV
I_{OL}	LOW-level output current	Standby mode after local wake-up; V_{TXD} = 0.4 V	1	—	10	mA
R_{pd}	pull-down resistance	$V_{BAT} > V_{uvd(VBAT)}$; in all modes except in Standby mode after local wake-up	350	—	1000	kΩ
LIN receive data output; pin RXD						
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	1	—	10	mA
$I_{LO(off)}$	off-state output leakage current		–5	—	+5	µA
Inhibit output; pin INH						
$R_{sw(INH)}$	inhibit switch-on resistance	I_{INH} = -15 mA; V_{BAT} = 12 V; Normal or Standby mode	—	20	50	Ω
I_{LI}	input leakage current	V_{BAT} = 28 V; Sleep or Reset mode	–5	—	+5	µA
LIN bus; pin LIN						
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LIN} = 18 V; V_{TXD} = 0 V	40	—	200	mA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	V_{BAT} = 12 V; V_{LIN} = 0 V; V_{TXD} = HIGH	–1	—	—	mA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	8 V < V_{BAT} < 28 V; 8 V < V_{LIN} < 28 V; $V_{LIN} \geq V_{BAT}$; V_{TXD} = HIGH	—	—	20	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	$V_{BAT} = V_{GND}$ = 12 V; 0 V < V_{LIN} < 18 V;	–1	—	+1	mA
		[2] $V_{BAT} = V_{GND}$ = 12 V; 0 V < V_{LIN} < 28 V;	–1.5	—	+1.5	mA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; 0 V < V_{LIN} < 28 V	–50	—	50	µA
V_{BUSdom}	receiver dominant state	8 V < V_{LIN} < 28V	—	—	0.4V_{BAT}	V
V_{BUSrec}	receiver recessive state	8 V < V_{LIN} < 28V	0.6V_{BAT}	—	—	V

Table 11. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.4 V to 40 V; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{th_rec} + V_{th_dom}) / 2; 8 V ≤ V_{LIN} < 28 V [3]	0.475V_{BAT}	0.5V_{BAT}	0.525V_{BAT}	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = (V_{th_rec} - V_{th_dom}); 8 V < V_{LIN} < 28 V [3]	—	—	0.175V_{BAT}	V
$V_{SerDiode}$	voltage drop at the serial diodes	in pull-up path with $R_{responder}$; $I_{SerDiode}$ = 315 µA	0.4	—	1.0	V
$R_{responder}$	responder resistance	V_{BAT} < 28 V	27.66	—	48	kΩ
C_{LIN}	capacitance on pin LIN	[2]	—	—	20	pF
Local wake input; pin WAKE_N						
I_I	input current	internal pull-down active; V_{WAKE_N} = $V_{th(wake)max}$	—	—	19	µA
I_O	output current	internal pull-up active				
		V_{WAKE_N} = $V_{th(wake)min}$	–21	—	—	µA
		V_{WAKE_N} = $V_{th(wake)max}$	—	—	–1	µA
$V_{th(wake)}$	wake-up threshold voltage		2	—	2.8	V
V_{hys}	hysteresis voltage		90	—	—	mV
Thermal shutdown						
$T_{sd(otp)}$	overtemperature protection shutdown temperature	[2]	180	—	200	°C
$T_{rel(otp)}$	overtemperature protection release temperature	[2]	175	—	195	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

10 Dynamic characteristics

Table 12. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.4 V to 40 V; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; unless otherwise specified[1].

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
Duty cycles; pin LIN						
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 18 V [2] [3] [4] [5]	0.396	—	—	
		$V_{th(rec)(max)}$ = 0.665 x V_{BAT}; $V_{th(dom)(max)}$ = 0.499 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.5 V to 7 V [2] [3] [4] [5]	0.396	—	—	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V [2] [3] [4] [5]	—	—	0.581	
		$V_{th(rec)(min)}$ = 0.496 x V_{BAT}; $V_{th(dom)(min)}$ = 0.361 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.5 V to 7.6 V [2] [3] [4] [5]	—	—	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V [2] [3] [4] [5]	0.417	—	—	
		$V_{th(rec)(max)}$ = 0.665 x V_{BAT}; $V_{th(dom)(max)}$ = 0.499 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.5 V to 7 V [2] [3] [4] [5]	0.417	—	—	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 18 V [2] [3] [4] [5]	—	—	0.590	
		$V_{th(rec)(min)}$ = 0.496 x V_{BAT}; $V_{th(dom)(min)}$ = 0.361 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.5 V to 7.6 V [2] [3] [4] [5]	—	—	0.590	
LIN receiver; pin LIN; see Figure 4, Figure 5, and Figure 7						
t_{rx_pd}	receiver propagation delay	rising and falling edge; C_{RXD} = 20 pF				
		7 V ≤ V_{BAT} < 28 V	—	—	6	µs
		5.4 V ≤ V_{BAT} < 7 V [2]	—	—	6.5	µs
t_{rx_sym}	receiver propagation delay symmetry	rising edge with respect to falling edge; C_{RXD} = 20 pF	–2	—	+2	µs

Table 12. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.4 V to 40 V; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; unless otherwise specified[1].

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(dom)LIN}$	LIN dominant wake-up time	[2] [6]	30	—	150	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	timer started at falling edge on TXD; V_{TXD} = 0 V [2] [7]	5	—	8.6	ms
$t_{det(sc)LIN}$	LIN short-circuit detection time	Normal mode, V_{TXD} = 0 V [2] [8]	40	50	60	µs
Mode transition						
$t_{t(moch)}$	mode change transition time	Normal, Standby,Sleep mode [2]	—	—	50	µs
$t_{startup}$	start-up time	$V_{BAT} > V_{uvd(VBAT)}$ [2]	—	—	1	ms
$t_{to(MCU)}$	MCU timeout time	Standby mode [7] [2]	940	—	1300	ms
$t_{fltr(IO)}$	IO filter time	on pin SLP_N [2]	1	—	5	µs
Undervoltage detection on pin VBAT						
$t_{det(uv)}$	undervoltage detection time	$V_{BAT} < V_{uvd(VBAT)}$ - 100 mV overdrive [2]	—	—	30	µs
$t_{rec(uv)}$	undervoltage recovery time	$V_{BAT} > V_{uvd(VBAT)}$ + 100 mV overdrive [2]	—	—	50	µs
Wake-up via WAKE_N						
t_{WAKE}	wake-up time	in response to a falling edge on WAKE_N [2] [9]	20	—	50	µs
Inhibit output; pin INH						
$t_{startup(INH)}$	INH start-up time	after local or remote wake-up [2]	—	—	50	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Not tested in production; guaranteed by design.

[3] $\delta 1, \delta 3 = \frac{t_{bus(rec)min}}{2 \times t_{bit}}$; $\delta 2, \delta 4 = \frac{t_{bus(rec)max}}{2 \times t_{bit}}$; see Figure 5

[4] Bus load conditions: $R_{commander}$ = off; C_{LIN} = 1 nF and R_{LIN} = 1 kΩ; C_{LIN} = 6.8 nF and R_{LIN} = 660 Ω; C_{LIN} = 10 nF and R_{LIN} = 500 Ω.

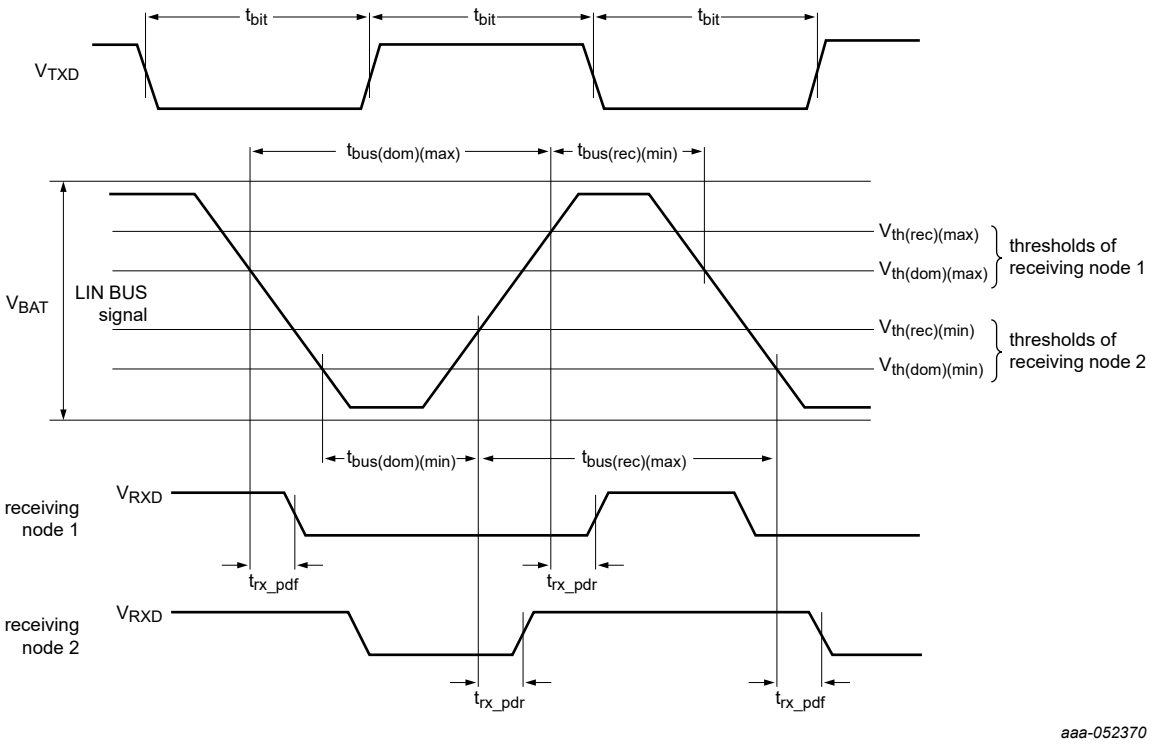
[5] See timing diagram in Figure 5.

[6] A falling edge on pin LIN, folllowed by LOW level of at least $t_{wake(dom)LIN}$, max, followed by a rising edge on pin LIN is guranteed to trigger a remote wake-up (see Section 6.6.1). A LOW level of less than $t_{wake(dom)LIN}$, min will not trigger a wake-up event.

[7] Time-out is guaranteed to have been triggered after max and will not be triggered before min.

[8] Detection is guaranteed to occur after $t_{det(SC)LIN}$, max and not to occur before $t_{det(SC)LIN}$, min.

[9] Wake-up is guaranteed to occur after t_{WAKE},max and not to occur before t_{WAKE},min.



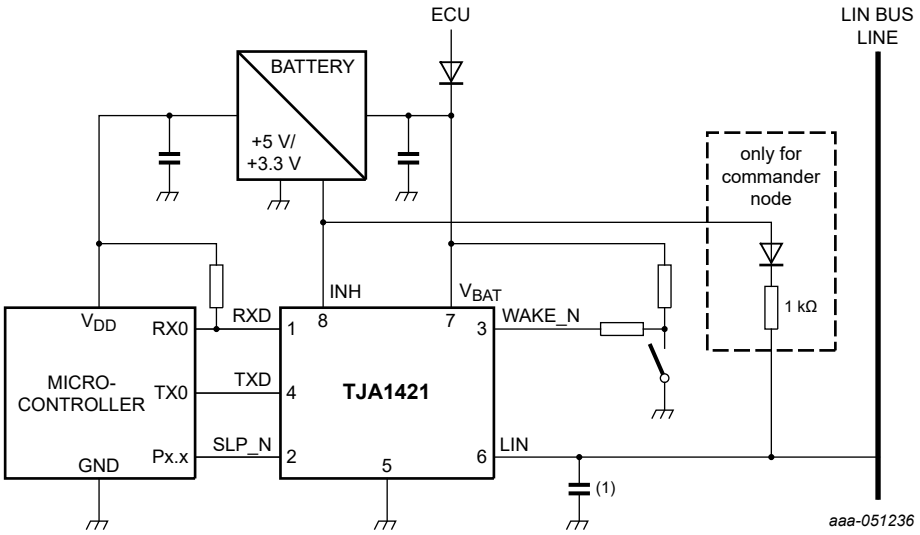
t_{rx_pdr} and t_{rx_pdf} depict the rising and falling edgies of paramter t_{rx_pd}.

Figure 5. Timing diagram of LIN duty cycle

11 Application information

11.1 Application diagram

The minimum external circuitry needed with the TJA1421 is shown in Figure 6. Further information on external components and PCB layout can be found in the Application Hints document (see Section 11.2).



(1) Typically specified by the car manufacturer

Figure 6. Application diagram

11.2 Application notes

Further information on the application of the TJA1421 can be found in NXP application hints AN14837 *LIN Transceivers TJA1421 and TJA1425*.

12 Test information

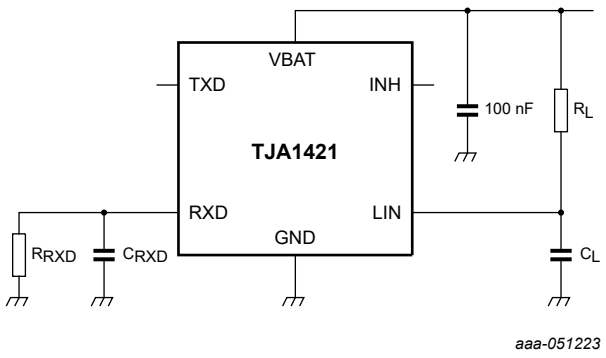


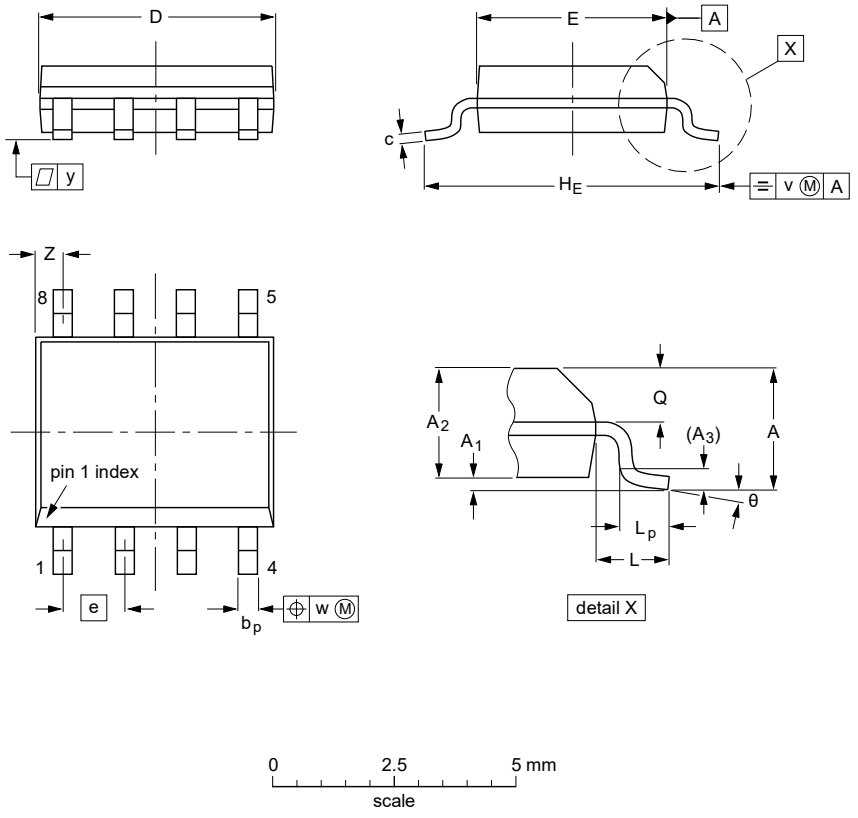
Figure 7. Timing test circuit for LIN transceiver

13 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

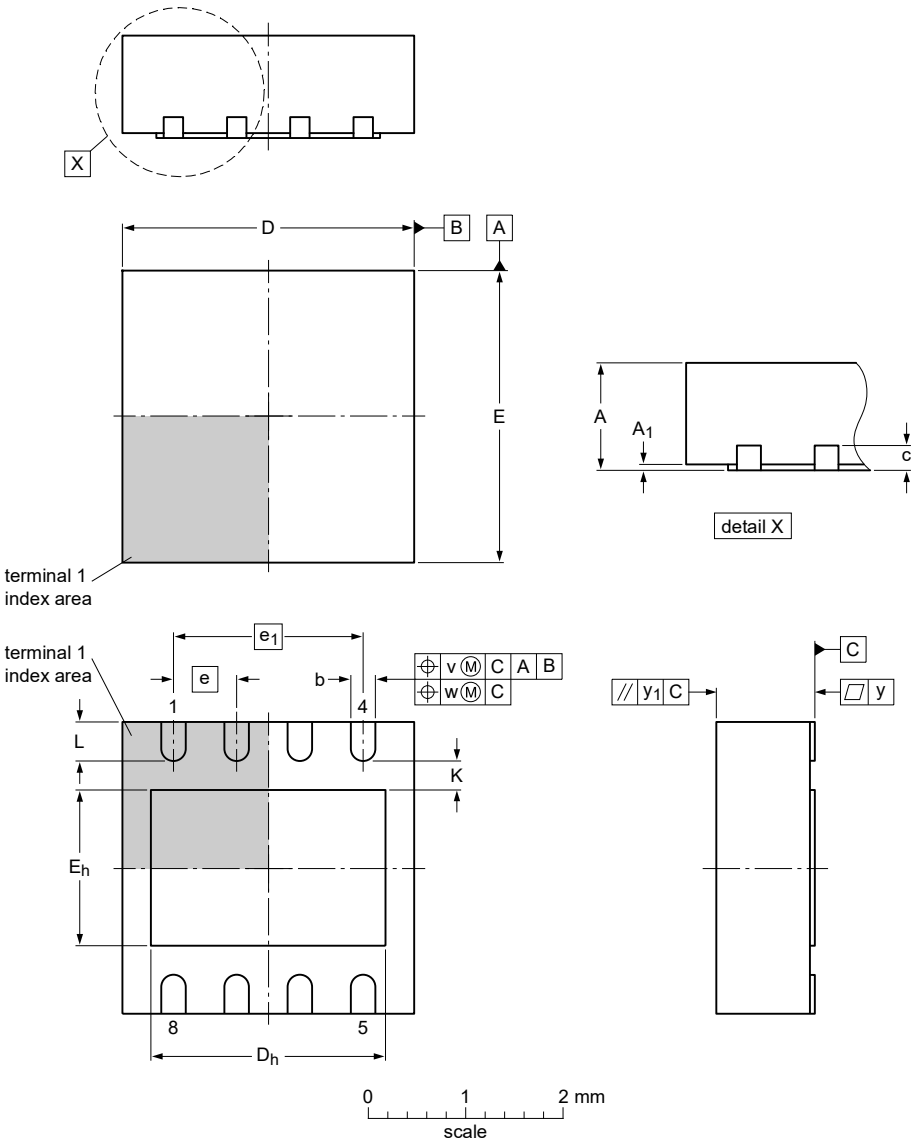
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Figure 9. Package outline SOT782-1 (HVSON8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and Table 14

Table 13. SnPb eutectic process (from J-STD-020D)

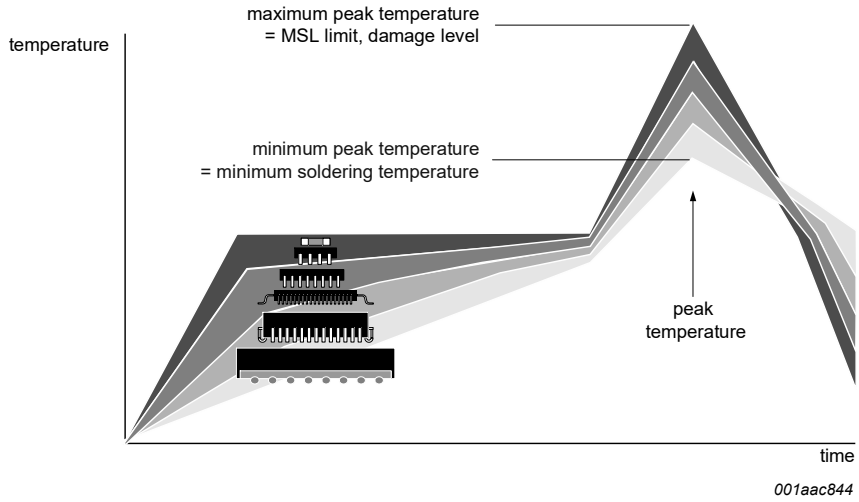
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Figure 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Revision history

Table 15. Revision history

Document ID	Release date	Description
TJA1421 v1.0	04 November 2025	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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