TJA1043

High-speed CAN transceiver

Rev. 7.0 — 29 September 2026 Product data sheet

1 General description

The TJA1043 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1043 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1041A. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, very low power consumption, and passive behavior when the supply voltage is turned off. Advanced features include:

- Low-power management controls the power supply throughout the node while supporting local and remote wake-up with wake-up source recognition
- Several protection and diagnostic functions including bus line short-circuit detection and battery connection detection
- Can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

The TJA1043 implements the CAN physical layer as defined in ISO 11898-2:2026 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The TJA1043H provides support for 48 V systems.

These features make the TJA1043 the ideal choice for high speed CAN networks containing nodes that need to be available all times, even when the internal V_{IO} and V_{CC} supplies are switched off.

2 Features and benefits

2.1 General

- ISO 11898-2:2026 and SAE J2284-1 to SAE J2284-5 and SAE-J1939-14[1] compliant
- Loop delay symmetry timing enables reliable communication at data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V, 24 V, and 48 V (TJA1043HT(K) only) systems
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI), tested according to EMC standards IEC TS62228
- VIO input allows for direct interfacing with 3.3 V and 5 V microcontrollers
- SPLIT voltage output for stabilizing the recessive bus level
- Listen-only mode for node diagnosis and failure containment
- Available in SO14 and HVSON14 packages
- Leadless HVSON14 package (3.0 mm x 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- AEC-Q100 qualified

1 Compliant with the exception of parameters $V_{CM(STEP)}$ and $V_{CM(PP)}$; intended as an indication of emission performance. Note that the device fulfills the EMC requirements, as evidenced through IBEE reports available on request.

2.2 Low-power management

- Very low current Standby and Sleep modes, with local and remote wake-up
- Capability to power down the entire node while supporting local, remote and host wake-up
- Wake-up source recognition
- Transceiver disengages from the bus (zero load) when V_{BAT} absent
- Functional behavior predictable under all supply conditions

2.3 Protection and diagnosis (detection and signalling)

- High ESD handling capability on the bus pins
- Bus pins and VBAT protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function with diagnosis
- TXD-to-RXD short-circuit handler with diagnosis
- Thermal protection with diagnosis
- Undervoltage detection and recovery on pins VCC, VIO and VBAT
- Bus line short-circuit diagnosis
- Bus dominant clamping diagnosis
- Cold start diagnosis (first battery connection)

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	—	5.5	V
V_{IO}	supply voltage on pin VIO		2.8	—	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		3	3.5	4.3	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	V_{BAT} or V_{CC} > 4.5 V	0.8	1.8	2.5	V
I_{CC}	supply current	Standby or Sleep mode	0	0.75	2	µA
		Normal or Listen-only mode; bus recessive	3	6	9	mA
		Normal mode; bus dominant	30	48	65	mA
I_{IO}	supply current on pin VIO	Standby or Sleep mode	0	1	4	µA
		Normal or Listen-only mode; $V_{TXD} = V_{IO}$ (recessive)	0	1	4	µA
		Normal mode; V_{TXD} = 0 V (dominant)	—	150	500	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	–8	—	+8	kV
V_{CANH}	voltage on pin CANH		–58	—	+58	V
V_{CANL}	voltage on pin CANL		–58	—	+58	V
T_{vj}	virtual junction temperature		–40	—	+150	°C

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4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1043T TJA1043HT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1043TK TJA1043HTK	HVSON14	plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

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5 Block diagram

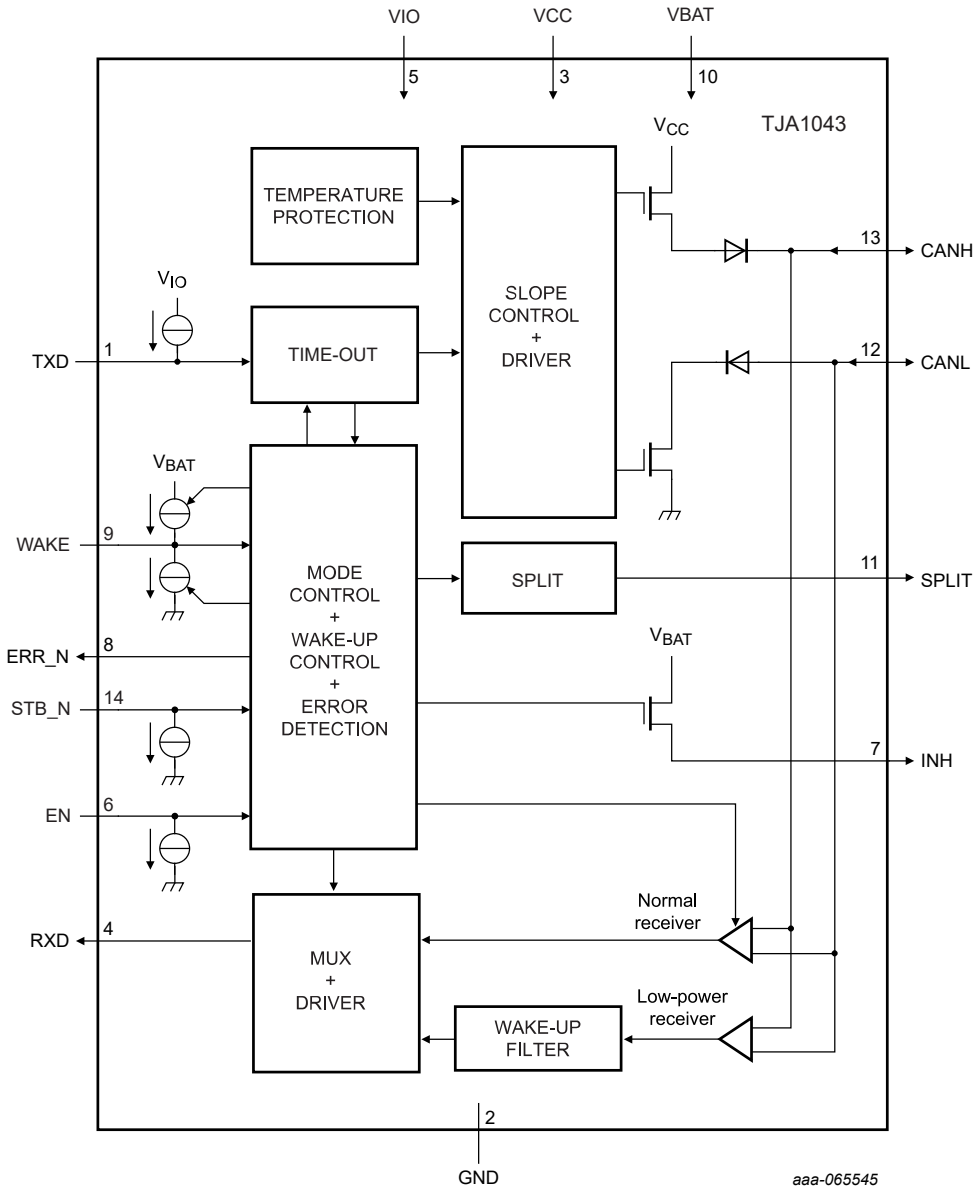

Figure 1. Block diagram

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6 Pinning information

6.1 Pinning

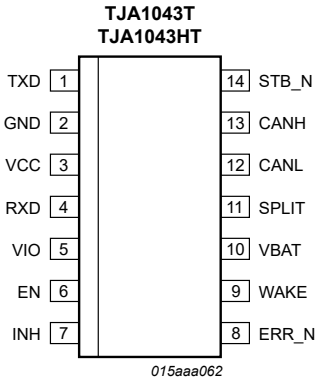

Figure 2. Pin configuration diagram: SO14

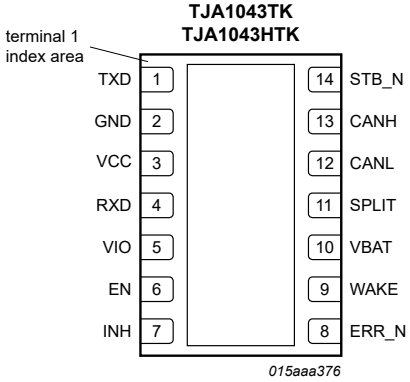

Figure 3. Pin configuration diagram: HVSON14

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND[2]	2	G	ground supply
VCC	3	P	transceiver supply voltage
RXD	4	O	receive data output; reads out data from the bus lines
VIO	5	P	supply voltage for I/O level adapter
EN	6	I	enable control input
INH	7	AO	inhibit output for switching external voltage regulators
ERR_N	8	O	error and power-on indication output (active LOW)
WAKE	9	AI	local wake-up input
VBAT	10	P	battery supply voltage
SPLIT	11	AO	common-mode stabilization output
CANL	12	AIO	LOW-level CAN-bus line
CANH	13	AIO	HIGH-level CAN-bus line
STB_N	14	I	standby control input (active LOW)

[1] Type description
- I: digital input
- O: digital output
- AI: analog input
- AIO: analog input/output
- AO: analog output
- P: power supply
- G: ground

[2] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

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7 Functional description

The TJA1043 is a stand-alone high-speed CAN transceiver with a number of operating modes, fail-safe features and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver combines the functionality of the TJA1041A with improved EMC and ESD capability and quiescent current performance. Improved slope control and high DC handling capability on the bus pins provide additional application flexibility.

7.1 Supply

Table 4. Supply description

Supply pin	Supply	Description
VBAT	V_{BAT}	Main supply for the device, needed for all internal processes; supplies the wake-up receiver and local wake-up
VCC	V_{CC}	Supply for the CAN transmitter, normal receiver, and for busbiasing
VIO	V_{IO}	Supply and reference level for the digital interface pins TXD, RXD, EN, STB_N, and ERR_N

7.2 Operating modes

The TJA1043 supports five operating modes. Control pins STB_N and EN are used to select the operating mode. Switching between modes allows access to a number of diagnostics flags via pin ERR_N. Table 5 describes how to switch between modes. Figure 4 illustrates the mode transitions when V_{CC}, V_{IO} and V_{BAT} are valid.

Table 5. Operating mode selection

Internal flags			Control pins		Operating mode	Pin INH
UV_{NOM}[1]	UV_{BAT}	Wake[2]	STB_N[3]	EN		
From Normal, Listen-only, Standby and Go-to-Sleep modes						
set	X	X	X	X	Sleep mode	floating
cleared	set	X	HIGH	X	Standby mode	HIGH
cleared	X	set	LOW	X	Standby mode	HIGH
cleared	X	cleared	LOW	LOW	Standby mode	HIGH
cleared	X	cleared	LOW	HIGH	Go-to-Sleep mode[4]	HIGH[4]
cleared	cleared	X	HIGH	LOW	Listen-only mode	HIGH
cleared	cleared	X	HIGH	HIGH	Normal mode	HIGH
From Sleep mode						
set	X	X	X	X	Sleep mode	floating
cleared	set	X	HIGH	X	Standby mode	HIGH
cleared	X	set	LOW	X	Standby mode	HIGH
cleared	X	cleared	LOW	X	Sleep mode	floating
cleared	cleared	X	HIGH	LOW	Listen-only mode	HIGH
cleared	cleared	X	HIGH	HIGH	Normal mode	HIGH

[1] Setting the UV_{NOM} flag will clear the WAKE flag.
[2] Setting the Wake flag will clear the UV_{NOM} flag.
[3] A LOW-to-HIGH transition on pin STB_N will clear the UV_{NOM} flag
[4] After the minimum hold time, in Go-to-Sleep mode, $t_{h(min)}$, the transceiver will enter Sleep mode and pin INH will be set floating.

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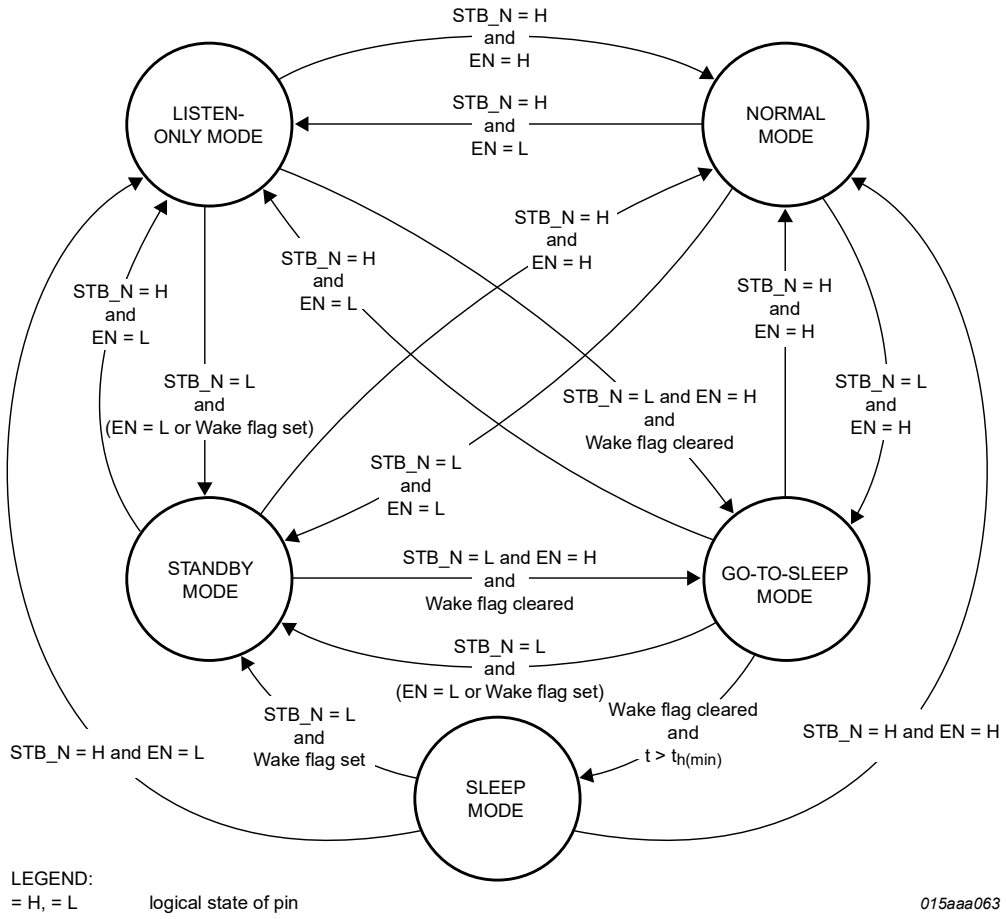

Figure 4. Mode transitions when valid V_{CC}, V_{IO} and V_{BAT} voltages are present

7.2.1 Normal mode

In Normal mode, the transceiver can transmit and receive data via the bus lines CANH and CANL. See Figure 1 for the block diagram. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. The bus pins are biased to $0.5V_{CC}$ (via R_i). Pin INH is active, so voltage regulators controlled by pin INH (see Figure 8) will be active too.

7.2.2 Listen-only mode

In Listen-only mode, the transceiver's transmitter is disabled, effectively providing a transceiver listen-only feature. The receiver will still convert the analog bus signal on pins CANH and CANL into digital data, available for output on pin RXD. As in Normal mode, the bus pins are biased at $0.5V_{CC}$ and pin INH remains active.

7.2.3 Standby mode

Standby mode is the TJA1043's first-level power saving mode, offering reduced current consumption. In Standby mode, the transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor bus activity. The bus pins are biased at ground level (via R_i). Pin INH is still active, so voltage regulators controlled by this pin will also be active.

Pins RXD and ERR_N will reflect any active wake-up requests (provided that V_{IO} and V_{BAT} are present).

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7.2.4 Go-to-Sleep mode

Go-to-Sleep mode is the controlled route for entering Sleep mode. In Go-to-Sleep mode, the transceiver behaves as in Standby mode, with the addition that a go-to-sleep command is issued to the transceiver. The transceiver will remain in Go-to-Sleep mode for the minimum hold time ($t_{h(min)}$) before entering Sleep mode. The transceiver will not enter Sleep mode if the state of pin STB_N or pin EN is changed or if the Wake flag is set before $t_{h(min)}$ has elapsed.

7.2.5 Sleep mode

Sleep mode is second-level power saving mode of the TJA1043. Sleep mode is entered via Go-to-Sleep mode, and also when the undervoltage detection time on either V_{CC} or V_{IO} elapses before the relevant voltage level has recovered. In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set floating. Voltage regulators controlled by this pin will be switched off, and the current into pin VBAT will be reduced to a minimum. Pins STB_N, EN and the Wake flag can be used to wake up a node from Sleep mode. See Table 5.

7.3 Internal flags

The TJA1043 makes use of seven internal flags for its fail-safe fallback mode control and system diagnosis support. Five of these flags can be polled by the controller via pin ERR_N. Which flag is available on pin ERR_N at any time depends on the active operating mode and on a number of other conditions. Table 6 describes how to access these flags.

Table 6. Accessing internal flags via pin ERR_N

Internal flag	Flag is available on pin ERR_N[1]	Flag is cleared
UV_{NOM}	no	by setting the Pwon or Wake flags, by a LOW-to-HIGH transition on STB_N or when both V_{IO} and V_{CC} have recovered.
UV_{BAT}	no	when V_{BAT} has recovered
Pwon	in Listen-only mode (coming from Standby mode, Go-to-Sleep mode, or Sleep mode)	on entering Normal mode
Wake	in Standby mode, Go-to-Sleep mode, and Sleep mode (provided that V_{IO} and V_{BAT} are present)	on entering Normal mode or by setting the UV_{NOM} flag
Wake-up source	in Normal mode (before the fourth dominant-to-recessive edge on pin TXD[2]	on leaving Normal mode
Bus failure	in Normal mode (after the fourth dominant-to-recessive edge on pin TXD)[2]	on re-entering Normal mode or by setting the Pwon flag
Local failure	in Listen-only mode (coming from Normal mode)	on entering Normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved) or by setting the Pwon flag

[1] Pin ERR_N is an active-LOW output, so a LOW-level indicates a set flag and a HIGH-level indicates a cleared flag. Allow pin ERR_N to stabilize for at least 8 µs after changing operating modes.
[2] Allow for a TXD dominant time of at least 4 µs per dominant-recessive cycle.

7.3.1 UV_{NOM} flag

UV_{NOM} is the V_{CC} and V_{IO} undervoltage detection flag. The flag is set when the voltage on pin VCC drops below the V_{CC} undervoltage detection voltage, $V_{uvd(VCC)}$, for longer than the undervoltage detection time, $t_{det(uv)}$, or when the voltage on pin V_{IO} drops below $V_{uvd(VIO)}$ for longer than $t_{det(uv)}$. When the UV_{NOM} flag is set, the

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transceiver enters Sleep mode to save power and to ensure the bus is not disturbed. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding any extra power consumption that might be generated as a result of a short-circuit condition.

Any wake-up request, setting the Pwon flag or a LOW-to-HIGH transition on STB_N will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated (at least until UV_{NOM} is set again). UV_{NOM} will also be cleared if both V_{CC} and V_{IO} recover for longer than the undervoltage recovery time, $t_{rec(uv)}$. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN. See Table 5.

7.3.2 UV_{BAT} flag

UV_{BAT} is the V_{BAT} undervoltage detection flag. This flag is set when the voltage on pin VBAT drops below $V_{uvd(VBAT)}$. When UV_{BAT} is set, the transceiver will try to enter Standby mode to save power and will disengage from the bus (zero load). UV_{BAT} is cleared when the voltage on pin VBAT recovers. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN. See Table 5.

7.3.3 Pwon flag

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin VBAT recovers after previously dropping below $V_{uvd(VBAT)}$ (usually because the battery was disconnected). Setting the Pwon flag clears the UV_{NOM} flag and timers. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. In Listen-only mode the Pwon flag can be polled via pin ERR_N. See Table 6. The flag is cleared when the transceiver enters Normal mode.

7.3.4 Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request. A local wake-up request is detected when the logic level on pin WAKE changes, and the new level remains stable for at least t_{wake}. The Wake flag can be set in Standby mode, Go-to-Sleep mode or Sleep mode. Setting the Wake flag clears the UV_{NOM} flag and timers. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided V_{IO} and V_{BAT} are present). This flag is also set at power-on and cleared when the UV_{NOM} flag is set or the transceiver enters Normal mode.

7.3.5 Remote wake-up (via the CAN bus)

The TJA1043 wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2026) is detected on the bus. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern. See Figure 5. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

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- The TJA1043 switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} undervoltage is detected (UV_{NOM} flag set; see Section 7.3.1)

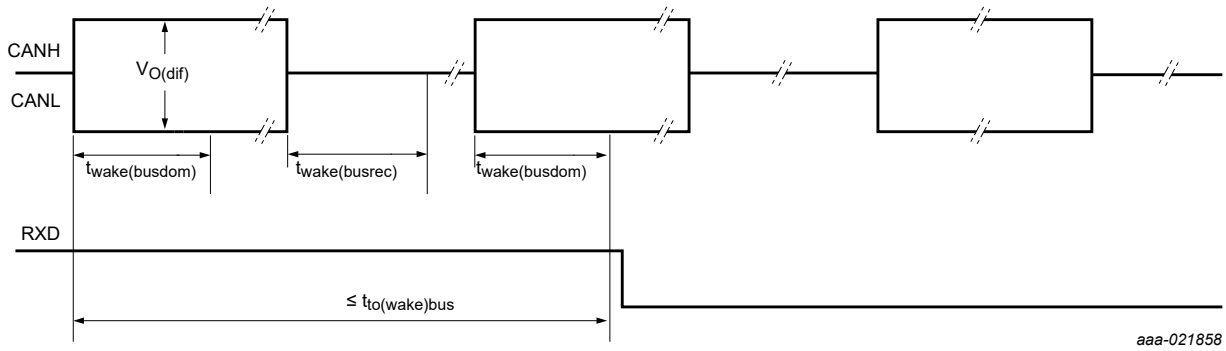

Figure 5. Wake-up timing

7.3.6 Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag, which is set when the Wake flag is set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode. See Table 6. This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

7.3.7 Bus failure flag

The Bus failure flag is set if the transceiver detects a bus line short-circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, while trying to drive the bus lines dominant. The Bus failure flag can be polled via the ERR_N pin in Normal mode. See Table 6. This flag is cleared at power-on or when the transceiver re-enters Normal mode.

7.3.8 Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four different local failure events, any of which will cause the Local failure flag to be set. The four local failure events are: TXD dominant clamping, TXD-to-RXD short circuit, bus dominant clamping and an overtemperature event. The nature and detection of these local failures is described in Section 7.4. The Local failure flag can be polled via the ERR_N pin in Listen-only mode. See Table 6. This flag is cleared at power-on, when entering Normal mode or when RXD is dominant while TXD is recessive, provided that all local failures have been resolved.

7.4 Local failures

The TJA1043 can detect four different local failure conditions. Any of these failures will set the Local failure flag, and in most cases the transmitter of the transceiver will be disabled.

7.4.1 TXD dominant time-out function

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communications. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter if pin TXD remains LOW for longer than the TXD dominant time-out time $t_{to(dom)TXD}$. The $t_{to(dom)TXD}$ timer defines the minimum possible bit rate of 40 kbit/s. The transmitter remains disabled until the Local failure flag has been cleared.

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7.4.2 TXD-to-RXD short-circuit detection

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

7.4.3 Bus dominant time-out function

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The Local failure flag is set if the dominant state on the bus persists for longer than $t_{to(dom)bus}$. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag does not retain a bus dominant clamping failure, and is released as soon as the bus returns to recessive state.

7.4.4 Overtemperature detection

If the junction temperature becomes excessive, the transmitter will shut down in time to protect the output drivers from overheating without compromising the maximum operating temperature. The transmitter will remain disabled until the Local failure flag has been cleared.

7.5 SPLIT pin

Using the SPLIT pin on the TJA1043 in conjunction with a split termination network (see Figure 6 and Figure 8) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal and Listen-only modes, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby, Go-to-Sleep, and Sleep modes, pin SPLIT is floating.

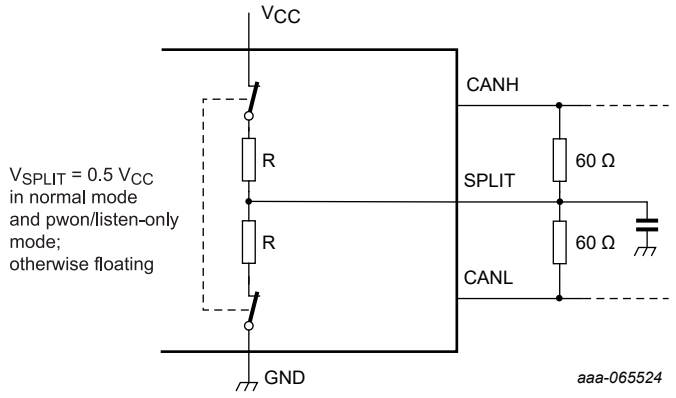

Figure 6. Stabilization circuit and application

7.6 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. See Figure 8. This will cause the signal levels of pins TXD, RXD, STB_N, EN and ERR_N to be adjusted to the I/O levels of the microcontroller, facilitating direct interfacing without the need for glue logic.

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7.7 WAKE pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin, allowing for maximum flexibility when designing a local wake-up circuit.To minimize current consumption, the internal bias voltage will follow the logic state on the pin after a delay of t_{wake}. A HIGH level on pin WAKE is followed by an internal pull-up to V_{BAT}. A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that don't make use of the local wake-up facility, it is recommended that the WAKE pin be connected to V_{BAT} or GND to ensure optimal EMI performance.

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8 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
Limiting Voltages/Currents					
V_{BAT}	battery supply voltage[1]		–0.3	+58	V
		load dump	—	58	V
V_x	voltage on pin x[1]	on pins CANH, CANL and SPLIT	–58	+58	V
		TJA1043H only; on pins CANH, CANL	–60	+60	V
		on pin WAKE	–0.3	+58	V
		on pin INH	–0.3	V_{BAT} + 0.3	V
		on pins VCC, VIO, TXD, RXD, STB_N, EN, ERR_N	–0.3	+7	
I_{WAKE}	current on pin WAKE		—	–15	mA
Limiting Differential Voltages					
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		–20	+20	V
$V_{(X-Y)}$	voltage between pin X and Y	TJA1043H only: X and Y can be any combination of pins VBAT, WAKE, CANH, and CANL	–60	+60	V
Transients					
V_{trt}	transient voltage	on pins CANH, CANL, SPLIT, and VBAT [2]			
		pulse 1	–100	—	V
		pulse 2a	—	75	V
		pulse 3a	–150	—	V
		pulse 3b	—	100	V
V_{Bus}	CAN bus voltage (wiring failure)	TJA1043H only; Common-mode choke 100 µH; all modes; transmitting dominant and recessive bits [3]	V_{BAT} –58	+58	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [4]			
		at pins CANH and CANL	–8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ [5]			
		at pins CANH and CANL	–8	+8	kV
		at any other pin	–4	+4	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [6]			
		at any pin	–300	+300	V
		Charged Device Model (CDM); field Induced charge; 4 pF [7]			
		at corner pins	–750	+750	V
		at any other pin	–500	+500	V
Temperature					
T_{vj}	virtual junction temperature	[8]	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

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[3] Test condition emulating bus short-to-battery or module loss-of-ground failure cases. Internal clamping mechanisms protect the device from transients caused by such condition, no further external protection device needed. The observed peak voltages are the result of successful internal clamping and thus are tolerated by the device, even when they exceed the rated voltage range V_x.
[4] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.
[5] According to AEC-Q100-002.
[6] According to AEC-Q100-003
[7] According to AEC-Q100-011 Rev-C1. The classification level is C4B.
[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9 Thermal characteristics

Table 8. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO14 package; in free air	76	K/W
		HVSON14 package; in free air	45	K/W
$R_{th(j-c)}$	thermal resistance from junction to case [2]	HVSON14 package; in free air	12	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO14 package; in free air	8	K/W
		HVSON14 package; in free air	5	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).
[2] Case temperature refers to the center of the heatsink at the bottom of the package.

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10 Static characteristics

Table 9. Static characteristics

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; RL = 60 Ω; T_{vj} = –40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to GND; positive currents flow into the device[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	—	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC	V_{BAT} > 4.5 V	3	3.5	4.3	V
I_{CC}	supply current	Normal mode; dominant; V_{TXD} = 0 V	30	48	65	mA
		Normal or Listen-only mode; recessive; V_{TXD} = V_{IO}	3	6	9	mA
		Standby or Sleep mode; V_{BAT} > V_{CC}	0	0.75	2	µA
		Normal mode; dominant; V_{TXD} = 0 V; short circuit on bus lines; –3 V < (V_{CANH} = V_{CANL}) < +18 V	3	79	109	mA
I/O level adapter supply; pin VIO						
V_{IO}	supply voltage on pin VIO		2.8	—	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	V_{BAT} or V_{CC} > 4.5 V	0.8	1.8	2.5	V
I_{IO}	supply current on pin VIO	Normal mode; V_{TXD} = 0 V (dominant)	—	150	500	µA
		Normal or Listen-only mode; V_{TXD} = V_{IO} (recessive)	0	1	4	µA
		Standby or Sleep mode	0	1	4	µA
Supply pin VBAT						
V_{BAT}	battery supply voltage		4.5	—	40	V
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin VBAT		3	3.5	4.3	V
I_{BAT}	battery supply current	Normal or Listen-only mode	15	40	70	µA
		Standby mode; V_{CC} > 4.5 V; V_{INH} = V_{WAKE} = V_{BAT}	5	18	30	µA
		Sleep mode; V_{INH} = V_{CC} = V_{IO} = 0 V; V_{WAKE} = V_{BAT}	5	18	30	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	—	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	—	0.3V_{IO}	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{IO}	–5	0	+5	µA
I_{IL}	LOW-level input current	Normal mode; V_{TXD} = 0 V	–300	–200	–30	µA
C_i	input capacitance	not tested	—	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} – 0.4 V; V_{IO} = V_{CC}	–12	–6	–1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; V_{TXD} = V_{IO}; bus dominant	2	6	14	mA
Standby and enable control inputs; pins STB_N and EN						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	—	V_{IO} + 0.3	V

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Table 9. Static characteristics...*continued*

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; RL = 60 Ω; T_{vj} = –40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to GND; positive currents flow into the device[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		–0.3	—	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	V_{STB_N} or V_{EN} ≥ 0.7 V_{IO}	1	4	10	µA
I_{IL}	LOW-level input current	V_{STB_N} = V_{EN} = 0 V [2]	–1	0	+1	µA
Error and power-on indication output; pin ERR_N						
I_{OH}	HIGH-level output current	V_{ERR_N} = V_{IO} – 0.4 V; V_{IO} = V_{CC}	–50	–20	–4	µA
I_{OL}	LOW-level output current	V_{ERR_N} = 0.4 V	0.1	0.5	2	µA
Local wake-up input; pin WAKE						
I_{IH}	HIGH-level input current	V_{WAKE} = V_{BAT} – 1.9 V	–10	–5	–1	µA
I_{IL}	LOW-level input current	V_{WAKE} = V_{BAT} – 3.1 V	1	5	10	µA
V_{th}	threshold voltage	V_{STB_N} = 0 V	V_{BAT} – 3	V_{BAT} – 2.5	V_{BAT} – 2	V
Inhibit output; pin INH						
ΔV_H	HIGH-level voltage drop	I_{INH} = –0.18 mA	0	0.25	0.8	V
I_L	leakage current	Sleep mode	–2	0	+2	µA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t< $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} – V_{CANH} – V_{CANL}	–400	—	+400	mV
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF; V_{CC} = 4.75 V to 5.25 V [2] [3]	$0.9V_{CC}$	—	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXD} = 0 V; t< $t_{to(dom)TXD}$;V_{CC} = 4.75 V to 5.25 V				
		R_L = 45 Ω to 65 Ω	1.5	—	3	V
		R_L = 45 Ω to 70 Ω	1.5	—	3.3	V
		R_L = 2240 Ω	1.5	—	5	V
		recessive; no load				
		Normal or Listen-only mode; V_{TXD} = V_{IO}	–50	—	+50	mV
		Standby or Sleep mode	–0.2	—	+0.2	V
$V_{O(rec)}$	recessive output voltage	recessive; no load				
		Normal or Listen-only mode; V_{TXD} = V_{IO}	2	$0.5V_{CC}$	3	V
		Standby or Sleep mode	–0.1	0	+0.1	V
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; t <$t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = –15 V to +40 V TJA1043H only: V_{CANH} = (V_{BAT} – 58 V) to +58 V	–100	–70	—	mA
		pin CANL; V_{CANL} = –15 V to +40 V TJA1043H only: V_{CANL} = (V_{BAT} – 58 V) to +58 V	—	70	100	mA

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Table 9. Static characteristics...*continued*

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; RL = 60 Ω; T_{vj} = –40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to GND; positive currents flow into the device[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; $V_{TXD} = V_{IO}$; $V_{CANH} = V_{CANL}$ = –27 V to +32 V	–3	—	+3	mA
		TJA1043H only; Normal mode; $V_{TXD} = V_{IO}$; $V_{CANH} = V_{CANL} = (V_{BAT} – 58\ V)$ to +58 V;	–9	—	+9	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	–30 V ≤ V_{CANL} ≤ +30 V; –30 V ≤ V_{CANH} ≤ +30 V				
		Normal or Listen-only mode	0.5	0.7	0.9	V
		Standby or Sleep mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	–30 V ≤ V_{CANL} ≤ +30 V; –30 V ≤ V_{CANH} ≤ +30 V				
		Normal or Listen-only mode	–4	—	0.5	V
		Standby or Sleep mode	–4	—	0.4	V
$V_{dom(RX)}$	receiver dominant voltage	–30 V ≤ V_{CANL} ≤ +30 V; –30 V ≤ V_{CANH} ≤ +30 V				
		Normal or Listen-only mode	0.9	—	9.0	V
		Standby or Sleep mode	1.15	—	9.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal or Listen-only mode; –30 V ≤ V_{CANL} ≤ +30 V; –30 V ≤ V_{CANH} ≤ +30 V	50	120	400	mV
I_L	leakage current	V_{CC} = 0 V; $V_{CANH} = V_{CANL}$ = 5 V	100	170	250	µA
		V_{BAT} = 0 V; $V_{CANH} = V_{CANL}$ = 5 V	–2	—	+2	µA
		$V_{CC} = V_{IO} = V_{BAT}$ = 0 V or $V_{CC} = V_{IO} = V_{BAT}$ = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	–2	—	+2	µA
R_i	input resistance	–2 V ≤ V_{CANL} ≤ +7 V; –2 V ≤ V_{CANH} ≤ +7 V [2]	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V [2]	–3	0	+3	%
$R_{i(dif)}$	differential input resistance	–2 V ≤ V_{CANL} ≤ +7 V; –2 V ≤ V_{CANH} ≤ +7 V [2]	19	30	52	kΩ
C_i	input capacitance	CANH or CANL relative to GND [2]	—	—	20	pF
$C_{i(dif)}$	differential input capacitance	[2]	—	—	10	pF
Common mode stabilization output; pin SPLIT						
V_O	output voltage	Normal or Listen-only mode; –500 µA < I_{SPLIT} < 500 µA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal or Listen-only mode R_L = 1 MΩ	$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
I_L	leakage current	Standby or Sleep mode; –58 V < V_{SPLIT} < +58 V	–3	0	+3	µA
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[2]	—	190	—	° C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

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[2] Not tested in production; guaranteed by design.
[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 10.

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11 Dynamic characteristics

Table 10. Dynamic characteristics

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V (58 V for H product version only); R_L = 60 Ω; T_{vj} = –40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to GND[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN FD timing characteristics according to ISO 11898-2:2026; see Figure 7 and Figure 9						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	—	70	—	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	—	90	—	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or Listen-only mode	—	60	—	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or Listen-only mode	—	70	—	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	40	—	240	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	40	—	240	ns
CAN FD timing characteristics according to ISO 11898-2:2026 parameter set B ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbit/s); see Figure 7 and Figure 9						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	–45	—	+10	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	–80	—	+20	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	–45	—	+15	ns
CAN FD timing characteristics according to ISO 11898-2:2026 parameter set A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s); see Figure 7 and Figure 9						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	–65	—	+30	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	–100	—	+50	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	–65	—	+40	ns
Dominant time-out time						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V [2]	0.4	—	1.5	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)}$ > 0.9 V	0.4	—	1.5	ms
Bus wake-up times; pins CANH and CANL; see Figure 7 and Figure 9						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby or Sleep mode; V_{BAT} = 12 V [3]	0.5	—	3	µs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby or Sleep mode; V_{BAT} = 12 V [3]	0.5	—	3	µs
$t_{to(wake)bus}$	bus wake-up time-out time	[4]	0.5	—	2	ms
Local wake-up input; pin WAKE, see Section 7.3.4 and Section 7.7						
t_{wake}	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode [5]	5	—	50	µs
Mode transitions						
t_h	hold time	from issuing go-to-sleep command to entering Sleep mode [3]	20	—	50	µs
Undervoltage detection; see Section 7.3.1						
$t_{det(uv)}$	undervoltage detection time	on pins VCC, VIO	100	—	350	ms
$t_{rec(uv)}$	undervoltage recovery time	on pins VCC, VIO	1	—	5	ms

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Minimum value of 0.8 ms required according to SAE J2284; 0.3ms is allowed according to ISO 11898-2:2026 for legacy devices. Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[3] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[4] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

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[5] Wake-up occurs between min and max values. Wake-up is guaranteed not to occur below the min value; wake-up is guaranteed to occur above the max value.

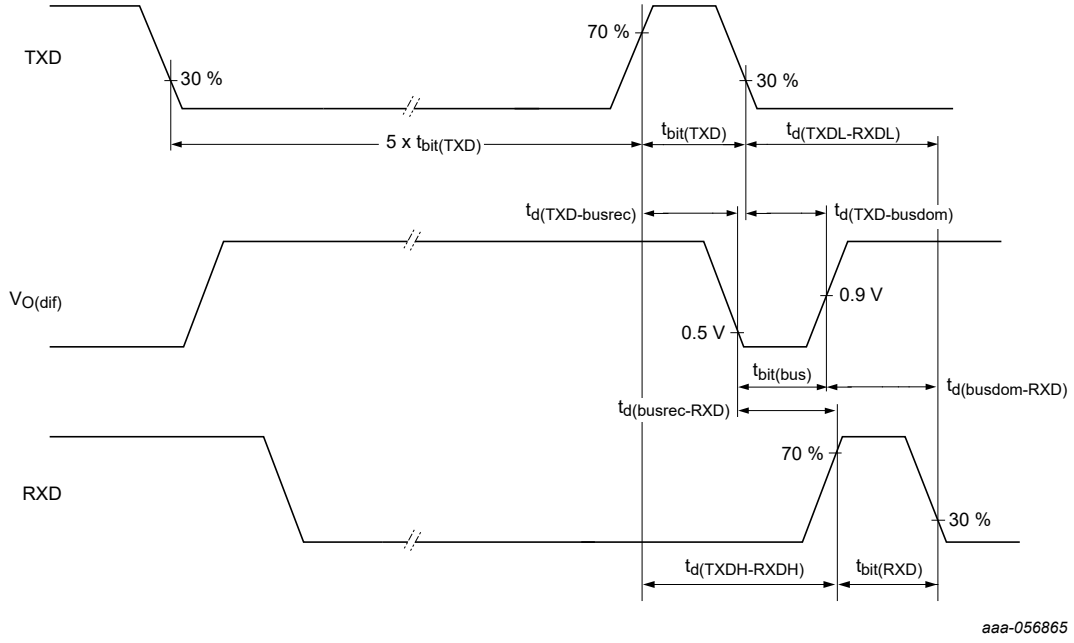

Figure 7. CAN transceiver timing diagram according to ISO 11898-2:2026

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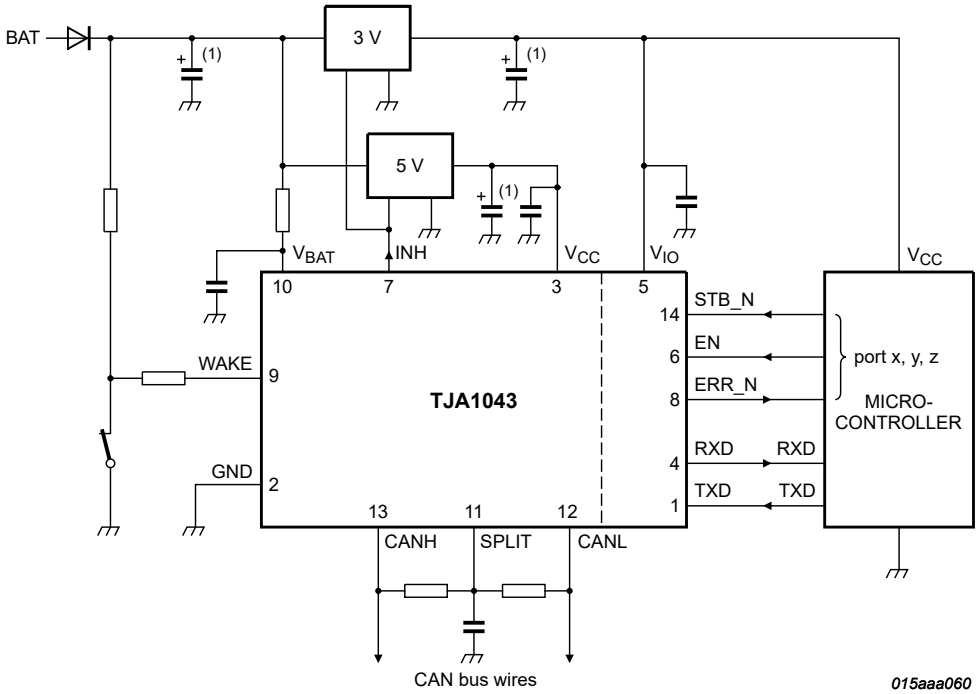
12 Application information

The minimum external circuitry needed with the TJA1043 is shown in Figure 8. See the Application Hints (Section 12.2) for further information about external components and PCB layout requirements.

12.1 Application diagram



1. Optional, depends on regulator

Figure 8. Typical application with a 3.3 V microcontroller

12.2 Application Hints

Further information on the application of the TJA1043 can be found in NXP application hints AH1014 ‘Application Hints - Standalone high speed CAN transceiver TJA1042/TJA1043/TJA1048/TJA1051’.

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13 Test information

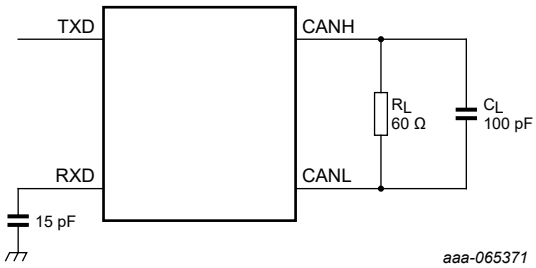

Figure 9. CAN transceiver timing test circuit

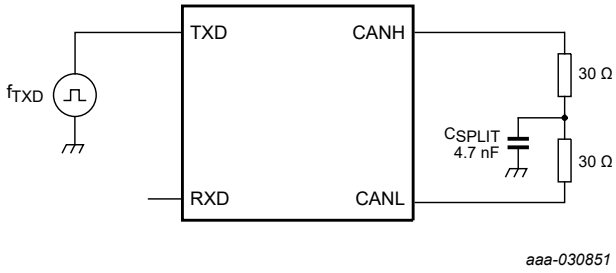

Figure 10. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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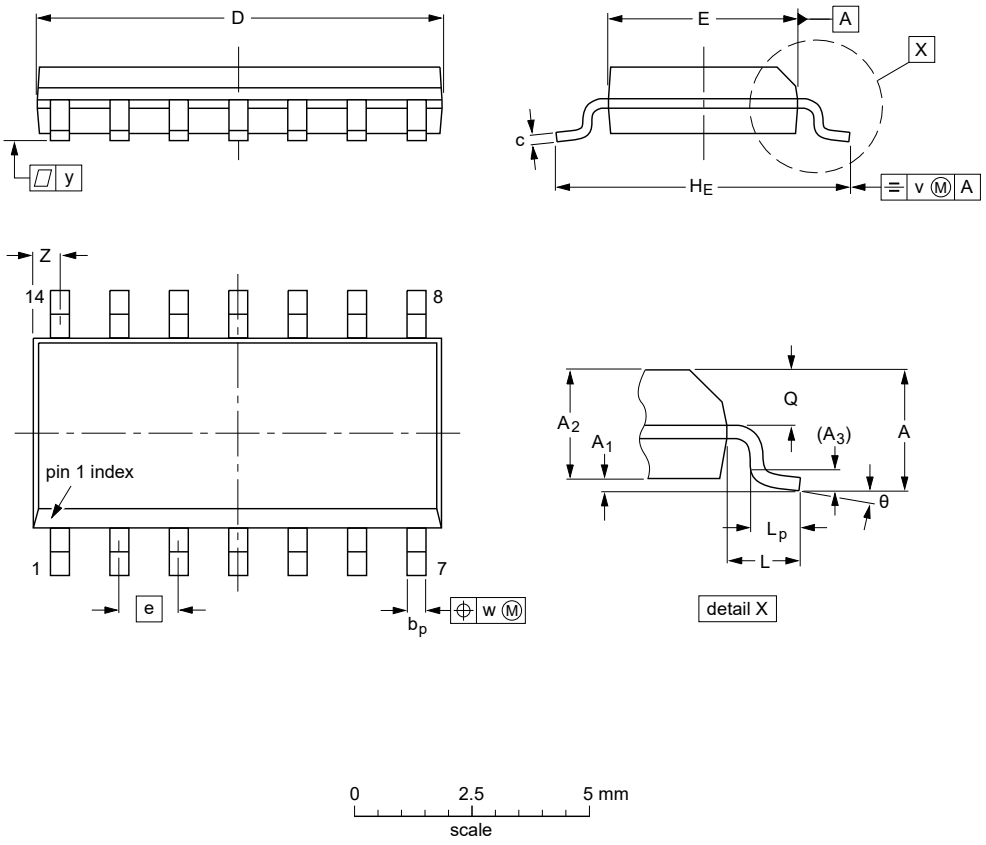
14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 11. Package outline SOT108-1 (SO14)

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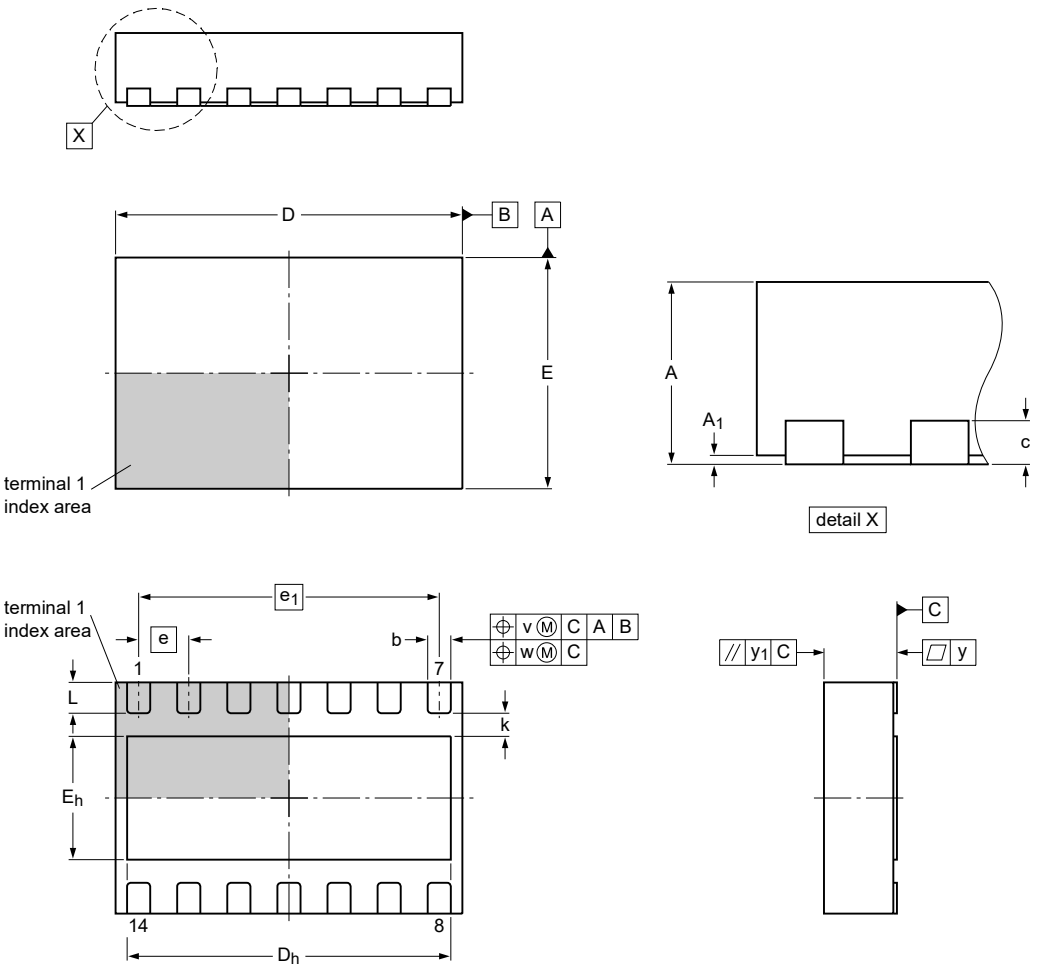
HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 12. Package outline SOT1086-2 (HVSON14)

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15 Handling information

All input and output pins are protected against Electrostatic discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in JESD625-A or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and Table 12

Table 11. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering. See Figure 13.

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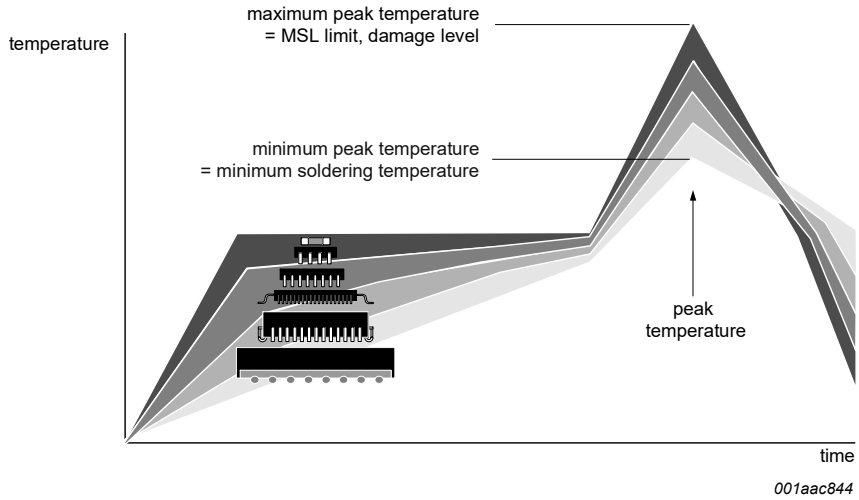

Figure 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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17 Appendix: ISO 11898-2:2026 parameter cross-reference lists

Table 13. ISO 11898-2:2026 to NXP data sheet parameter conversion[1] [2]

ISO 11898-2:2026		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff} (2)			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive (3 option a, 4, [A2])			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics (5, [A3])			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff_nom}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration	V_{Diff_arb}		
Optional: Differential voltage on extended bus load range	V_{Diff_ext}		
Maximum HS-PMA dominant driver output current (6, [A5])			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive (7, 8)			
Recessive state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
Dominant state differential input voltage range		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching) (9, 10)			
Differential internal resistance	$R_{DIFF_pas_rec}$	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	$R_{SE_pas_rec_H}$ $R_{SE_pas_rec_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered (11, [A5])			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry (12 option a, [A9])			
Driver symmetry	V_{sym_vcc} V_{sym}	V_{TXsym}	transmitter voltage symmetry

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Table 13. ISO 11898-2:2026 to NXP data sheet parameter conversion[1] [2] *...continued*

ISO 11898-2:2026		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Optional HS-PMA transmit dominant time-out (13, [A10])			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
HS-PMA implementation loop delay requirement for parameter sets A, B and C (14, [A11])			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD-BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS-RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter set A, B and C (15, 16, 17)			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry variation	$t_{\Delta Rec}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C (18)			
Differential internal resistance (CAN_H to CAN_L)	$R_{Diff_act_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Internal single-ended resistance	$R_{SE_act_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Start time of active signal improvement phase	$t_{act_rec_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act_rec_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas_rec_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start
PMA voltage wake-up control timings (20, [A16])			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time for an arbitration bit rate up to 667 kBit/s	$t_{Filter(667)}$	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time for an arbitration bit rate up to 1 MBit/s	$t_{Filter(1000)}$	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH_N)}$	INH start-up time
		$t_{startup(INH_N)}$	INH_N start-up time
		$t_{startup(ERR_N)}$	ERR_N start-up time

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Table 13. ISO 11898-2:2026 to NXP data sheet parameter conversion[1] [2] *...continued*

ISO 11898-2:2026		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Number of recessive bits before next SOF (21)			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	Number of idle bits before a SOF is accepted
Bitfilter in CAN FD data phase (22)			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter_option1}$	$t_{fltr(bit)dom}$	Dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter_option2}$		
HS-PMA bus biasing control timings (23)			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	Bus silence time-out time
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	Bus bias reaction time
PMA output characteristics during FAST TX mode (A4)			
Single-ended voltage on CAN_H	V_{CAN_H0} V_{CAN_H1}	$V_{CANH(se)}$	Single-ended voltage on pin CANH
Single-ended voltage on CAN_L	V_{CAN_L0} V_{CAN_L1}	$V_{CANL(se)}$	Single-ended voltage on pin CANL
Differential voltage on normal differential load	V_{Diff0} V_{Diff1}	V_{dif}	Differential voltage
PMA static receiver input characteristics, voltage biasing active, FAST RX mode or FAST TX mode (A6)			
Level_0 state differential input voltage	V_{Diff0}	$V_{level0(RX)}$	receiver level 0 voltage
Level_1 state differential input voltage	V_{Diff1}	$V_{level1(RX)}$	receiver level 1 voltage
PMA static OOB input characteristics (voltage bising active; SIC mode) (A7)			
Low state differential input voltage range	$V_{Diff(low)}$	$V_{low(OOB)}$	out-of-bounds receiver low voltage
High state differential input voltage range	$V_{Diff(high)}$	$V_{high(OOB)}$	out-of-bounds receiver high voltage
PMA TXD input characteristics (A8)			
TXD input threshold voltage	$V_{Thresh(TXD)}$	$V_{(TXD)Thresh}$	TXD input threshold voltage
TXD input low voltage range	$V_{Low(TXD)}$	V_{IL}	Low-level input voltage
TXD input high voltage range	$V_{High(TXD)}$	V_{IH}	High-level input voltage
Pull-up impedance	$R_{PU(TXD)}$	R_{pu}	Pull-up resistance
Pull-down impedance	$R_{PD(TXD)}$	R_{pd}	Pull-down resistance
Pull-up and pull-down impedance matching	$m_{R(TXD)}$	m_R	Resistance matching
PMA implementation data signal timing requirements, during SIC mode (A12)			
Transmitted bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta_{tbit(bus)}$	transmitted recessive bit width deviation
Received bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta_{tbit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δ_{trec}	receiver timing symmetry
Propagation delay from TXD logical 0 to bus dominant	$t_{Prop(TXD-Bus\ Dom)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
Propagation delay from TXD logical 1 to bus recessive	$t_{Prop(TXD-Bus\ Rec)}$	$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive

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Table 13. ISO 11898-2:2026 to NXP data sheet parameter conversion[1] [2] *...continued*

ISO 11898-2:2026		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Propagation delay of the receiver from bus to RXD logical 0	$t_{Prop(BusDom-RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD
Propagation delay of the receiver from bus to RXD logical 1	$t_{Prop(BusRec-RXD)}$	$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
RXD low pulse width during fast data traffic b, at the bit rate 10 Mbit/s	$t_{OOB_LOW\ (RXD)}$	$t_{OOB_LOW\ (RXD)}$	OOB RXD pulse width LOW
RXD low pulse width during fast data traffic b, at the bit rate 20 Mbit/s	$t_{OOB_LOW\ (RXD)}$	$t_{OOB_LOW\ (RXD)}$	OOB RXD pulse width LOW
PMA implementation data signal timing requirements, during FAST RX mode or FAST TX mode (A13)			
Signal improvement time in FAST TX mode	t_{SIC_data}	t_{SIC_data}	signal improvement time
SIC mode time after FAST RX detection	$t_{SIC_FAST_RXD_Dis}$	$t_{SIC_FAST_RXD_Dis}$	SIC mode time after FAST RX detection
Transmitted level_1 bit width variation in FAST TX mode	$t_{\Delta Bit(Bus)Level1}$	$\Delta t_{bit(bus)level1}$	transmitted level_1 bit width variation
Received logical width variation FAST TX mode	$t_{\Delta Bit(RXD)Logical1}$	$\Delta t_{bit(RXD)logical1}$	received logical 1 bit width variation
Logical 1 receiver timing symmetry in FAST RX mode	$t_{\Delta REC_Logical1}$	$\Delta t_{rec_logical1}$	logical 1 receiver timing symmetry
Propagation delay from mode change to bus level_0 in FAST TX mode	$t_{Prop(BusDom-BusLevel0)}$	$t_{d(busdom-buslevel0)}$	propagation delay from bus dominant to bus level 0
Propagation delay from mode change to bus recessive FAST TX mode and FAST RX mode	$t_{Prop(BusLevel0-Rec)}$	$t_{d(buslevel0-rec)}$	propagation delay from bus level 0 to bus recessive
Propagation delay from TXD logical 0 to bus level_0 in FAST TX mode	$t_{Prop(TXD-BusLevel0)}$	$t_{d(TXD-buslevel0)}$	propagation delay from TXD logical 0 to bus level_0 in FAST TX mode
Propagation from TXD bus level mode	$t_{Prop(TXD-BusLevel1)}$	$t_{d(TXD-buslevel1)}$	propagation delay from TXD logical 1 to bus level_1 in FAST TX mode
Propagation delay from bus level_0 to RXD logical 0 in FAST TX mode and FAST RX mode	$t_{Prop(BusLevel0-RXD)}$	$t_{d(buslevel0-RXD)}$	propagation delay from bus level_0 to RXD logical 0
Propagation delay from bus level_1 RXD logical 10 in FAST TX mode and FAST RX mode	$t_{Prop(BusLevel1-RXD)}$	$t_{d(buslevel1-RXD)}$	propagation delay from bus level_1 to RXD logical 1
Fall time VDiff in FAST TX mode	$t_{Busfall}$	$t_{Busfall}$	bus fall time
Rise time VDiff in FAST TX mode	$t_{Busrise}$	$t_{Busrise}$	bus rise time
PMA implementation propagation delay symmetry requirements, during mode transition (A14)			
Transmitter propagation delay symmetry ADS/DAS in FAST TX mode	$t_{\Delta Bit(Bus)ADS/DAS}$	$\Delta t_{bit(bus)ADS/DAS}$	transmitter propagation delay symmetry ADS/DAS
Receiver propagation delay symmetry ADS/DAS in FAST TX mode and FAST RX mode	$t_{\Delta Bit(RXD)ADS/DAS}$	$\Delta t_{bit(RXD)ADS/DAS}$	receiver propagation delay symmetry ADS/DAS

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Table 13. ISO 11898-2:2026 to NXP data sheet parameter conversion[1] [2] *...continued*

ISO 11898-2:2026		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
PMA mode selection timing requirements (A15)			
PWM symbol acceptance length	$t_{SymbolNom}$	$t_{SymbolNom}$	PWM symbol acceptance length
FAST to SIC mode switching time	$t_{FastToSIC}$	$t_{(FAST-SIC)}$	FAST to SIC mode switching time
PWM ratio detected as logical_0 FAST TX	$t_{Logical_0_Tx}$	$t_{logical_0_Tx}$	PWM ratio detected as logical_0 FAST TX
PWM ratio detected as logical_1 FAST TX	$t_{Logical_1_Tx}$	$t_{logical_1_Tx}$	PWM ratio detected as logical_1 FAST TX
PWM ratio detected FAST RX	$t_{Logical_Rx}$	$t_{logical_Rx}$	PWM ratio detected FAST RX
Mode pre-selection time	t_{Select}	t_{Select}	mode pre-selection time
PWM detection resolution	t_{Decode}	t_{Decode}	PWM detection resolution

[1] This is a general glossary of ISO-to-NXP parameter conversion. A product may not have all parameters defined, the actual parameters are defined in the Static and Dynamic characteristics table of the product's datasheet.
[2] The identifier(s) between brackets after each section header refer(s) to the associated table(s) in ISO 11898-2:2026.

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18 Revision history

Table 14. Revision history

Document ID	Release date	Description
TJA1043 v.7.0	29 Sep 2026	• Added product variants TJA1043HT and TJA1043HTK throughout • ISO 11898-2:2016 upgraded to ISO 11898-2:2026 throughout • Section 2.1 – Added footnote [1] – Revised bullet 3 (suitability for voltage systems) and 4 (EMC compliance) – Added "The TJA1043H provides support for 48 V systems." • Figure 1: Added bidirectional arrows on pins CANH and CANL • Added Table 4 • Table 3: Added "Type" column • Table 7: Added various TJA1043H-only parameter specifications and footnote [3] • Table 8: Revised table • Table 9: Added $I_{O(sc)rec}$ specification for TJA1043H • Table 10 – Formatting of CAN (FD) timing characteristics revised according to ISO 11898-2:2026 – Added footnotes [3] and [4] – Original Figs. 7 and 8 combined in new single Figure 7 • Section 13: Replaced all figures in this section • Table 13: Cross-reference table updated to ISO 11898-2:2026 • Deleted *Soldering of HVSON packages*
TJA1043 v.6.01	20171110	—
TJA1043 v.5.01	20160523	—
TJA1043 v.4	20150119	—
TJA1043 v.3	20130424	—
TJA1043 v.2	20110620	—
TJA1043 v.1	20100330	• Initial version

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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