TAA6065AT

Digital configurable LLC controller

Rev. 1.0 — 3 September 2025 Product data sheet

1 General description

The TAA6065AT is an AEC-Q100 automotive qualified digital configurable controller for high-efficiency resonant micro-DCDC converters and local BMS HV supplies. The micro-DCDC converter is easy to design and has a very low component count. It meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines.

To increase the efficiency of a low-voltage supply output, the TEA2095T dual SR controller can be added on the secondary side.

When an EV is parked, all main functions are switched-off, except for some required vital functions, for example, vehicle monitoring, battery temperature management, theft protection, and the use of external apps.

The power consumption in EV parking mode is called battery vampire drain (BVD). It can cause a reduction of the EV range.

In the EV parking mode, the main HV-LV DCDC converters are preferably switched-off, due to limited efficiency at light loads. To keep the vital functions active in the EV parking mode, a micro-DCDC converter can be used.

The key benefit of the TAA6065AT controller is that it achieves the highest efficiencies at all load levels, because of the NXP GreenChip V_{cap} control technology and the advanced low-power mode. It helps to reduce the power consumption in parking mode.

In contrast to traditional resonant topologies, the TAA6065AT achieves a high efficiency at low loads due to the low-power mode. This mode operates in the power region between continuous switching (also called high-power mode) and burst mode.

Because the TAA6065AT is regulated via the primary capacitor voltage, it has accurate information about the power delivered to the output. The measured output power defines the mode of operation (burst mode, low-power mode, or high-power mode).

The TAA6065AT contains a low-voltage die with a fully digital controller for output power control, start-up, initializations, and protections. These protections include overcurrent protection (OCP), overvoltage protection (OVP), and capacitive mode regulation (CMR). The TAA6065AT also contains a high-voltage silicon-on-insulator (SOI) controller for high-voltage start-up, integrated drivers, level shifter, protections, and circuitry that ensures zero-voltage switching.

The TAA6065AT LLC controller enables the building of an easy to design, highly efficient, and reliable micro-DCDC converter. It can provide 90 W to 1500 W output power with a minimum of external components. It has a very low no-load input power (< 75 mW) and a high efficiency from minimum to maximum load.

2 Features and benefits

2.1 Distinctive features

- AEC-Q100 grade 1 qualified: −40 °C to +125 °C ambient temperature range
- LLC controller in a single small-size SO16 package
- Integrated high-voltage start-up
- Integrated drivers and high-voltage level shifter (LS)
- High-side driver directly supplied from the low-side driver output
- Power good function
- Several parameters can easily be configured during evaluation with use of the graphical user interface (GUI), like:
  - Operating frequencies to be outside the audible area at all operating modes
  - Soft start and soft stop in burst mode, reducing the audible noise
  - Accurate transition levels between operation modes (high-power mode/low-power mode/burst mode)
  - Enabling/disabling the lower power mode

2.2 Green features

- Zero voltage switching for minimum switching losses
- Extremely high efficiency from low load to high load
- Compliant with latest energy-saving standards and directives (Energy Star, EuP)
- Excellent no-load input power (< 75 mW for TAA6065AT/TEA2095T combination)

2.3 Protection features

- Independently configurable levels and timers
- Many protections can independently be set to latched, safe restart, or latched after several attempts to restart
- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- Internal and external overtemperature protection (OTP)
- Capacitive mode regulation (CMR)
- Accurate overvoltage protection (OVP)
- Overcurrent protection (OCP)
- Brownin/brownout protection
- Disable input
- Input to reset all protections

3 Applications

- Automotive EV micro-DCDC converter or standby supply
- BMS HV supply and contactor driver

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TAA6065AT/1	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Marking

Table 2. Marking

Type number	Marking code
TAA6065AT/1	TAA6065AT

6 Block diagram

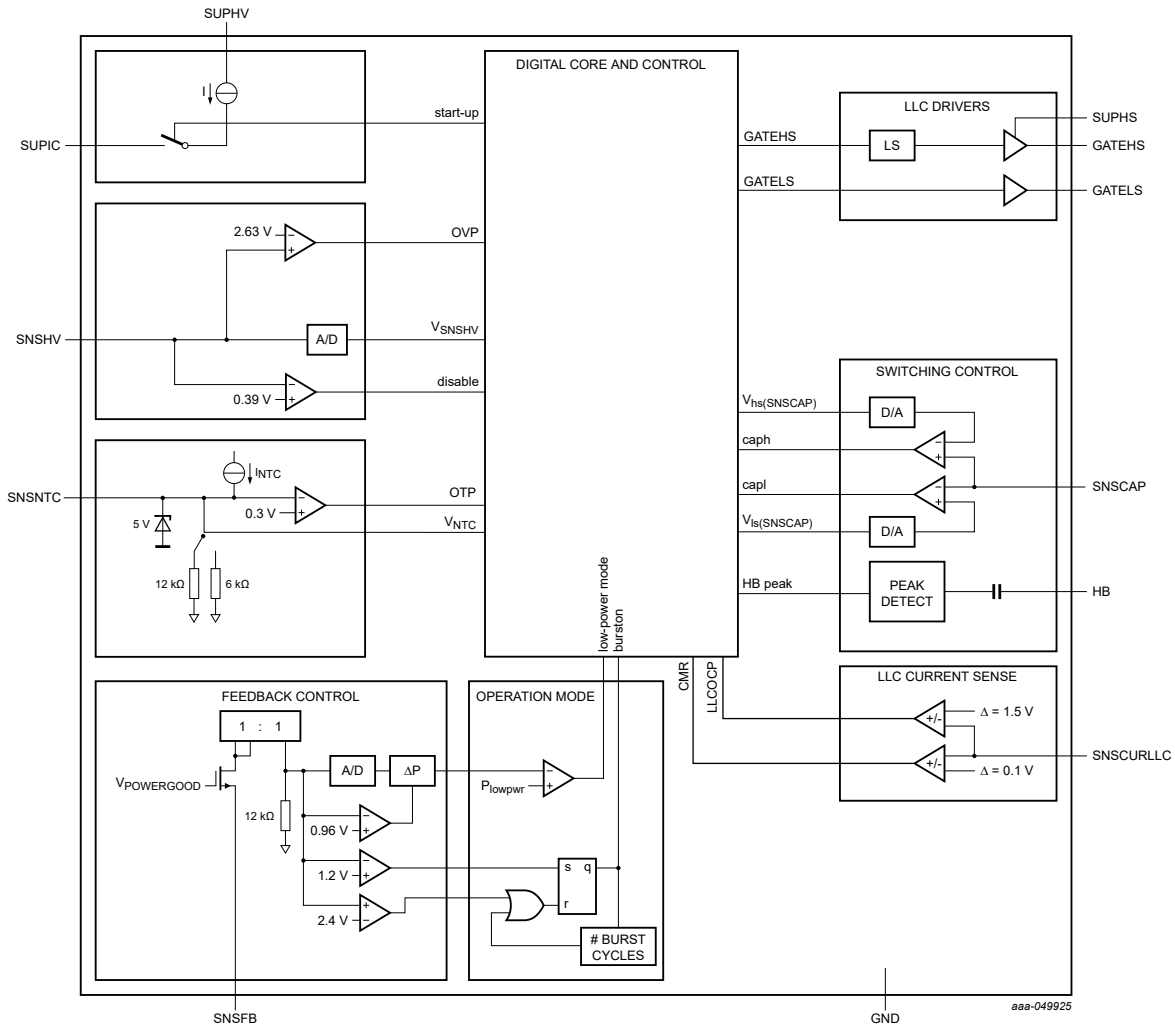


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

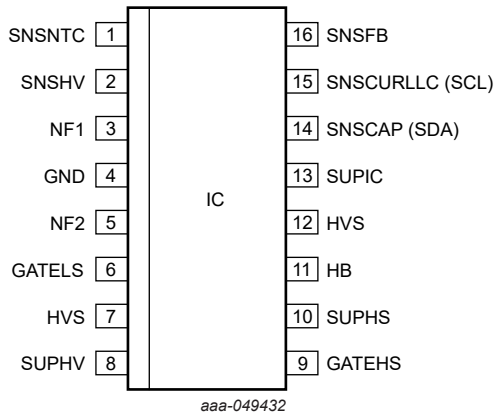


Figure 2. Pin configuration (SOT109-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SNSNTC	1	sense input for NTC
SNSHV	2	sense input for HV battery voltage; externally connected to resistive divider
NF1	3	not functional; must be connected to pin 4 (GND)
GND	4	ground
NF2	5	not functional; not to be connected.
GATELS	6	LLC low-side MOSFET gate driver output and supply for bootstrap capacitor
HVS	7	high-voltage spacer. Not to be connected.
SUPHV	8	internal HV start-up source
GATEHS	9	LLC high-side MOSFET gate driver output
SUPHS	10	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})
HB	11	low-level reference for high-side driver and input for half-bridge slope detection; externally connected to half-bridge node HB between the LLC MOSFETs
HVS	12	high-voltage spacer. Not to be connected.
SUPIC	13	input supply voltage and output of internal HV start-up source; externally connected to an auxiliary winding of the LLC via a diode or to an external DC supply
SNSCAP	14	LLC capacitor voltage sense input; externally connected to divider across LLC capacitor
SNSCURLLC	15	LLC current sense input; externally connected to the resonant current sense resistor
SNSFB	16	output voltage regulation feedback sense input; externally connected to an optocoupler. Output for power good function.

8 Functional description

8.1 Supply voltages

The TAA6065AT includes:

- A high-voltage supply pin for start-up (SUPHV pin)
- A general supply to be connected to an external auxiliary winding (SUPIC pin)
- A floating supply for the high-side driver (SUPHS pin)

8.1.1 Start-up and supply voltage

Initially, the capacitor on the SUPIC pin is charged via the SUPHV pin. The SUPHV pin is connected to the HV battery. Internally, a high-voltage current source is located between the SUPHV pin and the SUPIC pin (see Figure 3).

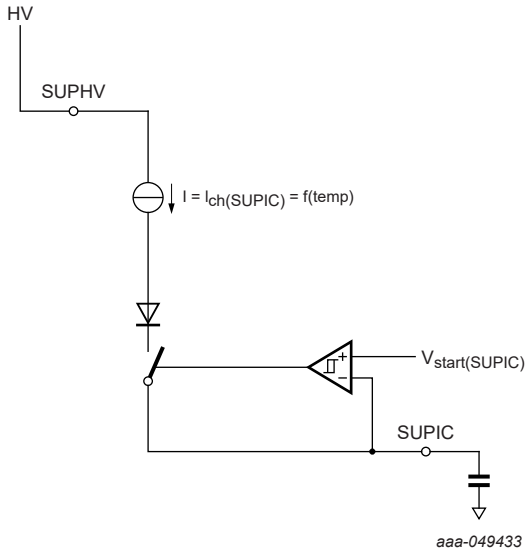


Figure 3. HV start-up

The maximum current of the internal current source is limited to $I_{ch(SUPIC)}$. To limit the IC dissipation, the charge current is reduced when the current source exceeds its maximum temperature.

At start-up, when the SUPIC reaches the $V_{start(SUPIC)}$ level, it is continuously regulated to this start level with a hysteresis ($V_{start(hys)SUPIC}$).

When the start level is reached, it reads the internal MTP (multi-time programmable memory) and defines the settings.

When the SNSHV reaches the minimum level $V_{start(SNSHV)}$, the LLC starts switching.

When start-up is complete and the LLC controller is operating, the LLC transformer auxiliary winding supplies the SUPIC pin. In this operational state, the HV start-up source is disabled.

When the system enters the protection mode, it cannot be supplied via the auxiliary winding. So, the SUPIC pin is regulated to $V_{start(SUPIC)}$ via the SUPHV pin.

During the non-switching period of the burst mode, the SUPIC is regulated to the $V_{low(SUPIC)}$ when SUPIC drops to below this level. It regulates the voltage with a hysteresis of $V_{low(hys)SUPIC}$. In this way, the system avoids that the SUPIC undervoltage protection ($V_{uvp(SUPIC)}$) is triggered because of a long non-switching period in burst

mode. However, the system must be designed such that the internal current source at the SUPHV pin is only active at start-up and extreme output voltage overshoots, followed by a long time of non-switching. Continuous use of this current source increases the input power and affects the lifetime of the product.

When the SUPIC voltage drops to below $V_{rst(SUPIC)}$, the TAA6065AT restarts.

8.1.2 High-side driver floating supply (SUPHS pin)

As the voltage range on the SUPIC pin exceeds that of the maximum external MOSFETs gate-source voltage, the external bootstrap capacitor C_{SUPHS} cannot directly be supplied from the SUPIC.

To provide an external supply for the high-side driver without the need of additional external components, the GateLS output is designed such that it can drive the low-side MOSFET and supply the high-side MOSFET (see Figure 4).

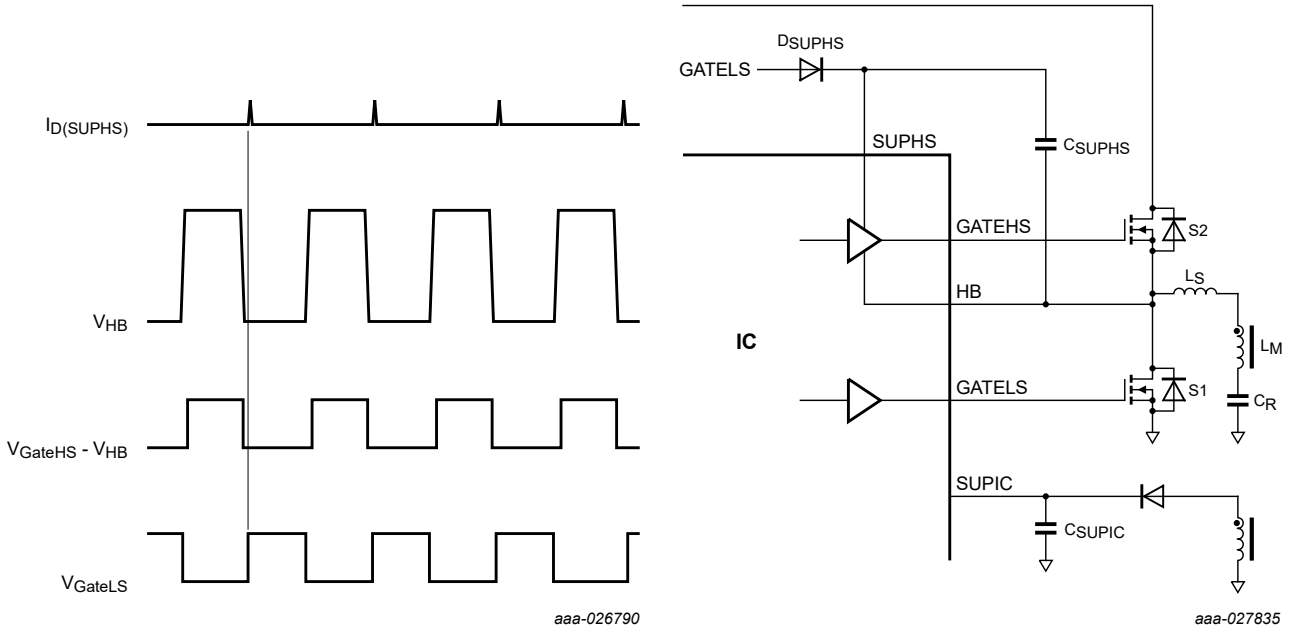


Figure 4. High-side driver supply

The external bootstrap buffer capacitor C_{SUPHS} supplies the high-side driver. The bootstrap capacitor is connected to the low-side driver supply, the GATELS pin, and the half-bridge node (HB) via an external diode (D_{SUPHS}). When GATELS is active high and the HB node is pulled low, C_{SUPHS} is charged.

Careful selection of the appropriate diode minimizes the voltage drop between the GATELS and SUPHS pins, especially when large MOSFETs and high switching frequencies are used. A great voltage drop across the diode reduces the gate drive of the high-side MOSFET.

8.2 LLC system regulation

The TAA6065AT regulates the output power by adjusting the voltage across the primary capacitor. Compared to a standard frequency control loop, it has the advantage that the control loop has a constant gain and the IC has information about the output power. So, the operation mode transition levels are derived from the output power.

Although the TAA6065AT uses the primary capacitor voltage as a regulation parameter, all application values, like the resonant inductances, resonant capacitor, and primary MOSFETs remain unchanged compared to a frequency-controlled LLC converter. A secondary TL431 circuitry with an optocoupler connected to the primary SNSFB pin continuously regulates the output voltage.

8.2.1 Output power regulation loop

Figure 5 shows the output power regulation loop of V_{cap} control as used by the TAA6065AT. Figure 6 shows a corresponding timing diagram.

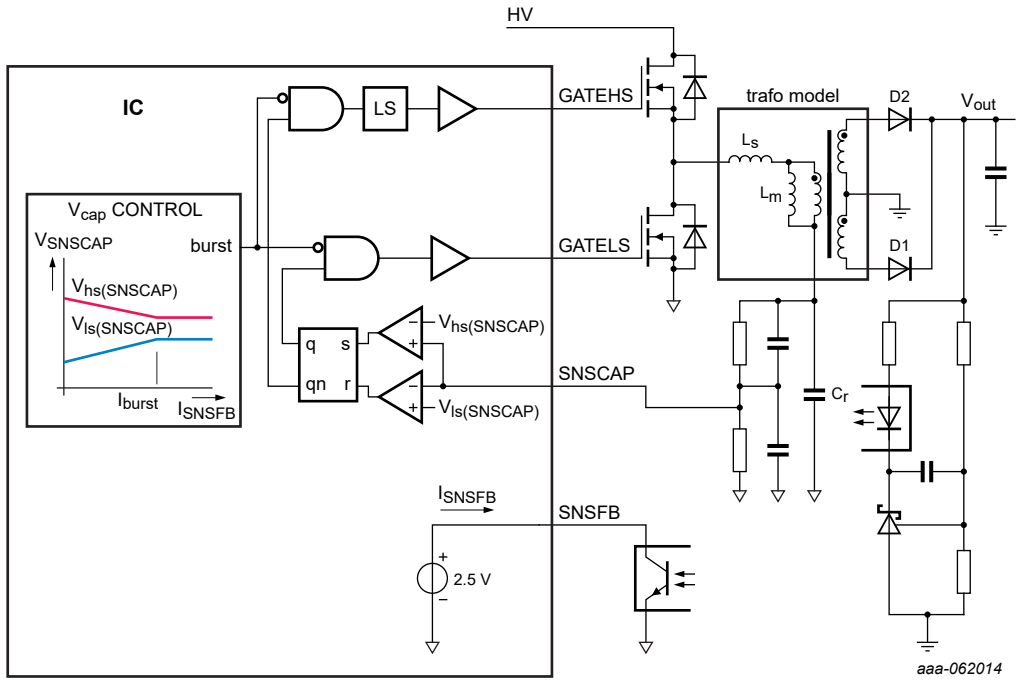


Figure 5. Regulation loop V_{cap} control

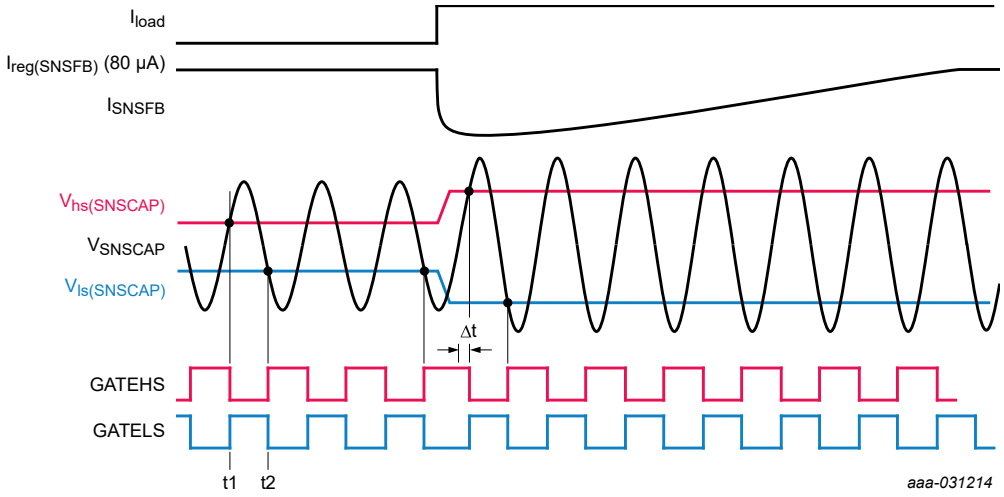


Figure 6. Timing diagram of the regulation loop

When the divided resonant capacitor voltage (V_{SNSCAP}) exceeds the capacitor voltage high level ($V_{hs(SNSCAP)}$), the high-side MOSFET is switched off (see Figure 6 (t1)). After a short delay, the low-side MOSFET is switched on. Because of the resonant current, the resonant capacitor voltage initially increases further but eventually drops.

When the divided capacitor voltage (V_{SNSCAP}) drops to below the capacitor voltage low level ($V_{ls(SNSCAP)}$), the low-side MOSFET is switched off (see Figure 6 (t2)). After a short delay, the high-side MOSFET is switched on. Figure 6 shows that the switching frequency is a result of this switching behavior. In a frequency-controlled system, the frequency is a control parameter and the output power is a result. The TAA6065AT regulates the power and the frequency is a result.

The difference between the high and low capacitor voltage level is a measure of the delivered output power. The value of the primary optocurrent, defined by the secondary TL431 circuitry, determines the difference between the high and low capacitor voltages.

Figure 6 also shows the behavior at a transient. If the output load increases, the current pulled out of the SNSFB pin decreases. The result is that the TAA6065AT increases the high-level capacitor voltage and lowers the low-level capacitor voltage. The output power increases and eventually the output voltage increases to its regulation level.

To minimize no-load input power of the system, the primary current into the optocoupler is continuously regulated to $I_{reg(SNSFB)}$ (see Section 8.4).

8.2.2 Output voltage start-up

At start-up, when the system slowly increases the ΔV_{SNSCAP}, it continuously monitors the primary current via the SNSCURLLC pin. When the voltage at this pin exceeds the $V_{lmtr(ocp)}$ level, increasing the ΔV_{SNSCAP} is on hold until the voltage at the SNSCURLLC pin drops to below the $V_{lmtr(ocp)}$ level again (see Figure 7). The output current is regulated and its voltage shows a nice ramp during start-up. It also avoids that during startup the OCP (overcurrent protection) is triggered. In this way, the LLC converter behaves like a limited current source during start-up.

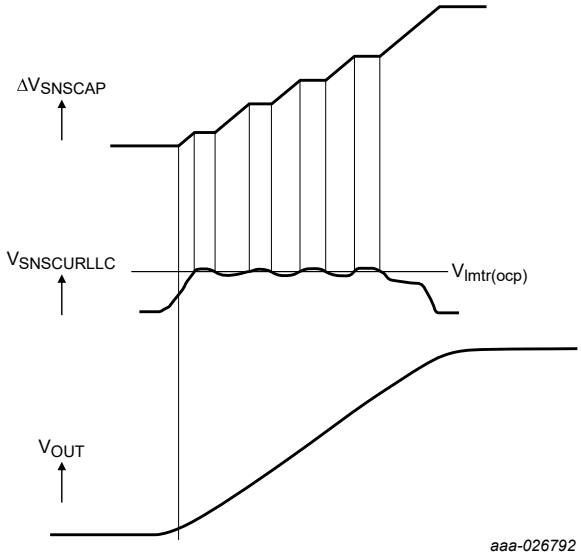


Figure 7. LLC start-up behavior

8.3 Modes of operation

Figure 8 shows the control curve between the output power and the voltage difference between the high and low capacitor voltage levels.

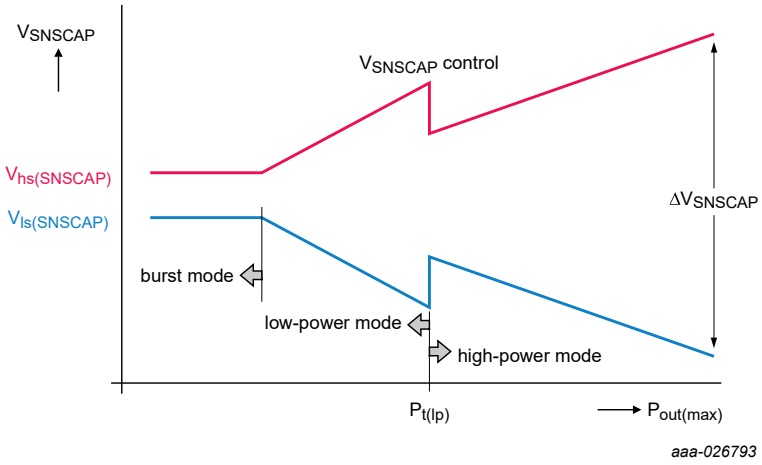


Figure 8. TAA6065AT control curve

When the output power (P_{out}) is at its maximum, the low capacitor voltage level ($V_{ls(SNSCAP)}$) is at its minimum, and the high capacitor voltage ($V_{hs(SNSCAP)}$) is at its maximum level. The maximum ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$), which is the divided ΔV_{Cr} voltage, corresponds to the maximum output power.

When the output load decreases, the ΔV_{SNSCAP} voltage decreases. As a result, the output power decreases and the output voltage is regulated. This mode is called high-power mode. Figure 6 shows a timing diagram of the system operating in high-power mode.

When the output power drops to below the transition level ($P_{t(lp)}$), the system enters the low-power mode. The $P_{t(lp)}$ level can be initialized via the MTP.

To compensate for the non-switching period in low-power mode, also called hold period, ΔV_{SNSCAP} is initially increased at entering the low-power mode (see Section 8.3.2). In low-power mode, the output power is regulated by adapting ΔV_{SNSCAP}, until it reaches a minimum. The system then enters the burst mode (see Section 8.3.3).

8.3.1 High-power mode

In high-power mode, the system operates as described in Section 8.2.1. Figure 9 shows a flow diagram of the high-power mode.

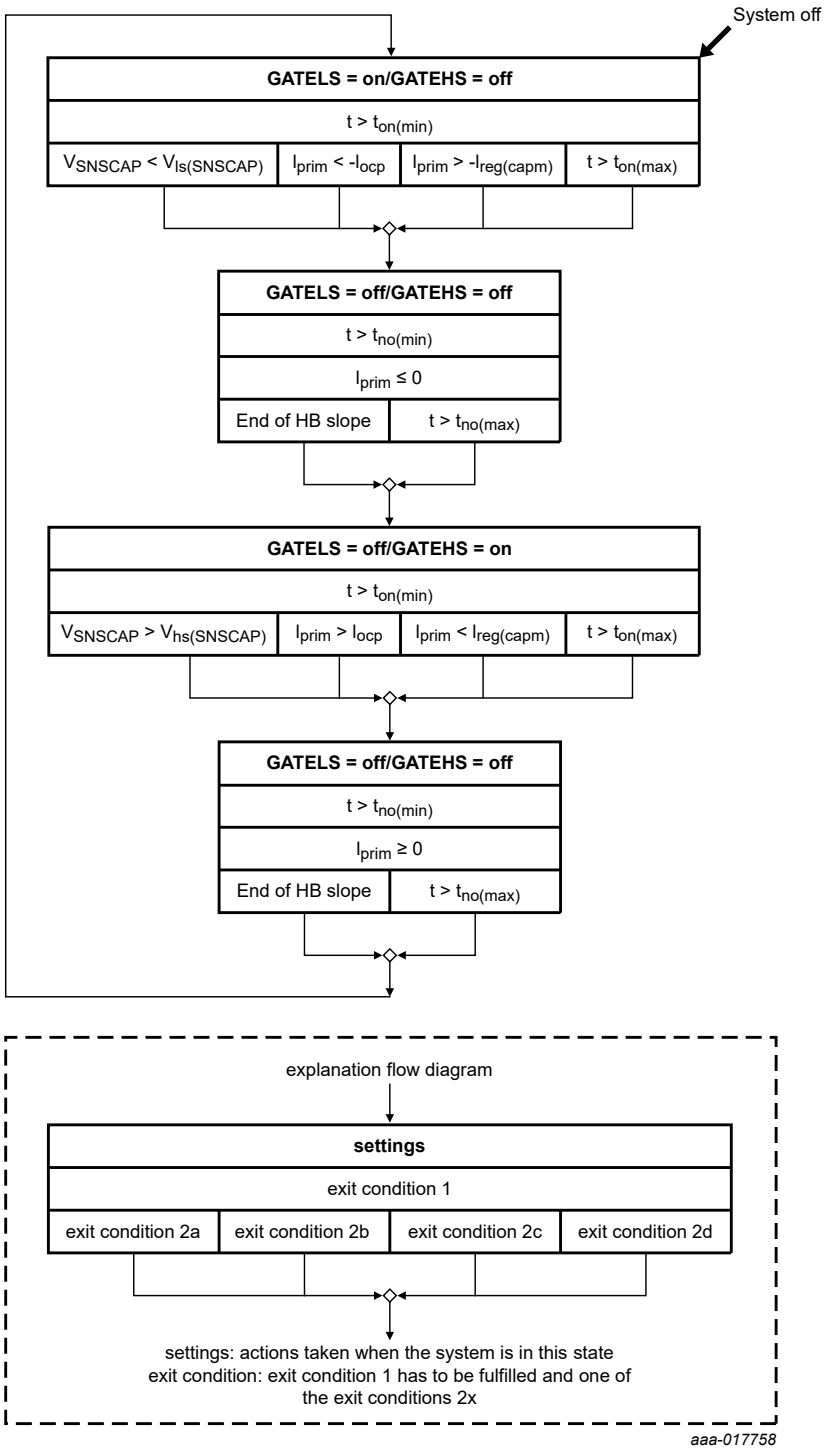


Figure 9. High-power mode flow diagram

Initially, GATELS is on and GATEHS is off. The external bootstrap buffer capacitor (C_{SUPHS}) is charged via the GATELS pin and an external diode. The system remains in this state for at least the minimum on-time ($t_{on(min)}$) of GATELS. Before entering the next state, one of the following conditions must be fulfilled:

- The V_{SNSCAP} voltage drops to below the minimum V_{SNSCAP} voltage ($V_{ls(SNSCAP)}$).
- The measured current exceeds the OCP level (see Section 8.5.12).
- The system is close to capacitive mode (see Section 8.5.11).
- The maximum on-time ($t_{on(max)}$), a protection that maximizes the time the high-side or low-side MOSFET is kept on, is exceeded.

To avoid false detection of the HB peak voltage, the system remains in this state until the minimum non-overlap time ($t_{no(min)}$) is exceeded. When this time is exceeded and it detects the peak of the HB node and the measured resonant current is negative (or zero), it enters the next state.

If the system does not detect a peak at the HB node, it also enters the next state when the maximum non-overlap time ($t_{no(max)}$) is exceeded under the condition of a negative (or zero) resonant current.

Finally, the third and fourth states (see Figure 9) describe the GATEHS and GATEHS to GATELS transition criteria which are the inverse of the first two states.

8.3.2 Low-power mode

At low loads, the efficiency of a resonant converter drops as the magnetization and the switching losses become dominant. A low-power mode ensures high efficiency at lower loads because it reduces the magnetization and switching losses.

When the output power drops to below the $P_{t(lp)}$ level, the system enters the low-power mode (see Figure 8 and Figure 10). It continues switching for 3 half-cycles (low-side, high-side, low-side) with an MTP selectable duty cycle. To ensure a constant output power level, it increases the energy per cycle ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) at the same time.

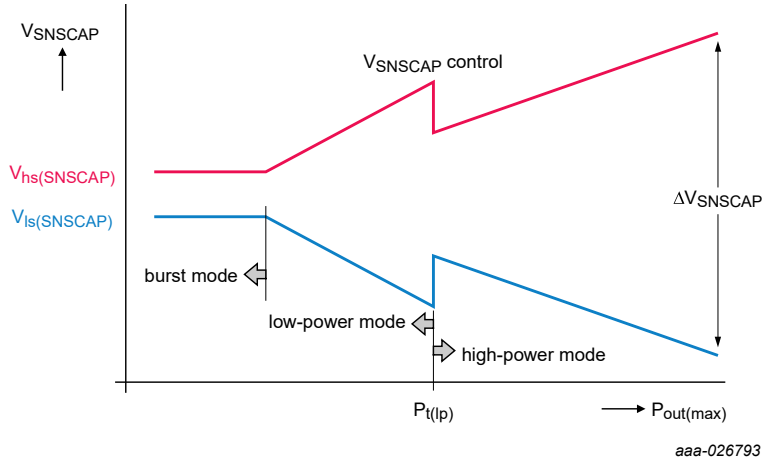


Figure 10. Timing diagram transition high-power mode to low-power mode

As the system continuously tracks the primary capacitor voltage, it knows exactly when to enter the "hold" period. It can also continue again at exactly the correct voltage and current levels of the resonant converter. In this way, a "hold" period can be introduced which reduces the magnetization and switching losses without any additional losses. The currents I_{D1} and I_{D2} (see Figure 10) are the secondary currents through diodes D1 and D2 (see Figure 6).

When in low-power mode the output power is further reduced, the amount of energy per cycle (= ΔV_{SNSCAP}) is reduced and the duty cycle remains the same (see Figure 11).

When in low-power mode the system reaches the programmable minimum energy per cycle (= ΔV_{SNSCAP}), it enters burst mode.

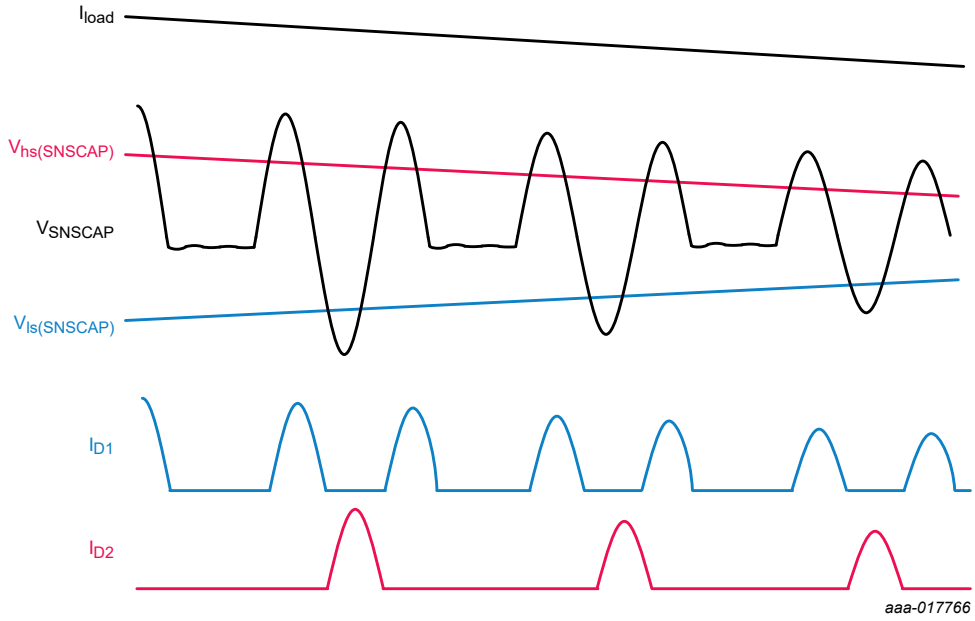


Figure 11. Low-power mode: Lowering the energy-per-cycle (ΔV_{SNCAP})

8.3.3 Burst mode

In burst mode, the system alternates between operating in low-power mode and an extended hold state (see Figure 12). Because of this additional extended hold period, the magnetization and switching losses are further reduced. So, the efficiency of the system is increased.

Figure 12 shows that all operating frequencies are outside the audible area. The minimum low-power frequency can be set with a parameter. Within a low-power period, the system is switching at the resonant frequency of the converter, which is typically between 50 kHz and 200 kHz. The burst frequency ($1/T_{burst}$) can be programmed out side the audible noise area.

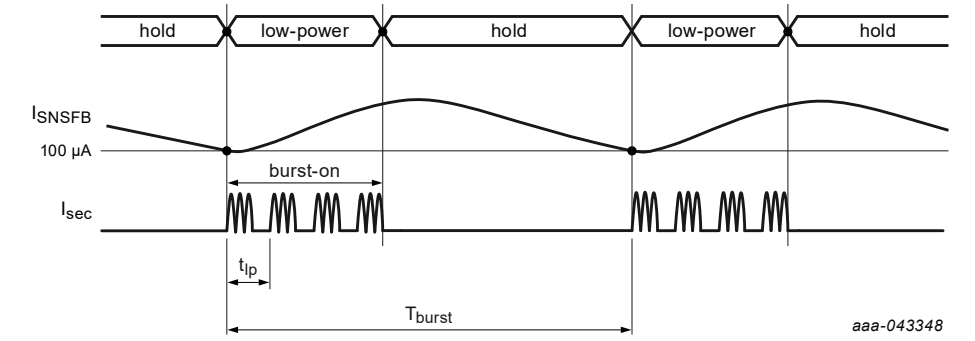


Figure 12. Burst mode

8.3.3.1 Frequency regulation

When the primary optocurrent (I_{SNSFB}) drops to below $I_{start(burst)}$ (100 µA typical), a new burst-on period is started. The end of the burst-on period depends on the calculated number of low-power cycles. The number of low-power cycles within a burst-on period is continuously adjusted so that the total burst period (T_{burst}) is at least the period defined by the setting (see Figure 13).

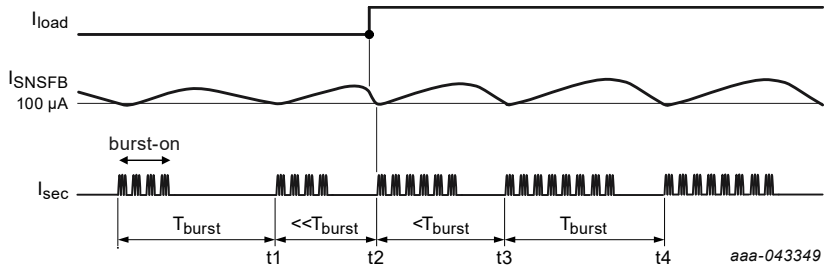


Figure 13. Burst mode: Regulating the number of low-power cycles

The system continuously measures the burst period from the start of the previous burst-on period to a new burst-on period. At t1, the measured burst period (T_{burst}) equals the required T_{burst}. So, the next number of low-power cycles equals the number of previous low-power cycles. At a constant output power, the system expects that when the next burst-on period has the same number of low-power cycles as the previous burst-on period, the burst period (T_{burst}) remains constant.

At a positive transient (t2), a new low-power cycle is started immediately to minimize the drop in output voltage. The measured time period, at time t2, is below the targeted burst period. The system increases the number of burst cycles. At t3, it measures the burst period again. In this example, the burst period is still below the targeted burst period. So, the system increases the number of low-power cycles again and again until the measured burst period equals the target burst period, which occurs at t4.

8.3.3.2 Negative transient response

When the system operates in burst mode, it defines the new number of cycles at the start of a new burst cycle. If the output load is reduced just after the start of a new burst cycle, the output voltage shows an overshoot (see Figure 14).

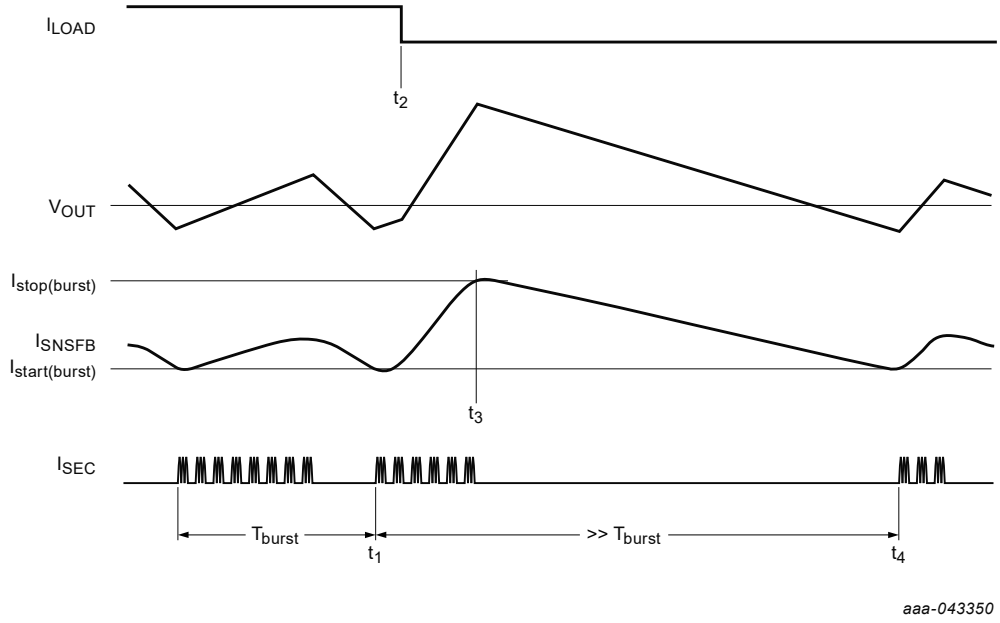


Figure 14. Burst mode - transient

At t1, the system starts with a new burst cycle period. Shortly later at t2, the output load is reduced. As a result the output voltage shows an overshoot and the optocoupler current increases. To limit the overshoot, the system also ends the burst cycle when the optocoupler current exceeds the $I_{stop(burst)}$ level.

8.3.3.3 Burst-mode exit delay function

When the system is in burst mode and a positive transient occurs, it may be preferred to leave the burst mode and restart the burst-mode delay function (see Figure 15).

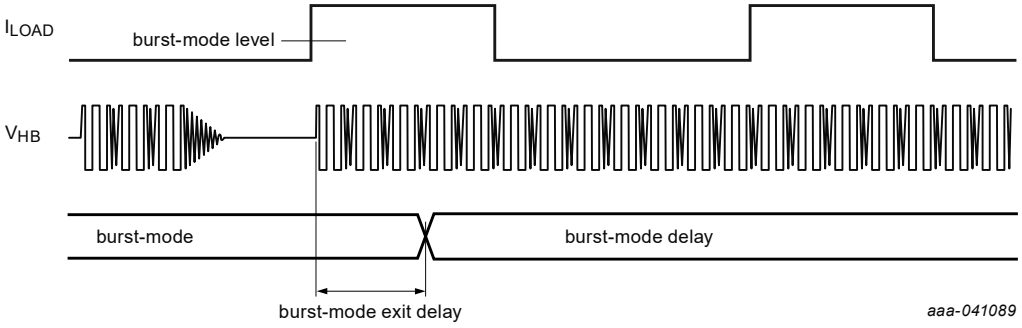


Figure 15. Restart of the burst-mode delay

When the LLC is switching for a time that exceeds the burst-mode exit delay time and the output load exceeds the burst-mode level, the system leaves the burst mode. The burst-mode delay function is activated again. The burst-mode exit delay time can be set with a parameter.

In this way, the transient response is improved at a variable load while the system was initially in burst mode.

8.4 Optobias regulation

In a typical application, the output voltage is sensed using a TL431 and connected to the SNSFB pin of the TAA6065AT via an optocoupler (see Figure 21). Because of the behavior of the TL431, the current through the optocoupler is at the maximum level when the output power is at the minimum level. It is therefore one of the most critical parameters to achieve the required no-load input power. To achieve maximum efficiency at low load/no load, the TAA6065AT continuously regulates the optocurrent to a low level that is independent of the output load.

Because of the parasitic capacitance at the optocoupler collector, a very low optocurrent reduces the transient response of the system. So, the TAA6065AT applies a fixed voltage at the SNSFB pin. It measures the current through the optocoupler which defines the required output power. Via an additional internal circuitry, which adds an offset to the required output power, the optocurrent is continuously (slowly) regulated to the $I_{reg(SNSFB)}$ level (= 80 µA typical). This level is independent of the output power.

At a positive load transient, the optocurrent initially decreases (see Figure 6; I_{SNSFB}). The TAA6065AT immediately increases the ΔV_{SNSCAP} which again increases the output power.

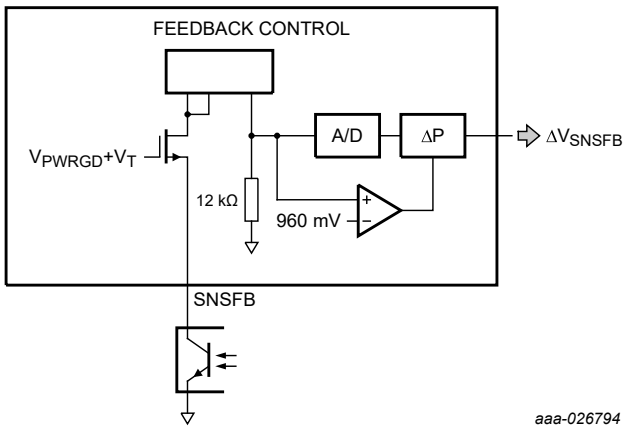


Figure 16. Optobias regulation

Figure 16 shows that when the optocurrent decreases, the internal voltage across the 12 kΩ resistor drops to below the targeted level of 960 mV (= 80 µA (typical) × 12 kΩ). The TAA6065AT then slowly increases an additional offset at the power level (ΔP). It continues to increase the additional offset until the optocurrent reaches the target of 80 µA (typical). When the optocurrent increases due to a transient, the additional offset to the power level is decreased. As a result, the output voltage decreases which again decreases the optocurrent. In this way, the optocurrent is continuously regulated to the $I_{reg(SNSFB)}$ level.

The behavior of the internal circuitry connected to the SNSFB pin is the same as the behavior of the traditional circuitry. The fixed voltage at the SNSFB pin and the continuous regulation of the optocurrent level does not influence the regulation level. The advantage, however, is a reduction in no-load input power and an optimization of the transient response.

When the system operates in low-power mode at the minimum energy per cycle and at minimum duty cycle, it can no longer reduce the optocurrent level to the $I_{reg(SNSFB)}$ target (» 80 µA typical). If the output power decreases further and the optocurrent increases to above the level of Istart(burst) (» 100 µA typical), the burst mode is triggered. When the output power drops to below this level again, a new burst cycle is started (see Figure 12 and Figure 13).

8.5 Protections

8.5.1 Protections overview

Table 4. Protections overview

Protection	Description	Action	LLC	Protection register
General protections				
UVP SUPIC	undervoltage protection SUPIC pins	recharge via SUPHV; restart when $V_{SUPIC} > V_{start(SUPIC)}$	off	-
MTPfail	reading of the internal MTP failed	continue reading until the data is valid; only checked once at start-up	off	Y
OTPint	internal overtemperature protection	latched or safe restart [1]	off	Y
OTPext	external overtemperature protection	latched or safe restart [1]	off	Y
SCP SNSHV/ fast disable	short-circuit protection/ disable LLC	restart when $V_{SNSHV} > V_{scp(start)}$	off	Y
LLC protections				
UVP SUPHS	undervoltage protection SUPHS pin	GATEHS = off	off	-
UVP SNSHV	undervoltage protection SNSHV	restart when $V_{SNSHV} > V_{start(SNSHV)}$	off	-
OVP SUPIC	output overvoltage protection; measured via the SUPIC pin	latched or safe restart [1]	off	Y
OVP SNSHV	overvoltage protection SNSHV voltage	restart when $V_{SNSHV} < V_{stop(ovp)}$	on/off[1]	Y
maximum on-time	maximum on-time of the LLC MOSFET	LLC MOSFET switched off; continue operation	-	Y
CMR	capacitive mode regulation	system ensures that mode of operation is inductive	-	Y
OCP	overcurrent protection	switch off cycle-by-cycle; After several consecutive cycles, latched or safe restart [1]	off	Y
STARTUP MAX	maximum start-up time	latched or safe restart [1]	off	Y
OPP	overpower protection	latched or safe restart [1]	off	Y

[1] Selectable via a parameter at the MTP.

When the system is in a latched or safe restart protection, the SUPIC voltage is regulated to its start level via the SUPHV pin.

8.5.2 Undervoltage protection SUPIC

When the voltage on the SUPIC pin is below its undervoltage level $V_{uvp(SUPIC)}$, the LLC converter stops switching. The capacitors at the SUPIC pin are recharged via the SUPHV pin.

When the SUPIC supply voltage exceeds its start level, the system restarts.

8.5.3 MTP fail

At start-up, when the SUPIC reaches 12 V, the system reads the parameters from the internal MTP. If reading the MTP failed, a protection is triggered. A mains reset is required before the system starts. During this time, the LLC remains off.

8.5.4 Internal overtemperature protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the LLC stops switching.

The response of the internal OTP can be either latched or safe restart.

8.5.5 External overtemperature protection

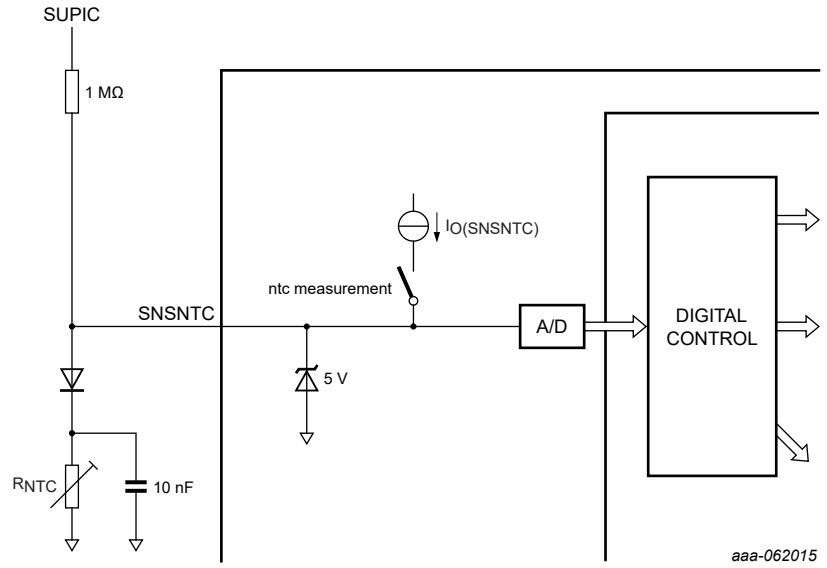


Figure 17. Mains measurement

During an NTC measurement, which is enabled every ~20 ms, an internal current source of $I_{o(SNSNTC)}$ is switched on. With the external NTC and diode, the internal current source generates a voltage at the SNSNTC pin. If this voltage remains below the $V_{det(SNSNTC)}$ level, the external OTP protection is triggered after $t_{d(otp)}$.

8.5.6 Short-circuit protection/fast disable

The LLC does not start switching until the voltage on the SNSHV pin exceeds $V_{scp(start)}$. This function acts as short circuit protection for the HV voltage.

When the SNSHV pin is shorted to ground or the SNSHV pull-up resistor is disconnected, this protection inhibits switching.

This function can also be used as a fast disable. If this pin is shorted to ground via an external MOSFET, the system either stops switching or enters the protection mode followed by safe restart or latched protection. In this way, an additional external protection can be added.

When the fast disable function is selected to stop switching only, it can be combined with a reset of all protections. The MTP bit “fast disable FLR” must be enabled then. So, if any protection is triggered, it is reset when the SNSHV voltage drops to below the $V_{scp(stop)}$ level for at least $t_{d(flr)}$. When the SNSHV voltage exceeds the $V_{start(SNSHV)}$ level, the LLC resumes switching.

8.5.7 Overvoltage protection (SNSHV pin)

When an OVP at the SNSHV is detected for a minimum period (can be set using a parameter), the LLC can be disabled.

8.5.8 Undervoltage protection SUPHS

To ensure a minimum drive voltage at the high-side driver output (GATEHS), this driver is turned off when its voltage is below the minimum level ($V_{SUPHS} < V_{rst(SUPHS)}$).

8.5.9 Undervoltage protection HV

The HV voltage is measured via a resistive divider connected to the SNSHV pin. The voltage at the SNSHV pin must exceed the start level ($V_{SNSHV} > V_{start(SNSHV)}$) before the LLC converter is allowed to start switching.

When the system is operating and the voltage at the SNSHV pin drops to below the minimum level ($V_{SNSHV} < V_{uvp(SNSHV)}$), the LLC converter stops switching. When it exceeds the start level, it restarts.

8.5.10 Overvoltage protection (SUPIC pin)

When the voltage at the SUPIC pin exceeds the $V_{O(ovp)SUPIC}$ level for $t_{d(ovp)SUPIC}$, the OVP protection is triggered. The voltage at the SUPIC pin is continuously monitored via an internal A/D converter.

The OVP protection level and the OVP delay time can be selected with a parameter.

The OVP function can also be disabled.

8.5.11 Capacitive mode regulation (CMR)

The TAA6065AT has a capacitive mode regulation (CMR) which ensures that the system is always operating in inductive mode and avoids operation in capacitive mode.

At lower input voltage or higher output power and depending on the resonant design, the resonant current can already approach zero before the capacitor voltage reaches the regulation level.

When the resonant current has changed polarity before the switches are turned off and the other switch is turned on, hard switching occurs. This event is called capacitive mode. To avoid that the LLC operates in capacitive mode, the system also switches off the high-side/low-side switch when the resonant current approaches zero.

Figure 18 shows the signals that occur when a resonant converter is switching in CMR mode. At t1 (and also at t3), the low-side switch is on while the resonant current approaches zero before V_{SNSCAP} reaches $V_{ls(SNSCAP)}$. At t2, the resonant current is also close to changing polarity while the divided capacitor voltage (V_{SNSCAP}) has not reached the $V_{hs(SNSCAP)}$ level yet. To avoid a turn-off of the high-side switch at a negative current or the low side at a positive current, the system also turns off the high-side/low-side switch when the primary

current approaches zero. So at t2, the high-side switch is turned off because the primary current is close to zero. At t_3 (and also at t_1), the low-side switch is turned off, although V_{SNSCAP} did not reach the regulation level ($V_{ls(SNSCAP)}$) yet. The primary current is measured via an external sense resistor connected to the SNSCURLLC pin. The capacitive mode protection levels are $V_{reg(capm)}$ (−100 mV typical and +100 mV typical). These levels can be adjusted with a parameter.

In this mode, the amount of output power is reduced and the output voltage decreases.

The TAA6065AT does not enter a so-called "capacitive mode protection", but avoids this mode of operation.

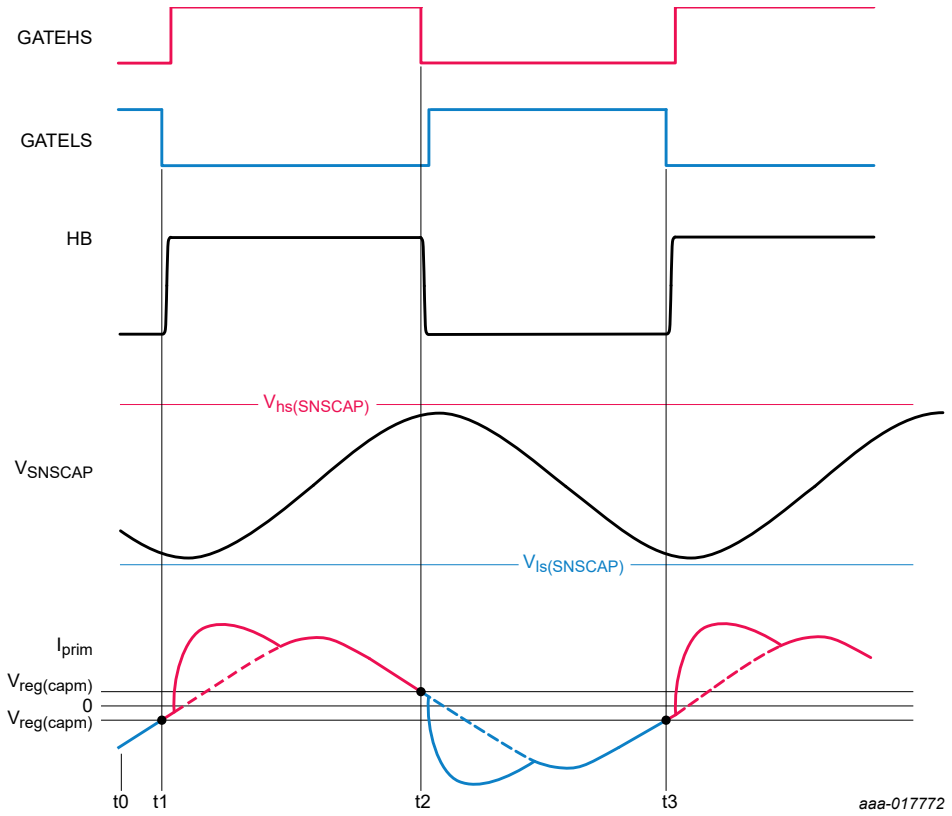


Figure 18. Near capacitive mode switching

8.5.12 Overcurrent protection

The system measures the LLC primary current continuously via a sense resistor connected to the SNSCURLLC pin. If the measured voltage exceeds the fixed overcurrent level ($V_{ocp(LLC)}$), the corresponding switch (GATELS/GATEHS) is turned off, but the system continues to switch. In this way, the primary current is limited to the OCP level.

The OCP level can be adjusted via the external sense resistor.

If the OCP is continuously triggered for an adjustable time, the system enters the OCP protection state. The OCP protection state can also be disabled. However, the primary current is always limited to the OCP level cycle-by-cycle.

8.5.13 Maximum start-up time

If the output voltage of the LLC is not in regulation within an adjustable time after the LLC has started switching, the maximum start-up time protection is triggered.

The maximum start-up time ($t_{startup(max)}$) can be set with the parameter “Maximum start-up time”. If this protection is triggered, the system is latched, safe restart, or latched after safe restart, which follows the setting of the OPP.

8.5.14 Overpower protection

For the overpower protection, three levels can be set:

- Absolute maximum output power, which is the highest output power level.When the output power exceeds this maximum level, it is limited cycle-by-cycle. If the output power exceeds this maximum, the output voltage decreases.
  The maximum output power can be set to a percentage of the rated output power.
- A first overpower level, which is below the maximum output power level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. The LLC is switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the maximum output power is set to 170 % and this first overpower level is set to −20 %, the timer is started at 150 % of the rated output power.
  The timer of the first overpower level can also be set. The first overpower level can also be disabled.
- A second overpower level, which is typically below the first overpower level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. The LLC is switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the output power is set to 170 % and this second overpower level is set to −50 %, the timer is started at 120 % of the rated output power.
  The timer of the second overpower level can be set to a predefined level. The second overpower level can also be disabled.

The overpower function can be either latched, safe restart, or latched after safe restart. Section 8.5.15 describes this function.

8.5.15 Latched, safe restart, or latched after safe restart

When a protection is selected to be latched, the system stops switching when this protection is triggered. The system only restarts after a fast latch reset (see Section 8.5.16) or when the SUPIC supply voltage drops below the UVP level.

When a protection is selected to be safe restart, the system continuously restarts after a predefined safe restart time. This safe restart time is the same for all protection functions. It can be set with a parameter.

When selecting “latched after safe restart”, a protection is initially a safe restart protection. If the failure occurs again within a specific time, it latches eventually.

Figure 19. Latched after safe restart

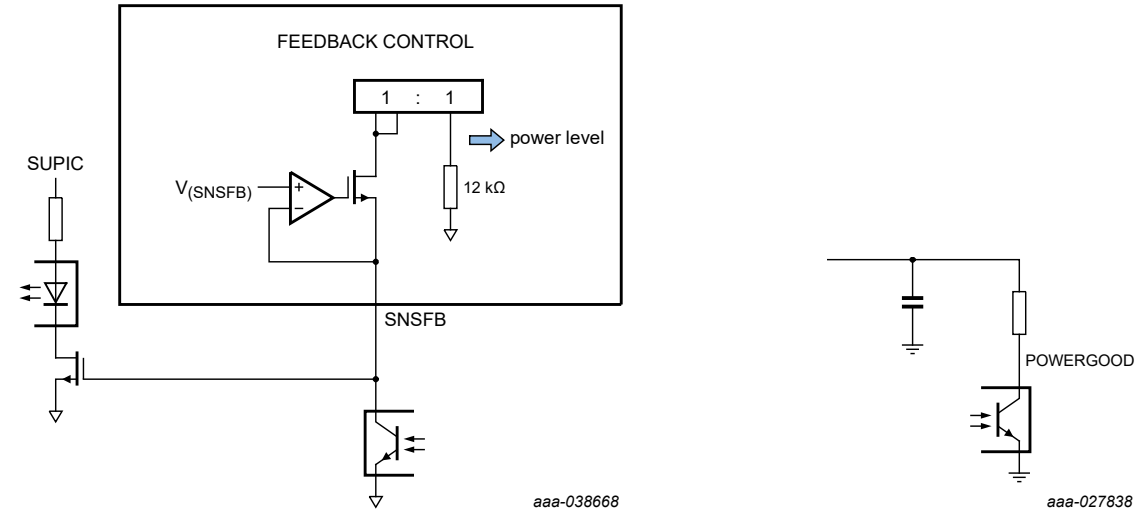
Figure 19 shows an example of when the OVP is set to latched after safe restart. Initially at an OVP, the system restarts after the safe restart time. An internal counter is then set to '1'. If the protection is triggered again, the counter is increased. If the counter reaches the number as set with a parameter, the system latches. If no protection is triggered within 65 seconds, the counter is reset.

8.5.16 Fast latch reset

If a protection is triggered, the system enters the protection state. Especially when the protection is latched, this function is inconvenient during production tests. So, when the mains voltage is below the brownout level for a specified time, the system also restarts. This time can be set with a parameter. This function is called fast latch reset.

8.6 Power good function

The TAA6065AT provides a power good function via the SNSFB pin.



a. Primary side

b. Secondary side

Figure 20. Power good function

The primary function of the SNSFB pin is to regulate the output voltage via an optocoupler. So, it measures the current that is drawn from the SNSFB. Via an internal 12 kΩ resistor, it regulates the output power. The output power regulation is independent of the voltage level of the SNSFB pin. So, the voltage level at the SNSFB

pin is used to indicate if the system is about to stop operating, a so-called power good signal. The voltage at the SNSFB pin can be used to generate a secondary power good signal using an external MOSFET and an optocoupler.

At start-up, the SNSFB voltage is at a high level, pulling down the secondary power good signal. As soon as the system enters the operating state, the SNSFB goes low. The external power good signal becomes active high.

The SNSFB voltage becomes active high, lowering the secondary power good signal when:

- The voltage on the SNSHV pin drops to below $V_{det(SNSHV)}$.
- The OPP counter is close to its end value.
- The converter is about to stop due to an OTP protection.
- When the LLC converter is about to stop due to an OVP on the SNSHV when this function is enabled.
- When the LLC converter is about to stop due to a mains brownout when this function is enabled.

To avoid any disturbance of the regulation loop, the increase and decrease of the SNSFB voltage is in alignment with a predefined ramp.

When the system enters protection mode (OVP, OCP, or UVP), it pulls high the SNSFB pin and stops switching immediately.

8.7 Settings

The TAA6065AT has an internal MTP at which different settings can be programmed.

The TAA6065AT settings can be found in Section 14.

Disclaimer:

The MTP parameter settings can be changed using the “Ringo” GUI software of NXP Semiconductors. Before the user can change any MTP parameters using the GUI, the terms and conditions in the start-up pop-up screen must be accepted.

8.7.1 General settings

8.7.1.1 Protection register

When the TAA6065AT triggers a protection, it can be read which protection was triggered. Even when the root cause of the protection is solved and the converter continues switching, the information about the protection remains until the software program (Ringo GUI) clears it.

8.7.1.2 Supply start level

The SUPIC start level can be selected between 12 V and 19 V. Typically, a level of 19 V is selected. When the TAA6065AT is externally supplied, for instance via a standby supply, the lower start level of 12 V can be used.

After start-up, when the MTP is read and a 12 V start level is selected, charging via the SUPHV is disabled, as the system assumes that it is externally supplied.

8.7.1.3 Read lock

Normally, the software tool can read all the programmed settings. This option can be used to verify the correct settings or for failure analyses.

However, once in production, enabling the "Read lock" bit protects the parameters. Then it is not possible anymore to read the MTP content. It can however still be reset to the default values and also clear the read lock parameter.

8.7.1.4 Write lock

To avoid that the MTP content (accidentally) gets overwritten, a write-lock bit can be set. It can, however, still be reset to the default values and clear the write lock parameter.

8.7.1.5 Reset to the default values

When the MTP is reset, it implies that all parameters are set to a default value. The default values normally do not correspond to the original MTP values. They are chosen such that a general application works properly.

When the MTP is reset, the MTP can be read and written again.

8.7.1.6 Customer MTP code

When in production, the content of the MTP can be hidden when the read lock bit is enabled. To get access to the content of the MTP, a unique customer code can be programmed. This customer code provides information about the MTP content.

This customer code can always be read, even when the read lock bit is enabled.

8.7.2 LLC settings

8.7.2.1 LLC disable

Especially for validation purposes, an option is available to disable the LLC. When the LLC is disabled, a restart is required.

8.7.2.2 Start-up

Maximum (start-up) frequency

The maximum switching frequency of the LLC is limited to a value, which is defined using a parameter. This value also defines the maximum switching frequency during start-up. The maximum frequency can be set to different values ranging from 150 kHz to 800 kHz.

LLC soft-start time

The LLC soft-start time defines the rate at which the converter lowers its switching frequency. This rate can be selected between 2 and 20 which leads to a start-up time of approximately between 1 ms and 10 ms. However, it depends on the LLC design. A higher speed lowers the start-up time. However, it can cause a high charge current and an overshoot at the output voltage.

Maximum primary current during start-up

At start-up, the LLC starts switching at the maximum frequency and ramps down the frequency until the ΔV_{SNSCAP} reaches the required level. If during this start-up time the primary current, which reflects the output current, reaches a predefined level, the frequency is temporarily not further reduced until the primary current drops to below the level again. This level is measured via the SNSCURLLC pin. The following values can be selected: 0.5 V, 0.75 V, 1.0 V, or 1.25 V.

8.7.2.3 LLC switching

ΔV_{SNSCAP} dump level

When the system is in low-power mode, a switching period is followed by a waiting period. The system ensures that it continues at the same stage as where it stopped. To reach the maximum efficiency, the end of the last switching cycle can be fine-tuned. For the ΔV_{SNSCAP} dump level, values between 2.525 V and 2.7 V can be selected in steps of 25 mV.

Minimum non-overlap time

To ensure that the GATEHS is properly turned off before the GATELS is turned on, and vice versa, there is a minimum non-overlap time. For the minimum non-overlap time, the following values can be selected: 100 ns, 230 ns, 350 ns, 500 ns.

Maximum non-overlap time

When the system does not detect a valley at the HB node after turning off GATEHS, the system turns on the GATELS after the maximum non-overlap time. The same counts when a peak at the HB node is not detected after turning off the GATELS and turning on the GATEHS. For the maximum non-overlap time, the following values can be selected: 0.5 µs, 0.7 µs, 0.9 µs, or 1.1 µs.

Maximum on-time

When the on-time of the GATELS or GATEHS exceeds the maximum on-time, the switch is turned off, and the LLC converter starts the next cycle. For the maximum on-time, the following values can be selected: 10 µs, 20 µs, 30 µs, or 38 µs.

Capacitive mode regulation

When the voltage at the SNSCURLLC pin, which reflects the resonant current, drops to below a predefined value, the LLC converter starts the next switching cycle. In this way, the TAA6065AT avoids that the converter operates in capacitive mode. For the capacitive mode regulation, the following values can be selected: 20 mV to 160 mV in steps of 20 mV.

LLC maximum ringing time

When the LLC operates in LP mode, it counts the amount of ringings. If a ringing is not detected, it assumes a peak after the timeout. This timeout can be set to 3 µs, 5 µs, 7.5 µs, or 10 µs. The appropriate value depends on the application. It must be chosen just above the maximum ringing period.

8.7.2.4 Feedback

Optocoupler current

To achieve a low no-load input power, the current through the optocoupler must be set at a low level. However, depending on the selected optocoupler, a higher optocoupler current may be requested. So, the optocoupler current can be set to different values ranging from 80 µA to 1.2 mA.

8.7.2.5 Operation modes

HP-LP transition level

When the output power drops to below a predefined level, the system switches from the HP to the LP mode. The HP-LP transition level can be set to different values ranging from 10 % to 54 %.

HP-LP transition hysteresis

When the system operates in LP mode, it switches over to HP mode when the output power exceeds the selected HP-LP transition level plus a hysteresis. For the hysteresis, the following values can be selected: 10 %,

20 %, 30 %, or 40 % of the selected HP-LP transition level. So, if the rated output at 100 % is 100 W, the HP-LP transition level is set at 30 % and the hysteresis is set at 10 %. The eventual hysteresis is 3 W.

LP-BM transition level

When the output power drops below the LP-BM transition level, the system enters burst mode. The LP-BM transition level can be set to different values ranging from 1 % to 25 %.

The actual LP-BM transition level can deviate from the selected value due to delays in the system. The deviation is most noticeable at low LP-BM transition levels. In this case, the LP-BM transition level can be fine-tuned in steps of 1 %.

BM-LP transition level

When the system operates in burst mode and output power increases to exceed the LP-BM transition level plus a hysteresis level, the system enters low-power mode. For the hysteresis, levels in the range from 5 % to 50 % can be selected, which are related to the selected LP-BM transition level. So, if the rated output at 100 % is 100 W, the LP-BM transition is set at 10 %, and the hysteresis at 50 %, the system switches from burst mode to low-power mode at a level of 15 W.

BM-LP transition level filter

When the output power slowly increases, the system ensures a smooth transition when leaving burst mode and entering low-power mode by setting a burst-mode-to-low-power-mode transition filter. When the output power exceeds the BM-LP transition level plus hysteresis for 2, 4, 8, or 16 burst cycles, it leaves the burst mode and enters the low-power mode. At a large transient at the output, the system immediately leaves burst mode.

BM repetition frequency

When the system operates in burst mode, it is regulated to a fixed frequency. This frequency can be set to different values ranging from 20 Hz to 3.2 kHz.

BM E/C (Energy-per-cycle) increase

As the TAA6065AT regulates the output via the primary capacitor voltage, it offers the ability to increase the output power per switching cycle when it enters burst mode. For the increase of output power per switching cycle, also called E/C (Energy-per-cycle), different values can be set ranging from 1 to 4. When, for instance, the E/C is set to 4, the system increases the E/C with a factor of 4 when it enters burst mode. The initial duty cycle is then 25 %. Increasing the E/C in burst mode increases the efficiency of the system, but at the cost of a higher output voltage ripple.

BM minimum cycles

As additional soft-start and soft-stop cycles reduces the audible noise, it increases the switching losses. To optimize the number of normal switching cycles in relation to the added soft-start and soft-stop switching cycles, the minimum number of normal switching cycles that can be selected ranges from 1 to 12.

Burst end SNSFB current

When the system operates in burst mode, it adjusts the number of switching cycles such that burst frequency corresponds to the selected burst frequency. If during these switching cycles the output load decreases, the output voltage increases as the system has calculated the number of required switching cycles. If the measured optocoupler current at the SNSFB pin exceeds a certain level, the system ends the burst switching cycle. This level can be between a factor of 2.5, 3.75, 5, or 7.5 times the selected optocoupler current level.

Burst-mode exit delay

When the LLC is switching for a time that exceeds the burst-mode exit delay time and the output load exceeds the burst-mode level, the system leaves the burst mode. The burst-mode exit delay time ($t_{burst\text{-}exit}$) can be set from 160 µs to 4 ms in 16 steps.

Low-power frequency

The frequency of the low-power mode can be selected by defining the ringing number at which the next low-power cycle must be started. The selection options are from 1 to 8 in steps of 1.

SNSHV compensation

A ripple at the input voltage of an LLC converter normally results in a ripple in the output voltage. To minimize the ripple at the output voltage, the TAA6065AT measures the input voltage of the LLC via the SNSHV pin and compensates the SNSCAP voltage via a feed-forward compensation. As the required compensation depends on the external components, it can be set at 8 different compensation levels.

8.7.3 Protection settings

8.7.3.1 General protections

Fast latch reset delay time

When the system does not detect a mains voltage for a programmed period, it assumes that the mains is disconnected and resets all protections. When the mains voltage exceeds the brownin level again, the system restarts. The delay between detecting a brownout (including the brownout delay time) and resetting all protections can be programmed to different values ranging from 0 s to 10 s.

Safe restart time

When the system is in protection mode and the triggered protection is programmed as safe restart, it restarts after a safe-restart time. This time can be set at different values ranging from 0.5 s to 10 s.

Fast disable

When the SNSHV voltage is pulled below the $V_{scp(stop)}$ level, the system enters the protection state. The response can be set to on/off, latched, or safe restart.

External OTP level

The external application temperature is measured via an NTC connected to the SNSNTC pin. To be able to set the appropriate NTC value and OTP level, the internal current used to measure the external NTC value can be set between 150 µA and 1050 µA in steps of 150 µA.

To avoid false triggering, an internal delay occurs before the system enters protection. This delay can be set to different values between 0.5 s and 8 s.

The response of the external OTP can be latched, safe restart, or latched after safe restart. The external OTP function can also be disabled.

Internal OTP level

The internal OTP is fixed at 135 °C.

8.7.3.2 LLC general protections

Maximum start-up time

When the LLC starts switching, it expects that its output voltage reaches the regulation level within a maximum start-up time. For the maximum start-up time, the following values can be selected: 25 ms, 50 ms, 100 ms, and 200 ms.

LLC brownout level (SNSHV)

When the voltage at the SNSHV drops below a predefined level, the LLC converter enters the protection state. When the SNSHV voltage exceeds the brownin level, the LLC converter starts switching again.

For the LLC brownout level at the SNSHV, a level in the range from 1.0 V to 2.05 V can be selected.

LLC brownin level (SNSHV)

The LLC brownin level defines the minimum voltage at the SNSHV pin before the LLC starts switching. For this level, a value ranging from 1.5 V to 2.4 V can be selected.

LLC maximum input voltage (SNSHV)

When an OVP is detected on the SNSHV pin, the response of the LLC can be set to either continue operation or stop switching. A delay can be set to either 5 ms, 50 ms, or 1250 ms.

Power limit

The maximum output power of the converter is limited by the controller. The limitation ensures that the applied load is below the maximum rating-selected components. For the maximum output power, several levels between 100 % and 200 % of the rated power can be selected.

OPP level 1

When the output power exceeds a first OPP level, a first counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level between 0 % and −50 % below the selected power limit can be selected.

For the time, a value between 50 ms to 40 s can be selected. The response of this protection can be latched, safe restart, or latched after safe restart. This OPP level can also be disabled.

OPP level 2

When the output power exceeds a second OPP level, a second counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level in the range from −10 % to −50 % below the selected power limit can be selected.

For the time, a value ranging from 50 ms to 3 s can be selected. The response of this protection follows the selected response of the OPP level 1. This OPP level can also be disabled.

OPP duty cycle

When the output power exceeds the OPP with a duty cycle of 50 %, the OPP may or may not be triggered. So, the duty cycle at which the OPP is triggered eventually can be set using a parameter to 11 %, 20 %, 33 %, or 50 %.

OVP protection

In a resonant converter, the voltage at the SUPIC pin reflects the output voltage. When the SUPIC voltage exceeds a defined level, the OVP protection is triggered. The level can be set between 1 V and 16 V above the start level in steps of 1 V.

To avoid false triggering, a delay can be set at different values ranging from 10 µs to 800 µs. The response of this protection can be latched, safe restart, or latched after safe restart. This OVP function can also be disabled.

OVP duty cycle

To minimize the sensitivity of the OVP function, a duty cycle can be set at which the OVP is eventually triggered. This parameter can be set to 11 %, 20 %, 33 %, or 50 %. If, for example, the OVP delay is set to 800 µs, the duty cycle to 50 %, and the SUPIC voltage exceeds the OVP level for 300 µs and drops to below the OVP level for 500 µs, the OVP is never triggered.

OCP protection

The current in the resonant tank is measured at the SNSCURLLC pin. When the voltage at this pin exceeds the OCP level, the corresponding switch (GATELS or GATEHS) is turned off and the system starts the next cycle. So, the LLC current is limited cycle-by-cycle.

If the OCP occurs for a defined number of cycles, the OCP protection is triggered. The number of cycles can be set to different values between 5 and 1000.

The response of this protection can be latched, safe restart, or latched after safe restart. The OCP protection function can also be disabled. However, the LLC current remains limited cycle-by-cycle.

8.7.4 Power good settings

The power good function gives a prewarning to the load that the converter is switched off due to disconnected mains or a triggered protection.

Power good time

The power good time is the time between the power good signal indicating that the converter is about to be switched off and the time the converter eventually stops switching. This delay can be set to 4 ms, 6 ms, 8 ms, or 10 ms.

Power good at OTP

The power good signal can give a prewarning when the converter is switched off due to an OTP detection. The OTP can be either an internal or an external OTP.

This function can be enabled or disabled. The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time.

Power good at OPP

The power good signal can give a prewarning when the converter is switched off due to an OPP detection. The prewarning can be given when the output power exceeds the OPP level1 or OPP level2 for the defined time.

This function can be enabled or disabled. The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time.

Power good at LLC brownout level (SNSHV)

When the measured voltage at the SNSHV pin drops to below the selected LLC brownout level, the LLC converter stops switching. It normally occurs due to a disconnected HV battery.

The power good signal can give a prewarning when the converter is switched off due to this LLC brownout detection. When the voltage at the SNSHV drops to below a selectable value, the power good feature is triggered. The level can be selected between 1 V and 2.05 V.

Power good at OVP (SNSHV)

The TAA6065AT offers a setting option to stop the LLC operation at an SNSHV OVP. When the LLC converter is switched off due to an SNSHV OVP, the power good signal can give a prewarning. This function can be enabled or disabled. The delay between the transition of the power good signal and the moment the converter stops switching equals the power good time.

Power good ready delay

When the output voltage is in regulation after start-up, power good indicates that the output voltage is in regulation. A delay can be set between the time the output voltage reaches the regulation level and the transition of the power good signal. This delay can be set at different values between 0 s and 1 s.

Power good transition time

The power good function is combined with the feedback network connected at the SNSFB pin. To avoid that a trigger of the power good function disturbs the regulation loop, its transition time must have a predefined value. This time can be set at 0.85 ms, 1.8 ms, 2.6 ms, or 3.5 ms.

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 14); positive currents flow into the chip. Voltage ratings are valid, provided other ratings are not violated; current ratings are valid, provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHV}	voltage on pin SUPHV	during surge t < 0.5 s; 10 times at a 0.1 Hz interval	−0.4	+685	V
SR_{SUPHV}	slew rate on pin SUPHV		−50	+50	V/ns
V_{SUPIC}	voltage on pin SUPIC		−0.4	+36	V
V_{SUPHS}	voltage on pin SUPHS	during surge t < 0.5 s; 10 times at a 0.1 Hz interval	−0.3	+685	V
		regarding pin HB	−0.4	+13	V
V_{GATEHS}	voltage on pin GATEHS		V_{HB} − 0.4	V_{SUPHS} + 0.4	V
V_{HB}	voltage on pin HB	during surge t < 0.5 s; 10 times at a 0.1 Hz interval	−0.3	+685	V
		t < 1 µs	−13	-	V
SR_{HB}	slew rate on pin HB		−70	+70	V/ns
V_{GATELS}	voltage on pin GATELS	[1]	−0.4	+14	V
V_{NF2}	voltage on pin NF2		−0.4	+14	V
V_{SNSCAP}	voltage on pin SNSCAP		−0.4	+12	V
$V_{SNSCURLLC}$	voltage on pin SNS CURLLC		−0.4	+12	V
V_{NF1}	voltage on pin NF1	DC; maximum	−0.4	+12	V
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
V_{SNSHV}	voltage on pin SNSHV		−0.4	+12	V
V_{SNSNTC}	voltage on pin SNSNTC		−0.4	+12	V
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.7	W
T_j	junction temperature		−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
Latch-up					
I_{lu}	latch-up current	all pins; according to JEDEC; standard 78D	−100	+100	mA

Table 5. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 14); positive currents flow into the chip. Voltage ratings are valid, provided other ratings are not violated; current ratings are valid, provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	human body model			
		SUPHS, GATEHS, HB, and SUPHV pins	−1000	+1000	V
		other pins	−2000	+2000	V
		charged device model			
		all pins	−500	+500	V

[1] Although the GATELS pin is an output pin, the maximum voltage of this pin must not exceed the maximum drive output voltage by 20 %.

10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUPHV}	voltage on pin SUPHV		-	440	V
V_{SUPHS}	voltage on pin SUPHS		-	440	V
V_{HB}	voltage on pin HB		-	440	V

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC test board	107	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	In free air; JEDEC test board	60	K/W

12 Characteristics

Table 8. Characteristics

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPHV pin						
$I_{off(SUPHV)}$	off-state current on pin SUPHV	V_{SUPHV} = 400 V; V_{SUPIC} = 19 V	2	5	9	µA
V_{SUPHV}	voltage on pin SUPHV	V_{SUPIC} = 19 V; I_{SUPHV} = 3 mA	22	26	30	V
$I_{ch(SUPIC)}$	charge current on pin SUPIC	V_{SUPHV} = 50 V; V_{SUPIC} = 19 V	−14	−6.5	−2	mA
SUPIC pin						
$V_{start(SUPIC)}$	start voltage on pin SUPIC		18.0	19.0	19.7	V
$V_{start(hys)SUPIC}$	start voltage hysteresis on pin SUPIC		−0.9	−0.7	−0.5	V
$V_{low(hys)SUPIC}$	low voltage hysteresis on pin SUPIC		0.5	0.7	0.9	V
$V_{low(SUPIC)}$	low voltage on pin SUPIC		11.5	12.0	12.5	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		9.5	10.0	10.4	V
$\Delta_{(vlow-vuvp)SUPIC}$	low voltage to undervoltage protection voltage difference on pin SUPIC	$V_{low} - V_{uvp}$	1.6	2.0	2.4	V
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC		8.6	9.0	9.4	V
$I_{CC(SUPIC)}$	supply current on pin SUPIC	non-operating mode; [1] I_{snsfb} = −100 µA; I_{snscap} = −100 µA	700	890	1100	µA
		operating mode; [1] f_{HB} = 100 kHz; I_{snsfb} = −80 µA; I_{snscap} = −100 µA; driver pins open	6	8	10	mA
Output overvoltage protection						
$V_{O(ovp)SUPIC}$	output overvoltage protection voltage on pin SUPIC		27.5	28.7	29.8	V
$t_{d(ovp)SUPIC}$	overvoltage protection delay time on pin SUPIC		45	50	55	µs
SNSNTC pin						
NTC voltage sensing						
$I_{clamp(max)}$	maximum clamp current	V_{SNSNTC} = 9.5 V	2.5	3.5	4.5	mA

Table 8. Characteristics...*continued*

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External overtemperature measurement						
$I_{o(SNSNTC)}$	output current on pin SNSNTC		−656	−600	−558	µA
$t_{det(max)NTC}$	NTC maximum detection time		45	50	55	µs
$V_{det(SNSNTC)}$	detection voltage on pin SNSNTC	NTC measurement; I_{SNNTC} = −600 µA	2.81	3.08	3.35	V
$t_{d(otp)}$	overtemperature protection delay time		3.6	4.0	4.4	s
SNSHV pin						
$I_{pd(SNSHV)}$	pull-down current on pin SNSHV	at $V_{SNSHV} = V_{scp(stop)}$	25	50	75	nA
$V_{stop(ovp)}$	overvoltage protection stop voltage	[2]	2.56	2.63	2.68	V
$V_{uvp(SNSHV)}$	undervoltage protection voltage on pin SNSHV		1.60	1.65	1.70	V
$V_{start(SNSHV)}$	start voltage on pin SNSHV		2.23	2.30	2.37	V
$V_{det(SNSHV)}$	detection voltage on pin SNSHV	Power good detection voltage	1.70	1.75	1.79	V
$\Delta V_{reg-det}$	voltage difference between regulation and detection	pin SNSHV; indication of the power good delay	0.71	0.75	0.79	V
Fast disable function						
$V_{scp(stop)}$	stop short-circuit protection voltage		0.37	0.39	0.42	V
$V_{scp(start)}$	start short-circuit protection voltage		0.40	0.45	0.50	V
$t_{fltr(scp)}$	short-circuit protection filter time		4	10	15	µs
SNSCAP pin						
$V_{AV(regd)SNSCAP}$	regulated average voltage on pin SNSCAP	regulated average of $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$	2.41	2.50	2.58	V
$I_{bias(max)SNSCAP}$	maximum bias current on pin SNSCAP		−245	−210	−175	µA
$V_{range(SNSCAP)}$	voltage range on pin SNSCAP	SNSCAP voltage range for the high-side comparator, $V_{hs(SNSCAP)}$	2.35	-	4.50	V
		SNSCAP voltage range for the low-side comparator, $V_{ls(SNSCAP)}$	0.5	-	2.65	V

Table 8. Characteristics...*continued*

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{th(SNSCAP)}$	threshold voltage difference on pin SNSCAP	$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 200 %; V_{SNSHV} < 1.9 V	3.05	3.27	3.58	V
		$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 100 %; V_{SNSHV} = 2.5 V	0.93	1.01	1.09	V
t_d	delay time	delay between exceeding V_{caph}/V_{capl} and driver off; dV/dt = 0.1 V/µs	-	-	125	ns
SNSCURLLC pin						
$V_{bias(SNSCURLLC)}$	bias voltage on pin SNSCURLLC		2.4	2.5	2.6	V
$R_{O(SNSCURLLC)}$	output resistance on pin SNS CURLLC		45	55	65	kΩ
$V_{lmtr(ocp)}$	overcurrent protection voltage limiter	soft-start overcurrent limiter	0.64	0.75	0.84	V
$V_{ocp(LLC)}$	LLC overcurrent protection voltage	positive level; $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$	1.30	1.50	1.66	V
		negative level; $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$	−1.66	−1.50	−1.30	V
$V_{reg(capm)}$	capacitive mode regulation level	positive level; $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$	83	100	116	mV
		negative level; $V_{SNSCURLLC} - V_{bias(SNSCURLLC)}$	−116	−100	−83	mV
$V_{det(zero)}$	zero detection voltage	detected as ≥ 0	−16	−11	−6	mV
		detected as ≤ 0	6	11	16	mV
SNSFB pin						
$V_{low(SNSFB)}$	low voltage on pin SNSFB	indicating iPowerGood = '1'; 0 µA < I_{opto} < 3.5 mA	0.42	0.50	0.58	V
$V_{high(SNSFB)}$	high voltage on pin SNSFB	indicating iPowerGood = '0'; 0 µA < I_{opto} < 3.5 mA	3.3	3.5	3.8	V
$t_{t(powergood)}$	powergood transition time		1.5	1.8	2.0	ms
Optobias regulator						
$I_{reg(SNSFB)}$	regulation current on pin SNSFB		−95	−80	−70	µA
Burst mode regulator						
$I_{start(burst)}$	burst mode start current	LLC burst mode	−112	−100	−88	µA
$I_{stop(burst)}$	burst mode stop current		−223	−200	−180	µA

Table 8. Characteristics...*continued*

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Burst mode						
$f_{burst(max)}$	maximum burst mode frequency		720	800	880	Hz
$t_{d(burst)exit}$	burst-mode exit delay time		3.6	4.0	4.4	ms
Power good characteristics						
$t_{d(powergood)}$	power good delay time	delay power good after output voltage ready	4.5	5.0	5.5	ms
		power good delay before protection	3.6	4.0	4,4	ms
LLC timing						
$t_{on(min)LLC}$	LLC minimum on-time		1105	1230	1355	ns
$t_{on(max)LLC}$	LLC maximum on-time		18	20	22	µs
Overpower protection						
$t_{startup(max)}$	maximum start-up time		90	100	110	ms
$t_{d(opp)}$	overpower protection delay time	OPP 1	45	50	55	ms
HB pin						
$\Delta V_{det(min)}/\Delta t$	minimum slope detection voltage	positive and negative minimum slope detection level	-	-	120	V/µs
$\Delta V_{det(max)}/\Delta t$	maximum slope detection voltage	positive and negative maximum slope detection level	50	-	-	V/ns
$t_{no(min)}$	minimum non-overlap time		200	230	260	ns
$t_{no(max)}$	maximum non-overlap time		0.99	1.10	1.21	µs
GATELS pin						
$I_{source(peak)}$	source peak current	C_{load} = 4.7 nF; V_{SUPIC} ≥ 13 V [1]	−1.1	−0.9	−0.7	A
$I_{sink(peak)}$	sink peak current	C_{load} = 4.7 nF; V_{SUPIC} ≥ 13 V [1]	0.7	1.0	1.3	A
$R_{OH(GATELS)}$	HIGH-level output resistance on pin GATELS	I_{GATELS} = −30 mA; V_{SUPIC} = 14.5 V	-	-	20	Ω
$R_{OL(GATELS)}$	LOW-level output resistance n pin GATELS	I_{GATELS} = 30 mA; V_{SUPIC} = 14.5 V	-	-	6	Ω
$V_{OH(GATELS)}$	HIGH-level output voltage on pin GATELS	f_{sw} = 100 kHz; I_{load} = 0; V_{SUPIC} ≥ 14.5 V [1]	11.5	12.3	13.1	V
		f_{sw} = 100 kHz; I_{load} = 0; V_{SUPIC} = 9.5 V [1]	9.45	9.50	9.55	V
$V_{OL(GATELS)}$	LOW-level output voltage on pin GATELS	I_{GATELS} = 40 mA; V_{SUPIC} ≥ 14.5 V	0.10	0.17	0.24	V

Table 8. Characteristics...*continued*

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(GATELS)}$	rise time on pin GATELS	1 V to 9 V; V_{SUPIC} = 13 V; 1 nF load [1]	10	15	20	ns
$t_{f(GATELS)}$	fall time on pin GATELS	9 V to 1 V; V_{SUPIC} = 13 V; 1 nF load [1]	10	15	20	ns
GATEHS pin						
$I_{source(peak)}$	source peak current	C_{load} = 4.7 nF; $V_{SUPHS} - V_{HB}$ = 12 V [1]	−0.8	−0.6	−0.4	A
$I_{sink(peak)}$	sink peak current	C_{load} = 4.7 nF; $V_{SUPHS} - V_{HB}$ = 12 V [1]	0.8	1.1	1.4	A
$R_{OH(GATEHS)}$	HIGH-level output resistance on pin GATEHS	I_{GATEHS} = −30 mA; $V_{SUPHS} - V_{HB}$ = 12 V	-	-	18	Ω
$R_{OL(GATEHS)}$	LOW-level output resistance on pin GATEHS	I_{GATEHS} = 30 mA; $V_{SUPHS} - V_{HB}$ = 12 V	-	-	9	Ω
$V_{OH(GATEHS)}$	HIGH-level output voltage on pin GATEHS	f_{sw} = 100 kHz; I_{load} = 0; $V_{SUPHS} - V_{HB}$ = 12 V [1]	11.5	12.0	12.5	V
$V_{OL(GATEHS)}$	LOW-level output voltage on pin GATEHS	I_{GATEHS} = 40 mA; $V_{SUPHS} - V_{HB}$ = 12 V	0.1	0.2	0.3	V
$t_{r(GATEHS)}$	rise time on pin GATEHS	1 V to 9 V; $V_{SUPHS} - V_{HB}$ = 11 V; 1 nF load [1]	15	25	35	ns
$t_{f(GATEHS)}$	fall time on pin GATEHS	9 V to 1 V; $V_{SUPHS} - V_{HB}$ = 11 V; 1 nF load [1]	10	15	20	ns
SUPHS pin						
$V_{rst(SUPHS)}$)	reset voltage on pin SUPHS	+25 °C < T < 125 °C	5.5	7.2	8.5	V
System protection						
$t_{d(restart)}$	restart delay time		0.9	1.0	1.1	s
$t_{d(flr)}$	fast latch reset delay time		45	50	55	ms
I^2C communication						
V_{IL}	LOW-level input voltage		0.0	-	0.8	V
V_{IH}	HIGH-level input voltage		1.4	-	5.0	V
$I_{pd(SNSCAP)}$	pull-down current on pin SNSCAP	To ensure proper operation, the external pull-up must always be lower than 6.8 mA. [3]	6.8	-	-	mA

Table 8. Characteristics...*continued*

T_{amb} = −40 °C to +125 °C; T_j = −40 °C to +150 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overtemperature protection						
T_{otp}	overtemperature protection trip		120	135	150	°C

[1] Covered by correlating measurement
[2] TAA6065AT MTP programming: "Disable LLC after SNSHV OVP" = off
[3] As the minimum limit determines the application design, the maximum limit is not relevant.

13 Application information

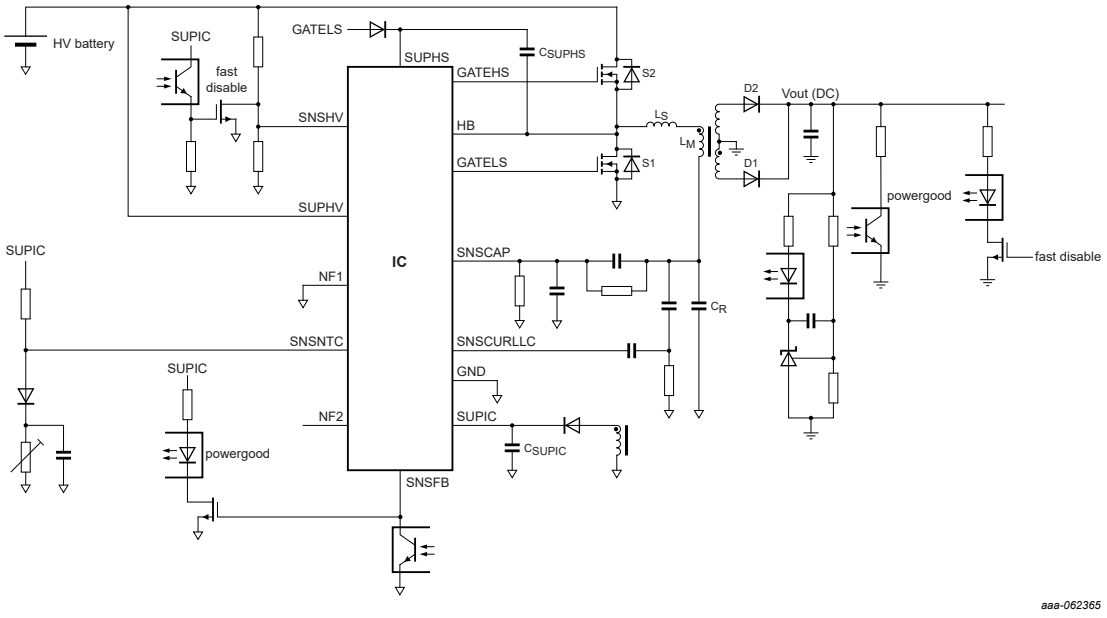


Figure 21. Application diagram

14 Ringo parameter settings

Table 9. Ringo parameter/IC parameter settings

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
1	NXP ID code	nxp_id_code	0x01	-	1
2	SNSHV OVP (SNSHV)	boost_ovp_snsboost	OK	-	0
3	LLC OPP 1	llc_opp1	OK	-	0
4	LLC OPP 2	llc_opp2	OK	-	0
5	LLC maximum start-up time	llc_max_startup_time	OK	-	0
6	LLC OCP	llc_ocp	OK	-	0
7	LLC OVP	llc_ovp_prot	OK	-	0
8	External OTP	ext_otp	OK	-	0
9	Internal OTP	int_otp	OK	-	0
10	Fast disable	fast_disable	OK	-	0
11	LLC maximum on-time	llc_max_on_time	OK	-	0
12	LLC maximum Iopto	llc_max_iopto	OK	-	0
13	LLC capacitive mode	llc_cap_mode	OK	-	0
14	MTP read failure	mtp_read_fail	OK	-	0
15	OPP via SUPIC UVP	opp_via_supic_uvp	OK	-	0
16	Write lock	write_lock	write enabled	-	0
17	Read lock	read_lock	read enabled	-	0
18	SUPIC resistor value	supic	20	MΩ	0
19	SUPIC SNS resistors	nr_supic_resistors	1	resistor	0
20	LLC soft-start speed	llc_tsoftstart	7	X	0
21	SUPIC control near UVP	dis_vlow	enabled	-	0
22	SUPIC start level	sup_start	19	V	0
23	LLC converter	llc_disable	enabled	-	0
24	Vdump level	vdump	2.55	V	1
25	Capacitive mode regulation level	capm_lvl	100	mV	0
26	Maximum on-time	llc_max_on	20	µs	0
27	LLC LP mode	lpmode_dis	enabled	-	0
28	OTP/external burst mode select	ext_burstmode	Ext OTP	-	0
29	LLC non-overlap mode	llc_non_overlap	adaptive	-	0
30	Maximum non-overlap time	t_no_max	1.1	µs	0
31	Minimum non-overlap time	t_no_min	230	ns	0

Table 9. Ringo parameter/IC parameter settings*...continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
32	Opto current level	iopto	80	µA	0
33	Burst-on end by opto current	iopto_bm_end	2.5	X	0
34	SNSHV compensation	snsb_comp	−1.4	-	0
35	HP-LP transition level	hp_lp_lev	30	%	0
36	HP-LP hysteresis	hp_lp_hys	20	%	0
37	Opto regulation level	opto_reg_level	standard	-	0
38	Opto regulation gain increase	opto_reg_gain_incr	96	-	0
39	LP number of peaks	lp_nr_peaks	2	-	0
40	LP-BM transition level	lp_bm_lev	10	%	0
41	BM-LP hysteresis	bm_lp_hys	50	%	7
42	BM LP hysteresis filter	bm_lp_filt	4	-	0
43	LP-BM delay time	lp_bm_del	0	s	0
44	Zero power slope	min_slope	6	mV/µs	0
45	dVcap offset	vcap_offset	0	mV	0
46	BM frequency	bm_freq	800	Hz	0
47	BM energy-per-cycle increase	bm_incr	1	X	0
48	Minimum cycles in burst	min_nr_cycl	3	-	0
49	Number of BM soft-start cycles	nr_bm_sstart	2	-	2
50	Number of BM soft-stop cycles	nr_bm_sstop	2	-	2
51	Burst mode exit delay	bm_exit_del	4000	µs	0
52	Slope of 4th BM soft-start cycle	start_cycle4	2	-	0
53	Slope of 3rd BM soft-start cycle	start_cycle3	6	-	0
54	Slope of 2nd BM soft-start cycle	start_cycle2	10	-	5
55	Slope of 1st BM soft-start cycle	start_cycle1	96	-	0
56	Slope of 4th BM soft-stop cycle	stop_cycle4	96	-	0
57	Slope of 3rd BM soft-stop cycle	stop_cycle3	24	-	0
58	Slope of 2nd BM soft-stop cycle	stop_cycle2	10	-	4
59	Slope of 1st BM soft-stop cycle	stop_cycle1	4	-	2
60	External OTP current level	eotp_lvl	600	µA	0
61	External OTP delay time	t_eotp	4	s	0
62	OTP mode	otp_ltch	safe restart	-	0
63	OTP number of restarts to latch	otp_nr_rest	0	-	0

Table 9. Ringo parameter/IC parameter settings*...continued*

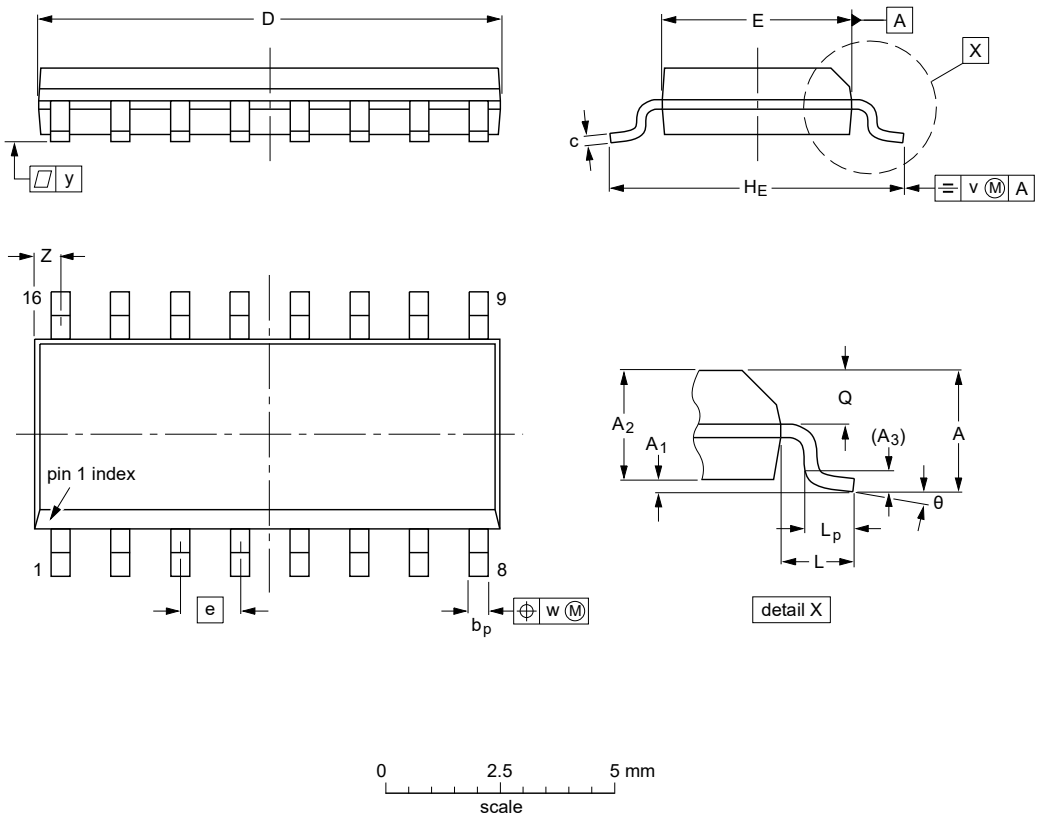
	Ringo parameter name	IC parameter name	Value	Unit	Binary value
64	Fast disable by SNSHV	llc_fast_disable	latched	-	3
65	Fast latch reset delay time	t_flr	50	ms	0
66	Safe restart timer	sr_time	1	s	0
67	HV OVP level (SNSHV)	ovp_lvl	2.63	V	0
68	LLC soft-start current limit	max_llc_istartup	0.75	V	0
69	Maximum (start-up) frequency	max_llc_freq	350	kHz	0
70	Maximum start-up time	t_start_max	100	ms	0
71	LLC maximum ringing time	max_tring_llc	5	µs	0
72	LLC OCP filter	llc_tocp	5	-	0
73	LLC OCP mode	llc_ocp_ltch	safe restart	-	0
74	OCP restarts to latch	llc_ocp_nr_rest	0	-	0
75	LLC (SUPIC) OVP level	llc_ovp	10	V	0
76	LLC (SUPIC) OVP delay	llc_tovp	50	µs	0
77	Down-counts/up-count (SUPIC) OVP	llc_ovp_nr_dwn	1	-	0
78	(SUPIC) OVP mode	llc_ovp_ltch	safe restart	-	0
79	OVP restarts to latch	llc_ovp_nr_rest	0	-	0
80	LLC brownin level (SNSHV)	snsb_start	2.3	V	6
81	LLC brownout level (SNSHV)	snsb_stop	1.65	V	3
82	Disable LLC after SNSHV OVP	dis_ovp_snsb	off	-	3
83	OPP1 level	opp1_lvl	−20	%	0
84	OPP1 time delay	opp1_time	50	ms	0
85	Fast disable FLR	fast_disable_flr	FD not starts FLR	-	0
86	OPP2 level	opp2_lvl	−10	%	0
87	OPP2 time delay	opp2_time	infinite	-	0
88	Down-counts/up-count OPP	opp_nr_dwn	1	-	0
89	OPP mode	opp_ltch	safe restart	-	0
90	OPP restarts to latch	opp_nr_rest	0	-	0
91	LLC power limitation level	pow_lim	155	%	0
92	Power good inverted	pgood_inv	disabled	-	0
93	Power good SNSHV reset level	pgd_lvl	1.75	V	0
94	Power good at OPP	pgd_opp	enabled	-	0
95	Power good at OTP	pgd_otp	enabled	-	0

Table 9. Ringo parameter/IC parameter settings*...continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
96	Power good signal at SNSHV OVP	pgd_ovp_sbo	enabled	-	0
97	Power good signal edge (SNSFB)	pgd_tr	1.8	ms	0
98	Power good delay	pgd_del	5	ms	0
99	Power good time to protection	pgd_tim	4	ms	0
100	Vendor code	mtp_code	0	-	0

15 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 22. Package outline SOT109-1 (SO16)

16 Revision history

Table 10. Revision history

Document ID	Release date	Description
TAA6065AT v.1.0	03 September 2025	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Tables

Figures

Contents