

## 1 General description

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ICODE 3 High-cap is a new contactless HF-RFID chip with 97pF internal tuning capacitance. The chip offers strong RF performance. It features a customizable digital Originality signature, to assure tag origin in cloning detection, and offers enhanced privacy modes to protect user privacy. It is operated at 13.56MHz from long-range HF-RFID readers and NFC phones, to support cross-range operations across manufacture, supply, and usage chains. It is fully compatible with the ISO/IEC 15693 standard and NFC Forum Type 5 tag.

Fully backward-compatible with SLIX 2, the ICODE 3 supports new features:

- Fast read with up to 212 kbit/s
- Configurable 24-bit counter
- ASCII mirror feature option
- One-shot read-only memory lock
- Extra configuration memory with optional password protection
- Programmable originality signature with 32 bytes or 48 bytes
- 2.4 kbit user memory size
- Flexible user memory segmentation with separate access conditions

## 1.1 Contactless energy and data transfer

The ICODE 3 can be operated at a distance of up to 1.5 m (gate width). No battery is needed.

The device is operated with easy-to-produce types of antennas<sup>1</sup> for the 13.56 MHz carrier frequency.

When the smart label is positioned in the field of an interrogator antenna, the high-speed RF communication interface enables data transmission at up to 212 kbit/s.

## 1.2 Anticollision

The anticollision algorithm selects each tag individually. This ensures that the execution of a transaction with a selected tag is performed without data corruption from other tags in the field.

## 1.3 Data protection

- Unique Identifier (UID):  
The UID guarantees the uniqueness of each label, and cannot be altered.
- Tag originality signature:  
32-byte or 48-byte ECC-based originality signature.
- Password protected memory management (Read/Write access):  
The user memory can be segmented into two pages. The read/write access rights can be defined for each page. Only authorized users get read/write access to the protected parts of the user memory (anticounterfeiting). READMULTIPLE BLOCK and (FAST) INVENTORY READ are compatible to ICODE SLIX 2.
- Password protected label Destroy:  
The 32-bit Destroy password enables an addressed label to be destroyed with the DESTROY command. The status is irreversible and the label never responds to any command again.
- Password-protected privacy modes:  
ICODE 3 supports two privacy modes to hide the original UID. A 32-bit password is used to enable or disable the privacy modes. This feature complies with the demand for data privacy.
- Password protected EAS and AFI functionality:  
The 32-bit EAS/AFI password enables the addressed label to be set in a mode where the EAS status, the EAS ID and/or the AFI value can only be changed if the correct EAS/AFI password is first transmitted with the SET PASSWORD command.
- 24-bit counter:  
The last block of the user memory is used for the 24-bit counter feature. The counter can be configured as a command-based counter or as an NFC counter. The NFC counter automatically increases by one when tapped with an NFC reader device.

<sup>1</sup> For example, antennas made out of a few windings printed, wound, etched or punched coil.

## 2 Features and benefits

### 2.1 ICODE 3 RF interface (ISO/IEC 15693)

- Contactless transmission of data and power (no battery needed)
- Operating distance of up to 1.5 m (depending on the antenna geometry)
- Operating frequency of 13.56 MHz (ISM, worldwide license freely available)
- Fast data transfer of up to 212 kbit/s
- High data integrity: 16-bit CRC, framing
- True anticollision feature
- Persistent quiet mode to enable faster inventory speed
- Write distance equal to read distance
- 97 pF internal resonance capacitance for small antenna form factors

### 2.2 EEPROM

- 2432 bits of user memory organized in 76 blocks of 4 bytes each. The last block is reserved for the 24-bit counter feature.
- 50 years of data retention
- Write endurance of 100,000 cycles

### 2.3 Data protection

- 8-byte unique identifier
- 32-byte or 48-byte programmable originality signature
- Lock mechanism for each user memory block (write protection), and lock protection pointer for fast locking
- Lock mechanism for DSFID, AFI, EAS
- Password (32-bit) protected memory management for Read access
- Password (32-bit) protected memory management for Write access
- Password (32-bit) protected label Destroy
- Password (32-bit) protected privacy mode
- Password (32-bit) protected EAS and AFI functionality
- Password (32-bit) protected memory configuration
- 24-bit counter (NFC counter, or command-based counter with optional password protection)

### 3 Applications

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- Product identification
- Product tracking and tracing
- Counterfeit protection
- Inventory management
- Smart-device consumable system communication
- Augmented mobile interaction

4 Ordering information

Table 1. Ordering information

Part number	Package		Version
		Description	
SL2S3103FUD	Wafer	sawn, 12" bumped wafer, 120 μm, on film frame carrier, C <sub>i</sub> between LA and LB = 97 pF (typical)	-

5 Block diagram

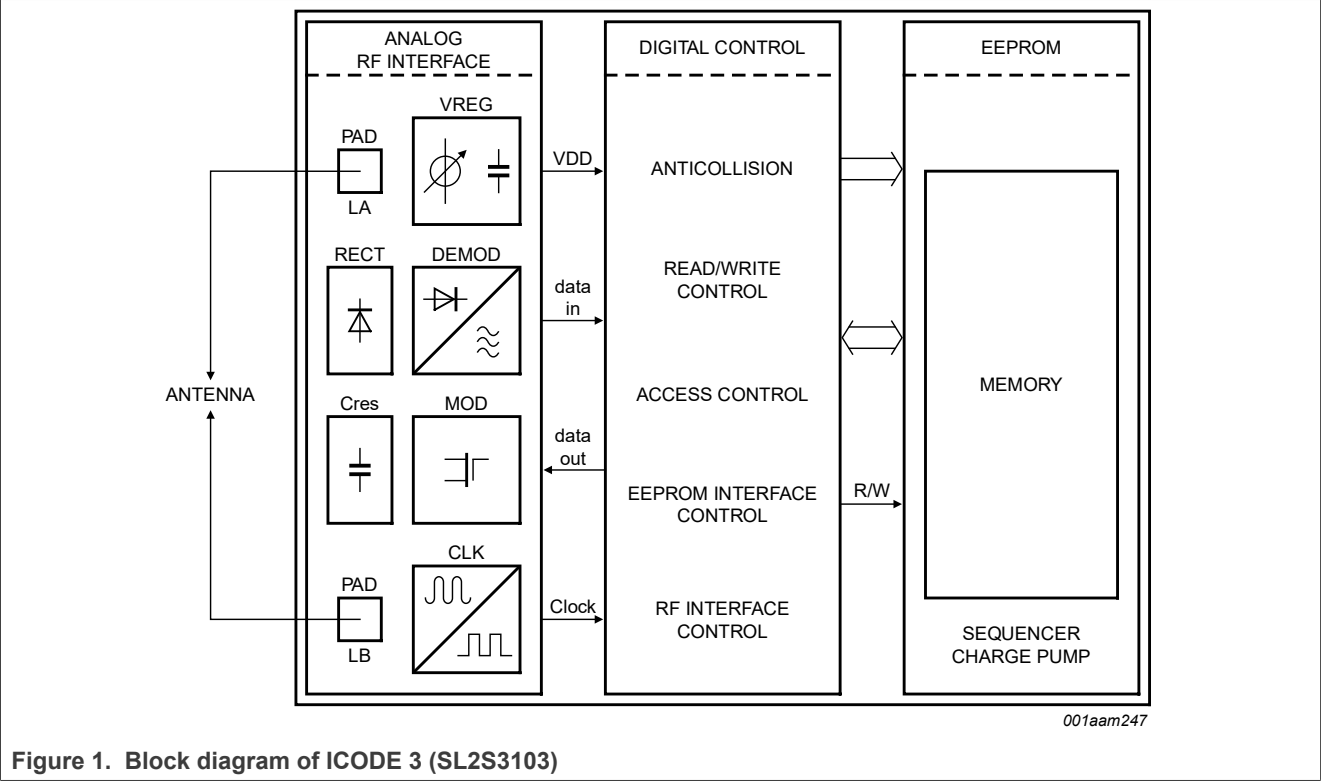
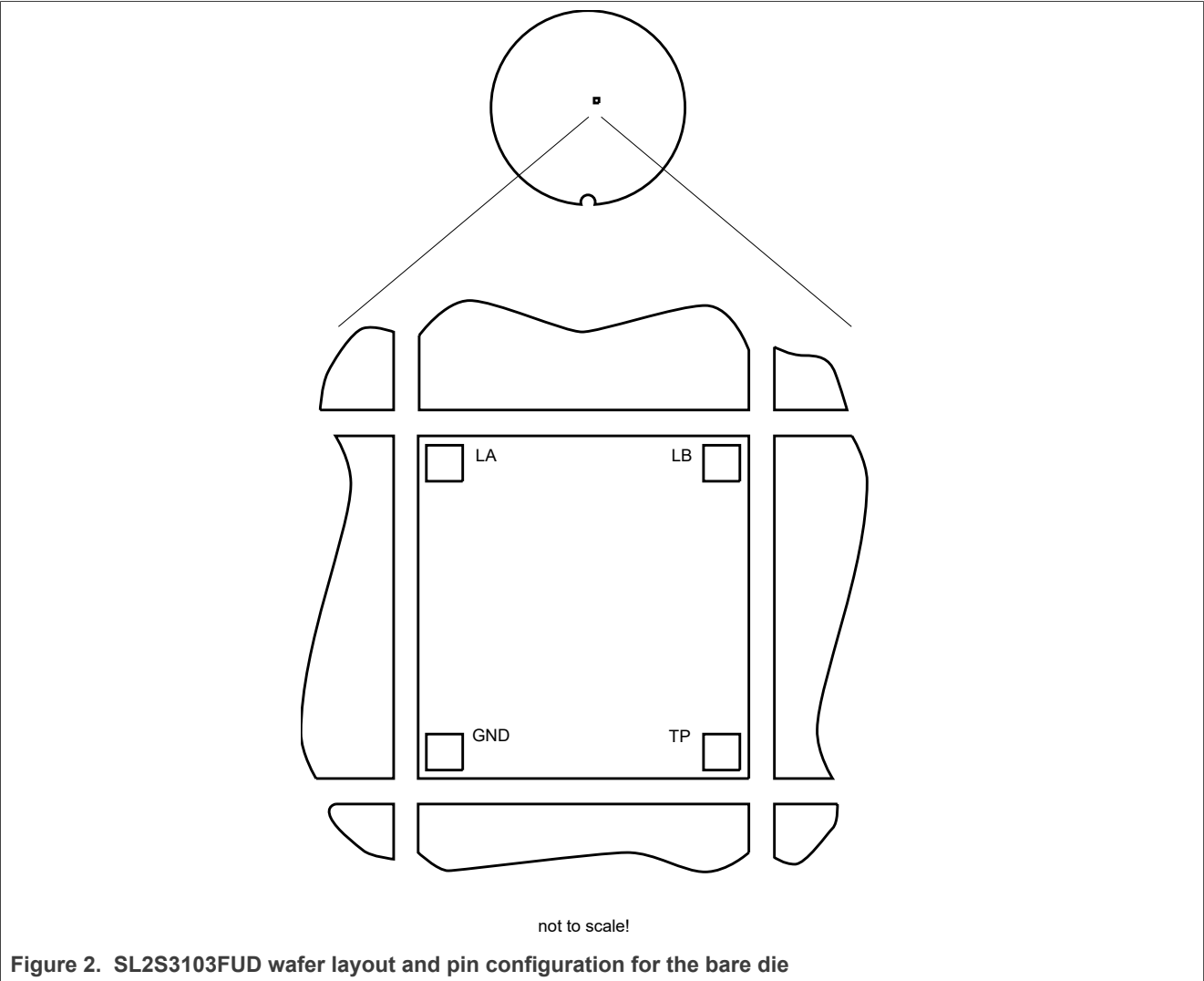


Figure 1. Block diagram of ICODE 3 (SL2S3103)

6 Wafer layout



6.1 Pin description

Table 2. Bonding pad description

Symbol	Description
LA	Antenna connection LA
LB	Antenna connection LB
GND	Ground (disconnected from internal circuitry)
TP	Test pin (disconnected from internal circuitry)

Refer to [ref.\[5\]](#).

## 7 Mechanical specification

### 7.1 Wafer specification

Refer to [ref.\[5\]](#).

Table 3. Wafer specification

Parameter	Value
<b>Wafer</b>	
Designation	each wafer is enscribed with batch number and wafer number
Diameter	300 mm (12 inches)
Thickness	120 $\mu\text{m}$ $\pm$ 15 $\mu\text{m}$
Process	CMOS 0.14 $\mu\text{m}$
Batch size	25 wafers
Dies per wafer	140037
<b>Wafer backside</b>	
Material	Si
Treatment	ground and stress release
Roughness	$R_a$ minimum = 0.5 $\mu\text{m}$
	$R_t$ maximum = 5 $\mu\text{m}$
<b>Chip dimensions</b>	
Die size without scribe	640 $\mu\text{m}$ $\times$ 660 $\mu\text{m}$ = 0.4224 mm <sup>2</sup>
<b>Scribe line width</b>	
X-dimension	35 $\mu\text{m}$ (scribe line width measured between nitride edges)
Y-dimension	35 $\mu\text{m}$ (scribe line width measured between nitride edges)
Number of pads	4
Pad location	non-diagonal/placed in chip corners
Distance pad to pad LA to LB	530 $\mu\text{m}$ (center to center)
Distance pad to pad LB to TP	550 $\mu\text{m}$ (center to center)
<b>Passivation on front</b>	
Type	sandwich structure
Material	PE-nitride (on top)
Thickness	1.75 $\mu\text{m}$ total thickness of passivation
<b>Au bump</b>	
Material	>99.9 % pure Au
Hardness	35 HV to 80 HV 0.005
Shear strength	>70 MPa
Height	18 $\mu\text{m}$



Table 3. Wafer specification...continued

Parameter	Value
<b>Height uniformity</b>	
within a die	±2 µm
within a wafer	±3 µm
wafer to wafer	±4 µm
Bump flatness	±1.5 µm
<b>Bump size</b>	
LA, LB	80 µm × 80 µm
TP, GND	80 µm × 80 µm
variation	±5 µm
Under bump metallization	sputtered TiW

7.1.1 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [ref.\[5\]](#).

7.1.2 Map file distribution

See [ref.\[5\]](#).

## 8 Functional description

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### 8.1 Block description

The ICODE 3 includes three major blocks: the analog RF interface, the digital controller, and the EEPROM.

#### Analog RF interface

The interrogator generates an electromagnetic field. The analog RF interface generates the stable power supply and the system clock from the electromagnetic field via the antenna. The ICODE 3 requires no internal power supply.

The analog RF interface also includes:

- The demodulator: Demodulates the data transmitted from the interrogator to the ICODE label. The data is then processed in the digital control block.
- The modulator: Modulates the electromagnetic field for data transmission from the ICODE label to the interrogator.

#### Digital control block

The digital control block includes the state machines. The block is used to process the data and to handle the communication with the EEPROM.

#### EEPROM

Data are stored in a non-volatile memory (EEPROM).

## 8.2 Memory organization

The 2432-bit user-accessible EEPROM memory is divided into 76 blocks. The block is the smallest access unit. Each block consists of 4 bytes or 32 bits. Bit 0 in each byte represents the least significant bit (LSB) and bit 7 is the most significant bit (MSB).

The entire memory is divided into two parts:

- User memory
  - The blocks 0 to 74 (2400 bits) are used to store the user data. Direct read/write access to this part of the memory is possible depending on the security and write protection conditions. The user memory can be accessed with the READ and WRITE commands.
  - The last block of the user memory (block 75) contains the 24-bit counter and the password protection flag of the counter.
- Configuration memory
  - This part of the memory stores the information to configure the ICODE 3. The configuration memory can be accessed with the READ CONFIG and WRITE CONFIG commands.

**Table 4. User memory organization**

Block	Byte 0	Byte 1	Byte 2	Byte 3	Description
0					User memory: 75 blocks, 4 bytes each, 300 bytes in total.
1					
2					
3					
:	:	:	:	:	
72					
73					
74					
75	C0	C1	C2	PROT	Counter

**Note:** Block 75 contains the 24-bit counter and cannot be used to store user data. READ and WRITE commands to that block require special data considerations (refer to [Section 8.5.3.24](#)).

**Table 5. Configuration memory organization**

Block	Byte 0	Byte 1	Byte 2	Byte 3	Description
0					Configuration memory: 48 blocks, 4 bytes each, 192 bytes in total.
1					
2					
3					
:	:	:	:	:	
44					
45					
46					
47					
48 - 127	RFU	RFU	RFU	RFU	Reserved configuration memory

8.2.1 Unique identifier

The 64-bit unique identifier (UID) is programmed during the production process according to ISO/IEC 15693-3 and cannot be changed afterward. For more information on the ISO standard, refer to [ref.\[3\]](#).

The 64 bits are numbered according to ISO/IEC 15693-3 starting with LSB 1 and ending with MSB 64. This is in contrast to the general used bit numbering within a byte.

The TAG type is a part of the UID (bits 41 to 48 next to the manufacturer code which is "04h" for NXP Semiconductors).

The TAG type of the ICODE 3 IC is "01h".

Bits 39 to 36 are used to identify the UID as ICODE 3.

Table 6. Unique identifier

MSB							LSB
64:57	56:49	48:41	40:1				
"E0"	"04"	"01"	IC manufacturer serial number				
UID 7	UID 6	UID 5	UID 4	UID 3	UID 2	UID 1	UID 0

Table 7. Type indicator bits

Bit 39	Bit 38	Bit 37	Bit 36	ICODE Type
0	1	0	0	ICODE 3

8.2.2 Originality signature

The ICODE 3 can verify the origin of a tag. The device compares the UID compared with an originality signature stored in the configuration memory. The originality signature can be read either with the READ SIGNATURE command (refer to [Section 8.5.3.20 "READ SIGNATURE"](#)), or with the READ CONFIG command (refer to [Section 8.5.3.21 "READ CONFIG"](#)). The outcome of the command is verified on the reader side.

The originality signature can be customized for specific applications. At delivery, the ICODE 3 is preprogrammed with the 32-byte NXP originality signature. The signature is unlocked in the dedicated memory. If needed, the signature can be reprogrammed with a custom-specific signature using the WRITE CONFIG command (refer to [Section 8.5.3.22 "WRITE CONFIG"](#)) during the customization process. Next, the signature can be permanently locked by setting the OTP\_OS\_LOCK bit to 1 with the WRITE CONFIG command to avoid further modifications.

The ICODE 3 can be configured with a 48-byte signature using the OS\_CFG\_MODE in the configuration memory (see [Table 39](#)). If the originality signature is set to 48 bytes, the customized signature must be programmed into blocks 0 to 11 in the configuration memory. Then the WRITE CONFIG command is used to set the configuration memory to "locked".

**Note:** If no customized originality signature is required, it is recommended to permanently lock the NXP signature during the initialization process by setting the configuration memory to "locked" with the WRITE CONFIG command.

8.2.2.1 Originality signature at delivery

At delivery, the ICODE 3 is programmed with a 32-byte NXP digital signature based on standard Elliptic Curve Cryptography (curve name secp128r1), according to the ECDSA algorithm [ref.\[6\]](#). The use of a standard algorithm and ECC curve ensures easy software integration. The originality check procedure in NFC devices does not require specific hardware. During production, each ICODE 3 UID is signed with an NXP private key. The resulting 32-byte signature is stored in the configuration memory blocks 0 to 7.

Table 8. Originality Signature location in the configuration memory

Config Block	Byte 0	Byte 1	Byte 2	Byte 3
0	OS_0 (LSB)	OS_1	OS_2	OS_3
1	OS_4	OS_5	OS_6	OS_7
:	:	:	:	:
6	OS_24	OS_25	OS_26	OS_27
7	OS_28	OS_29	OS_30	OS_31 (MSB)

Use the READ SIGNATURE command or the READ CONFIG command to retrieve the signature (refer to [Section 8.5.3.20 "READ SIGNATURE"](#)). Verify the signature in the NFC device by using the corresponding ECC public key provided by NXP [ref.\[7\]](#).

If the NXP public key is stored in the reader device, the complete signature verification procedure can be performed offline.

To verify the signature (for example with the use of the public domain cryptolibrary OpenSSL), set the tool domain parameters to secp128r1, defined within the standards for elliptic curve cryptography SEC [ref.\[6\]](#).

### 8.2.3 Configuration memory

The configuration memory stores the IC configuration settings. Direct access to this memory area is only possible with READ\_CONFIG and WRITE\_CONFIG commands depending on the initialization status.

The configuration lock bit locks only the access with the WRITE\_CONFIG command. Commands (WRITE\_AFI, LOCK\_AFI, WRITE\_PASSWORD, and others) that modify specific data fields in the configuration memory can still be used, if the related data fields are not locked.

- Blocks 26 - 31 (OTP bits)  
OTP bits can be set to 1 with the WRITE\_CONFIG command, writing of 0 is ignored. Each OTP bit is set to 1 one time. Each block with OTP bits must not be written more than four times with the WRITE\_CONFIG command.
- Block 38 (status bits)  
The bits in block 38 can only be read with the READ\_CONFIG command. Programming with the WRITE\_CONFIG command returns a response with the ERROR\_flag set to 1.
- Block 41 - 46 (passwords)  
If the password is not locked, the WRITE\_CONFIG or WRITE\_PASSWORD commands are used to program the password. See [Section 8.5.3.3 "WRITE\\_PASSWORD"](#). The READ\_CONFIG command masks all the passwords bytes with 00h.

**Note:** Use diversified passwords. Use passwords diversified per application for the privacy passwords. Use the configuration password only in trusted environments.

- RFU  
RFU marked fields are reserved for future use.

Table 9. Configuration memory blocks

Block Address	Byte number				
Dec	0	1	2	3	Access
0 - 7	OS 0 - 31				r/w
8 - 11	OS 32 - 47				r/w
12 - 15	RFU				
16	DSFID	RFU			
17	AFI	RFU			r/w
18	EAS ID0	EAS ID1	RFU		r/w
19	CID0	CID1	RFU		r/w
20	PPC_PNTR	PPC_CTRL	RFU		r/w
21	LP_PNTR	LP_CTRL	RFU		r/w
22	NFC_MIRROR_CTR	NFC_MIRROR_BLK	RFU		r/w
23	RFU				r/w
24 - 25	RFU				r
26	OTP_LOCK0	RFU			r/w
27	OTP_LOCK1	RFU			r/w
28	OTP_LOCK2	RFU			r/w
29	OTP_LOCK3	RFU			r/w
30	OTP_LOCK4	RFU			r/w
31	OTP_LOCK5	RFU			r/w
32	PRIVACY_MODE	RFU			r/w
33	COUNTER_CFG0	RFU			r/w
34	COUNTER_CFG1	RFU			r/w
35	OS_CFG	RFU			r/w
36 - 37	RFU				r
38	PRIVACY_STATUS	RFU	EAS_STATUS	RFU	r
39 - 40	RFU				r
41	CFG_PWD0 (LSB)	CFG_PWD1	CFG_PWD2	CFG_PWD3 (MSB)	w
42	READ_PWD0 (LSB)	READ_PWD1	READ_PWD2	READ_PWD3 (MSB)	w
43	WRITE_PWD0 (LSB)	WRITE_PWD1	WRITE_PWD2	WRITE_PWD3 (MSB)	w
44	PRIVACY_PWD0 (LSB)	PRIVACY_PWD1	PRIVACY_PWD2	PRIVACY_PWD3 (MSB)	w
45	DESTROY_PWD0 (LSB)	DESTROY_PWD1	DESTROY_PWD2	DESTROY_PWD3 (MSB)	w
46	EASAFI_PWD0	EASAFI_PWD1	EASAFI_PWD2	EASAFI_PWD3 (MSB)	w
47	RFU				r/w
48 - 127	RFU				

Table 10. PPC\_PNTR byte (Protect Page Pointer Address) configuration parameter descriptions

Field	Bit	Values at Delivery	Description
PPC_PTNR	8	0b	The Protection Pointer Address defines the base address for the password protection of the higher user memory segment Page H. All block addresses smaller than the protection pointer address are in the user memory segment Page L. <a href="#">Section 8.5.3.6</a>

Table 11. PPC\_CTRL byte (Protect Page Control)

Bit number							
0	1	2	3	4	5	6	7
RL	WL	RFU		RH	WH	RFU	

Table 12. PPC\_CTRL byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
RL	1	0b	Defines read password protection for Page L as defined with <a href="#">Section 8.5.3.6</a>
WL	1	0b	Defines write password protection for Page L as defined with <a href="#">Section 8.5.3.6</a>
RH	1	0b	Defines read password protection for Page H as defined with <a href="#">Section 8.5.3.6</a>
WH	1	0b	Defines write password protection for Page H as defined with <a href="#">Section 8.5.3.6</a>



Table 13. LP\_PNTR byte (Lock Protection Pointer Address) configuration parameter descriptions

Field	Bit	Values at Delivery	Description
LP_PNTR	8	0b	The Lock Pointer Address defines the block from which the user memory is divided into two pages (Page L and Page H) for the write lock (see in <a href="#">Section 8.5.2.3</a> ). All block addresses smaller than the Lock Pointer Address are in the user memory segment Page L. The lock conditions for those two pages L and H are defined with the settings in the LP_CTR byte (see in <a href="#">Table 14</a> ).

Table 14. LP\_CTRL byte (Lock Pointer Control)

Bit number							
0	1	2	3	4	5	6	7
LP_CTRL_L	LP_CTRL_H	RFU					

Table 15. LP\_CTRL byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
LP_CTRL_L	1	0b	Defines the write lock for Page L defined with the lock protection pointer byte LP_PNTR. Individual blocks can be write locked with the LOCK BLOCK command (refer to <a href="#">Section 8.5.2.3</a> ) 0b ... Page L is not write locked 1b ... Page L is write locked
LP_CTRL_H	1	0b	Defines the write lock for Page H defined with the lock protection pointer byte LP_PNTR. Individual blocks can be write locked with the LOCK BLOCK command (refer to <a href="#">Section 8.5.2.3</a> ) 0b ... Page H is not write locked 1b ... Page H is write locked

Table 16. NFC\_MIRROR\_CTL byte (NFC Mirror Control)

Bit number							
0	1	2	3	4	5	6	7
NFC_MIRROR_SEL			NFC_MIRROR_BYTE		RFU		

Table 17. NFC\_MIRROR\_CTL byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
NFC_MIRROR_SEL	3	000b	Defines the functionality for UID and Counter mirroring 000b ... NFC mirror is disabled 001b ... UID mirror is enabled 010b ... UID + Counter mirror is enabled
NFC_MIRROR_BYTE	2	00b	Defines the byte within the block defined in NFC_MIRROR_BLK where the NFC mirror shall start.

Table 18. NFC\_MIRROR\_BLK byte

Bit number							
0	1	2	3	4	5	6	7
NFC_MIRROR_BLK							RFU

Table 19. NFC\_MIRROR\_BLK byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
NFC_MIRROR_BLK	7	00h	Defines the first block within the user memory where the NFC mirror shall start.

Table 20. OTP\_LOCK0 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_CID_LOCK	OTP_LP_LOCK	OTP_PWD_R_LOCK	OTP_PWD_W_LOCK	RFU			

Table 21. OTP\_LOCK0 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_CID_LOCK	1	0h	Defines the write access of the CID bytes in configuration memory block 19: 0b ... CID bytes are not write locked 1b ... CID bytes are locked <b>Note:</b> Lock the CID at the end of the initialization of the IC. (Not required if the complete configuration memory is locked with the OTP_CONFIG_LOCK (see <a href="#">Table 26</a> )
OTP_LP_LOCK	1	0h	Defines the write access of the Lock Pointer bytes LP_PNTR and LP_CTR in configuration memory block 21: 0b ... Lock Pointer bytes are not write locked 1b ... Lock Pointer bytes are locked <b>Note:</b> Lock the Lock Pointer at the end of the initialization of the IC.
OTP_R_PWD_LOCK	1	0h	Defines the write access of the Read Password in configuration memory block 42: 0b ... Read Password is not write locked 1b ... Read Password is locked. The Read password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> )
OTP_W_PWD_LOCK	1	0h	Defines the write access of the Write Password in configuration memory block 43: 0b ... Write Password is not write locked 1b ... Write Password is locked. The Write password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> )

Table 22. OTP\_LOCK1 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_PPC_LOCK	OTP_PRIVACY_PWD_LOCK	OTP_DESTROY_PWD_LOCK	OTP_OS_LOCK	RFU			

Table 23. OTP\_LOCK1 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_PPC_LOCK	1	0h	Defines the write access of the Page Protection condition bytes PPC_PNTR and PPC_CTRL in configuration memory block 20: 0b ... Page Protection bytes are not write locked 1b ... Page Protection bytes are locked <b>Note:</b> Lock the Page Protection condition at the end of the initialization of the IC.
OTP_PRIVACY_PWD_LOCK	1	0h	Defines the write access of the Privacy Password in configuration memory block 44: 0b ... Privacy Password is not write locked 1b ... Privacy Password is locked. The Privacy password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> ).
OTP_DESTROY_PWD_LOCK	1	0h	Defines the write access of the Destroy Password in configuration memory block 45: 0b ... Destroy Password is not write locked 1b ... Destroy Password is locked. The Destroy password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> ).
OTP_OS_LOCK	1	0h	Defines the write access of the Originality Signature in configuration memory blocks 0 - 11 as well as the length of the originality signature defined with the OS_CFG_MODE bit: 0b ... Originality Signature is not write locked 1b ... Originality Signature is locked <b>Note:</b> Lock the Originality Signature at the end of the initialization of the IC. (Not required if the complete configuration memory is locked with the OTP_CONFIG_LOCK (see <a href="#">Table 26</a> ).

Table 24. OTP\_LOCK2 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_DSFI D_LOCK	OTP_ LOCKBITS_ LOCK	OTP_AFI_ PWD_EN	OTP_ COUNTER_ PRESET_DIS	RFU			

Table 25. OTP\_LOCK2 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_DSFI D_LOCK	1	0h	Defines the write access of the DSFID byte in configuration memory block 16: 0b ... DSFID byte is not write locked 1b ... DSFID byte is locked. The DSFID byte can also be locked with the LOCK DSFID command (see <a href="#">Section 8.5.2.10</a> ).
OTP_ LOCKBITS_ LOCK	1	0h	Defines if internal block lock bits can be set with the LOCK BLOCK command: 0b ... LOCK BLOCK command is enabled 1b ... LOCK BLOCK command is disabled
OTP_AFI_PWD_ EN	1	0h	Defines if the AFI Password Protection is enabled: 0b ... AFI Password Protection is disabled 1b ... AFI Password Protection is enabled. The AFI password protection can also be enabled with the PASSWORD PROTECT EAS/AFI command (see <a href="#">Section 8.5.3.16</a> ). <b>Note:</b> To avoid unauthorized change of the AFI, lock or password protect the AFI.
OTP_ COUNTER_ PRESET_DIS	1	0h	Defines if the Counter Preset is disabled: 0b ... Counter Preset is enabled 1b ... Counter Preset is disabled <b>Note:</b> If this functionality is not needed, disable the counter preset (recommendation).

Table 26. OTP\_LOCK3 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_EAS_PWD_EN	OTP_EASAFI_PWD_LOCK	OTP_CONFIG_LOCK	OTP_CONFIG_PWD_LOCK	RFU			

Table 27. OTP\_LOCK3 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_EAS_PWD_EN	1	0h	Defines if the EAS Password Protection is enabled: 0b ... EAS Password Protection is disabled 1b ... EAS Password Protection is enabled. The EAS password protection can also be enabled with the PASSWORD PROTECT EAS/AFI command (see <a href="#">Section 8.5.3.16</a> ). <b>Note:</b> To avoid unauthorized change of EAS, lock or password protect the EAS functionality (recommendation).
OTP_EASAFI_PWD_LOCK	1	0h	Defines the write access of the EAS/AFI Password in configuration memory block 46: 0b ... EAS/AFI Password is not write locked 1b ... EAS/AFI Password is locked. The EAS/AFI password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> ).
OTP_CONFIG_LOCK	1	0h	Defines the write access to the configuration memory with the WRITE_CONFIG command: 0b ... Configuration memory access with WRITE_CONFIG command is enabled 1b ... Configuration memory access with WRITE_CONFIG command is disabled. Settings within the configuration memory can still be changed with other commands, depending on the related access conditions <b>Note:</b> If no further changes need to be set with the WRITE_CONFIG command, write lock the configuration memory at the end of the initialization of the IC. If the configuration memory cannot be locked because changes are needed in the application, program and activate the configuration memory password with the OTP_CONFIG_PWD_EN (see <a href="#">Table 28</a> ).
OTP_CONFIG_PWD_LOCK	1	0h	Defines the write access of the Config Password in configuration memory block 41: 0b ... CONFIG Password is not write locked 1b ... CONFIG Password is locked. The Config password can also be locked with the LOCK PASSWORD command (see <a href="#">Section 8.5.3.4</a> ).

Table 28. OTP\_LOCK4 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_CONFIG_PWD_EN	RFU	OTP_AFI_LOCK	OTP_EAS_LOCK	RFU			

Table 29. OTP\_LOCK4 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_CONFIG_PWD_EN	1	0h	<p>Defines if the write access with the WRITE CONFIG command is password protected with the CFG_PWD password. Access to the configuration memory always depends on related lock options:</p> <p>0b ... Write access to the configuration memory is possible without password authentication</p> <p>1b ... Write access to the configuration memory is only possible with a valid previous password authentication with the CF_PWD password</p> <p><b>Note:</b> If changes with the WRITE CONFIG command are required in the application, program and activate the configuration memory password with the OTP_CONFIG_PWD_EN after the IC initialization. In case no further changes are required, use WRITE_CONFIG command to lock the write access to the configuration memory with the OTP_CONFIG_LOCK bit. See <a href="#">Table 26</a>.</p>
OTP_AFI_LOCK	1	0h	<p>Defines if the AFI in block 17 is write locked:</p> <p>0b ... AFI is not write locked</p> <p>1b ... AFI is write locked. The AFI can also be locked with the LOCK AFI command (see <a href="#">Section 8.5.2.8</a>)</p> <p><b>Note:</b> To avoid unauthorized change of the AFI, lock or password protect the AFI.</p>
OTP_EAS_LOCK	1	0h	<p>Defines if the current state of the EAS mode and the EAS ID is locked:</p> <p>0b ... EAS mode and EAS_ID are not locked</p> <p>1b ... EAS mode and EAS_ID are locked. EAS mode and EAS_ID can also be locked with the LOCK EAS command (see <a href="#">Section 8.5.3.14</a>).</p> <p><b>Note:</b> To avoid unauthorized change of EAS, password protect the EAS functionality.</p>

Table 30. OTP\_LOCK5 byte

Bit number							
0	1	2	3	4	5	6	7
OTP_PWD64_EN	RFU						

Table 31. OTP\_LOCK5 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OTP_PWD64_EN	1	0h	Defines if the 64-bit password protection is enabled: 0b ... 64 bit password protection is disabled 1b ... 64 bit password protection is enabled. The 64-bit password protection can also be enabled with the 64 BIT PASSWORD PROTECTION command (see <a href="#">Section 8.5.3.5</a> ).



Table 32. PRIVACY\_MODE byte

Bit number							
0	1	2	3	4	5	6	7
PRIVACY_MODE_SEL	RFU						

Table 33. PRIVACY\_MODE byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
PRIVACY_MODE_SEL	1	0h	<p>Defines the Privacy mode (see <a href="#">Section 8.5.3.9</a>):</p> <p>0b ... Privacy mode 1: In this mode, the IC only responds to the GET RANDOM NUMBER and SET PASSWORD commands</p> <p>1b ... Privacy mode 2: All ICs in this mode are responding with the same UID to an INVENTORY command</p> <p><b>Note:</b> To avoid unauthorized changes to the privacy mode, lock or password protect the configuration memory .</p>

Table 34. COUNTER\_CFG0 byte

Bit number							
0	1	2	3	4	5	6	7
COUNTER_MODE	RFU						

Table 35. COUNTER\_CFG0 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
COUNTER_MODE	1	0h	<p>Defines the mode of the counter (see <a href="#">Section 8.2.3.1</a>):</p> <p>0b ... Command-based counter is enabled</p> <p>1b ... NFC Counter is enabled</p> <p><b>Note:</b> Lock or password protect the configuration memory to avoid unauthorized changes to the counter mode.</p>

Table 36. COUNTER\_CFG1 byte

Bit number							
0	1	2	3	4	5	6	7
NFC_RETRY_MODE	RFU						

Table 37. COUNTER\_CFG1 byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
NFC_RETRY_MODE	1	0h	Defines how often the IC retries to increase the NFC Counter (see <a href="#">Section 8.2.3.1</a> ): 0b ... 16 retries with a retry period of 4.8 ms 1b ... 64 retries with a retry period of 9.6 ms

Table 38. OS\_CFG byte

Bit number							
0	1	2	3	4	5	6	7
OS_CFG_MODE	RFU						

Table 39. OS\_CFG byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
OS_CFG_MODE	1	0h	Defines the length of the originality signature (see <a href="#">Section 8.2.2</a> ): 0b ... 32 byte originality signature (configuration memory blocks 0-7) 1b ... 48 byte originality signature (configuration memory blocks 0-11)

Table 40. STATUS\_PRIVACY byte

Bit number							
0	1	2	3	4	5	6	7
STATUS_PRIVACY_ACTIVE	RFU						

Table 41. PRIVACY\_STATUS byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
STATUS_PRIVACY_ACTIVE	1	0h	Provides the information if the Privacy is enabled or disabled: 0b ... Privacy mode is not active 1b ... Privacy mode is active

Table 42. STATUS\_EAS byte

Bit number							
0	1	2	3	4	5	6	7
STATUS_EAS_ACTIVE	RFU						

Table 43. STATUS\_EAS byte configuration parameter descriptions

Field	Bit	Values at Delivery	Description
STATUS_EAS_ACTIVE	1	0h	Provides the information if the EAS functionality is set or reset: 0b ... EAS functionality is reset 1b ... EAS functionality is set

### 8.2.3.1 Counter feature

The ICODE 3 supports a 24-bit counter feature that is implemented in block 75 of the user memory.

The COUNTER\_MODE bit in the configuration memory is used to set the mode of the counter mode:

- Command-based counter (see to [Section 8.2.3.1.1](#)) or
- NFC counter (see [Section 8.2.3.1.2](#))

#### 8.2.3.1.1 Command-based counter

If the 24-bit counter is configured as a command-based counter:

- Use the WRITE SINGLE BLOCK command to increase and preset the counter.
- Use OTP\_COUNTER\_PRESET\_DIS bit in the configuration memory to disable the option to preset the counter.COUNTER\_MODE bit in the configuration memory.

Refer to [Section 8.5.3.24 "24-bit counter"](#).

8.2.3.1.2 NFC counter

If the 24-bit counter is configured as an NFC counter, at each start of the IC, the label IC automatically increases the 24-bit counter value. In the NFC counter mode, the startup time of the reader device must comply with the NFC Forum Tag 5 Type specification.

Once the NFC counter has reached the maximum value of FF FF FF hex, the NFC counter value does not change anymore.

The NFC counter is enabled or disabled with the COUNTER\_MODE bit in the configuration memory bit. See [Table 34](#) in [Section 8.2.3](#).

To read the NFC counter value, use either a read command to block 75 or the NFC counter mirror feature.

If the counter is configured as an NFC counter, the counter is incremented every time the tag is tapped by an NFC device or other read point. Due to response time constraints in ISO/IEC 15693 [ref.\[1\]](#), the increment is done at startup and not at the first read access to the user memory. A circuit that preserves its state over HF resets prevents further increments of the NFC counter until a read of the user memory is executed.

To ensure that the NFC counter is also incremented in situations where the tag slowly enters the HF field (typically in long range systems), the label IC retries to increment the counter at startup multiple times. To optimally adapt to the application, two options are available with the NFC\_RETRY\_MODE bit:

Table 44. NFC\_RETRY\_MODE request format

NFC_RETRY_MODE	Number of retries	Time between retries	Total retry period	Recommended usage
0	16	4.8 ms	> 77 ms	default (for most applications)
1	64	9.6 ms	> 614 ms	Applications where the label enters the field very slow

If all the retries fail, the counter returns 0x00 00 00 to indicate that the counter had not been increased.

8.2.3.2 NFC ASCII mirror feature

The NFC ASCII mirror feature of ICODE 3 enables the label IC to virtually mirror:

- The 8-byte UID (see [Section 8.2.1](#)), and
- The 3-byte counter value (see [Section 8.2.3.1](#)).

The feature depends on NFC mirror settings into the physical memory of the IC in ASCII code. On a READ or FAST READ command to the assigned user memory blocks, the label IC responds with the virtual memory content of the UID and/or counter value in ASCII code depending on the settings in the NFC\_MIRROR\_CTR byte (see [Table 16](#)).

The required length of the reserved physical memory for the mirror functions and the order for the ASCII mirrors are specified in [Table 45](#).

**Note:** The number of bytes (see [Table 45](#)) of the enabled ASCII mirrors must not exceed the boundary of the user memory. Use only valid values for NFC\_MIRROR\_BLK and NFC\_MIRROR\_BYTE. If the ASCII mirror exceeds the user memory area, the ASCII mirroring stops at the end of the user memory.

Table 45. Required memory space for ASCII mirror

ASCII mirror and order	Required number of bytes in the physical memory
UID mirror	16 bytes
UID + NFC counter mirror	23 bytes (16 bytes for UID + 1 byte separation + 6 bytes counter value)

The fields are mirrored into the defined user memory area in the following order:

- UID: MSB first
- Counter: MSB First

The NFC\_MIRROR\_BLK and NFC\_MIRROR\_BYTE values in the configuration define the position within the user memory where the mirroring of the ASCII mirror starts.

The NFC\_MIRROR\_BLK value defines the block where the ASCII mirror starts and the NFC\_MIRROR\_BYTE value defines the starting byte within the defined block.

The ASCII mirrors are enabled with the NFC\_MIRROR\_SEL bits (see [Table 17](#).)

If more than one ASCII mirror is enabled, the ASCII mirrors are separated automatically with an "x" character (78h ASCII code).

### 8.2.4 Configuration of delivered ICs

NXP ICODE 3 ICs are delivered with the following configuration:

- The unique identifier is unique and read-only.
- The write access allows changes to user blocks, AFI, DSFID, EAS, and passwords (password protection disabled).
- All password bytes are 00h for the Read and Write protection password, for the EAS/AFI password, and for the Config password.
- All password bytes are 0Fh for the privacy mode and label Destroy passwords.
- User data memory is **not** password protected.
- Password protected privacy Mode is disabled.
- EAS and AFI password protection is disabled.
- The status of EAS mode is not defined.
- AFI is supported and not defined
- DSFID is supported and not defined.
- The user data memory is not defined.
- NFC mirror feature is disabled.

**Note:**

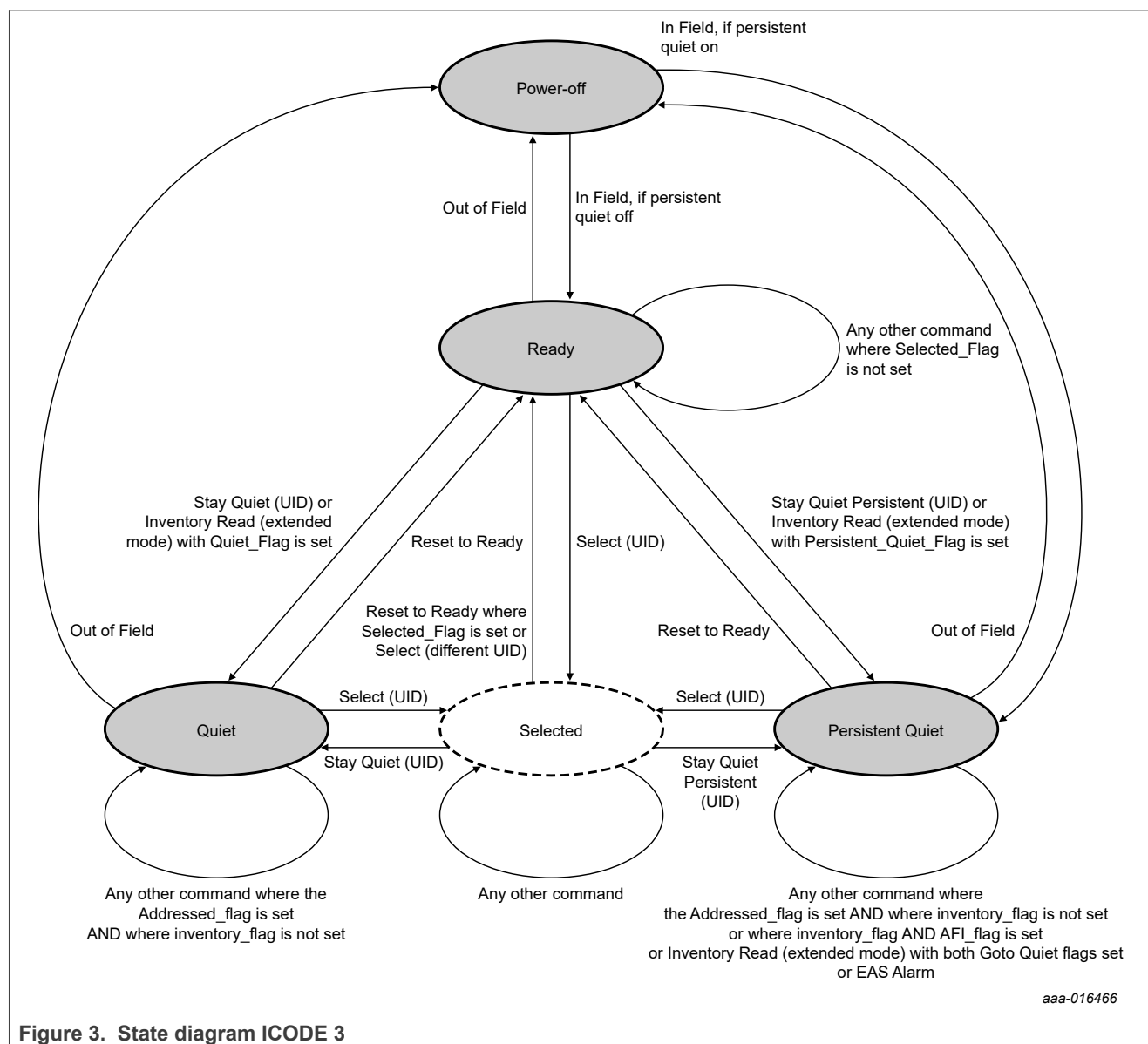
1. *As the EAS mode is undefined at delivery, enable or disable EAS mode according to your application requirements during the test or initialization phase.*
2. *If password protection is not required and depending on the targeted application, write random passwords during the label initialization (recommendation).*

### 8.3 Communication principle

For the detailed description of the protocol and timing refer to ISO/IEC 15693-2 [ref.\[2\]](#) (modulation, bit-coding, framing), and ISO/IEC 15693-3 [ref.\[3\]](#) (anti-collision, timing, protocol).

## 8.4 State diagram

Figure 3 illustrates the different states of the ICODE 3.



**Note:** You can set the ICODE 3 IC in the Quiet state and Persistent Quiet state at the same time. In this case, the behavior is the same as for the Quiet state only until the IC enters the Power-off state. If the persistent time has not been exceeded, the IC enters to the Persistent Quiet mode at the next power-on.

## 8.5 Supported commands

### 8.5.1 Mandatory commands

#### 8.5.1.1 INVENTORY

The command is as defined in ISO/IEC 15693-3 [ref.\[3\]](#).

Exception: If the Privacy or Destroy mode is enabled, the label does not respond.

#### 8.5.1.2 STAY QUIET

The command is as defined in ISO/IEC 15693-3 [ref.\[3\]](#).

### 8.5.2 Optional commands

#### 8.5.2.1 READ SINGLE BLOCK

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

If the related page of the addressed block is protected with the Read-Password, and if the password has not been transmitted first with the SET PASSWORD command, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

**Note:** Block 75 of the user memory is used for the 24-bit counter feature and must be used differently. Refer to [Section 8.5.3.24 "24-bit counter"](#).

#### 8.5.2.2 WRITE SINGLE BLOCK

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

If the addressed block is part of a write protected page, or if the block is protected with the Read Password only (see [Section 8.5.3.6 "PROTECT PAGE"](#)), and the password has not been transmitted first with the SET PASSWORD command, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

**Note:** Block 75 of the user memory is used for the 24-bit counter feature and must be used differently. Refer to [Section 8.5.3.24 "24-bit counter"](#).



### 8.5.2.3 LOCK BLOCK

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

If the addressed block is part of a write protected page, or if the block is protected with the read password only (see [Section 8.5.3.6 "PROTECT PAGE"](#)), and the password has not been transmitted first with the SET PASSWORD command, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

**Note:** Block 75 of the user memory is used for the 24-bit counter feature and must be used differently. Refer to [Section 8.5.3.24 "24-bit counter"](#).

The ICODE 3 supports the option to lock larger sections of the user memory with the settings in the configuration memory block 21 (see [Table 9](#)). The Lock Pointer LP\_PNTR defines the block from which the user memory is divided into two pages (Page L and Page H). The lock conditions for the two pages L and H are defined with the settings defined in the LP\_CTR byte (see [Table 14](#)).

### 8.5.2.4 READ MULTIPLE BLOCKS

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

If one of the addressed blocks is part of a page protected with the Read-Password, and if the password has not been transmitted first with the SET PASSWORD command, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

**Note:** Block 75 of the user memory is used for the 24-bit counter feature and must be used differently. Refer to [Section 8.5.3.24 "24-bit counter"](#).

### 8.5.2.5 SELECT

As defined in ISO/IEC 15693-3.

### 8.5.2.6 RESET TO READY

As defined in ISO/IEC 15693-3.

**Note:** RESET TO READY also resets the label IC from the persistent quiet state to the READY state. Refer to [Section 8.5.3.10 "INVENTORY READ"](#) and [Section 8.5.3.19 "STAY QUIET PERSISTENT"](#).

### 8.5.2.7 WRITE AFI

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

**Note:** The command can be password protected. Refer to [Section 8.5.3.16 "PASSWORD PROTECT EAS/AFI"](#).

**Note:** You can use also the WRITE CONFIG command to block 17 of the configuration memory to write the AFI. Refer to [Table 9](#).

### 8.5.2.8 LOCK AFI

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

**Note:**

1. The command can be password protected. Refer to [Section 8.5.3.16 "PASSWORD PROTECT EAS/AFI"](#).
2. To lock the AFI, you can set the OTP\_AFI\_LOCK bit to 1 with the WRITE CONFIG command to block 30 of the configuration memory. Refer to [Table 9](#).
3. To avoid unauthorized change of the AFI, lock or password protect the AFI.

### 8.5.2.9 WRITE DSFID

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

The DSFID can also be written by a WRITE CONFIG command to block 16 of the configuration memory containing the DSFID. Refer to [Table 9](#).

Also, the WRITE CONFIG command to block 16 of the configuration memory can write DSFID. Refer to [Table 9](#).

### 8.5.2.10 LOCK DSFID

As defined in ISO/IEC 15693-3.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

Also, setting the OTP\_DSFID\_LOCK bit to 1 with the WRITE CONFIG command to block 28 of the configuration memory can lock the DSFID. See [Table 9](#) and [Table 24](#).

### 8.5.2.11 GET SYSTEM INFORMATION

As defined in ISO/IEC 15693-3.

The TAG type of the ICODE 3 IC is "01h".

### 8.5.2.12 GET MULTIPLE BLOCK SECURITY STATUS

As defined in ISO/IEC 15693-3.

### 8.5.2.13 FAST READ MULTIPLE BLOCK

As defined in ISO/IEC 15693-3 (2019).

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

The supported data rates are as defined in ISO/IEC 15693-3 (2019):

- High data rate (26.48 kbits/s)
- X2 (52.97 kbits/s)
- X4 (105.94 kbits/s)
- X8 (211.88 kbits/s)

If one of the addressed blocks is part of a page protected with the Read-Password, and if the password has not been transmitted first with the SET PASSWORD command, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

**Note:** Block 75 of the user memory is used for the 24-bit counter feature and must be used differently. Refer to [Section 8.5.3.24 "24-bit counter"](#).

8.5.3 Custom commands

The manufacturer code of NXP Semiconductors is defined in ISO/IEC 7816-6A1 [ref.\[4\]](#). The code has the value "04h".

For the structure of custom commands, refer to ISO/IEC 15693-3 [ref.\[3\]](#).

Unless otherwise specified, all the address modes are supported.

8.5.3.1 GET RANDOM NUMBER

Command code = B2h

The GET RANDOM NUMBER command is required to receive a random number from the label IC. The passwords transmitted with the SET PASSWORD, ENABLE PRIVACY and DESTROY commands must be calculated with the password and the random number (see [Section 8.5.3.2 "SET PASSWORD"](#)).

The different passwords are addressed with the password identifier.

Table 46. GET RANDOM NUMBER request format

SOF	Flags	GET RANDOM NUMBER	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 47. GET RANDOM NUMBER response when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 48. GET RANDOM NUMBER response format when Error\_flag NOT set

SOF	Flags	Random number	CRC16	EOF
-	8 bits	16 bits	16 bits	-

### 8.5.3.2 SET PASSWORD

#### Command code = B3h

The SET PASSWORD command enables the different passwords to be transmitted to the label to access the different protected functions of the commands. If the label is powered, the SET PASSWORD command must be executed only once for the related passwords.

**Note:** The SET PASSWORD command can be executed only in Addressed or Selected mode except for the Privacy password. If the Privacy password is transmitted, the timing of the SET PASSWORD command is write alike. See [Section 8.5.3.9 "ENABLE PRIVACY"](#).

The XOR password must be calculated with the password and with twice the received random number from the last GET RANDOM NUMBER command:

$\text{XOR\_Password}[31:0] = \text{Password}[31:0] \text{ XOR } \{\text{Random\_Number}[15:0], \text{Random\_Number}[15:0]\}.$

The different passwords are addressed with the password identifier.

Table 49. SET PASSWORD request format

SOF	Flags	SET PASSWORD	IC Mfg code	UID	Password identifier	XOR password	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	32 bits	16 bits	-

Table 50. Password Identifier

Password identifier	Password
01h	Read
02h	Write
04h	Privacy
08h	Destroy
10h	EAS/AFI
20h	Configuration memory

Table 51. SET PASSWORD response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 52. SET PASSWORD response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

**Note:** If the IC receives an invalid password, it does not execute commands like WRITE PASSWORD or LOCK PASSWORD until a Power-On Reset (POR) or RF reset.

### 8.5.3.3 WRITE PASSWORD

#### Command code = B4h

The WRITE PASSWORD command is used to write a new password into the related memory:

- If the related old password has already been transmitted with a SET PASSWORD command, and
- If the addressed password is not locked (see [Section 8.5.3.4 "LOCK PASSWORD"](#)).

**Note:** The WRITE PASSWORD command can only be executed in addressed or selected mode. The new password takes effect immediately. That is, the new password must be transmitted with the SET PASSWORD command to access protected blocks/pages.

The different passwords are addressed with the password identifier.

The timing of the command is write alike.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

Also, the WRITE CONFIG command to the related blocks 41-46 in the configuration memory can be used to write the passwords. See [Table 9](#).

**Note:** Use diversified passwords. For the privacy passwords, use diversified passwords per application. Only use the configuration password in trusted environments.

Table 53. WRITE PASSWORD request format

SOF	Flags	WRITE PASSWORD	IC Mfg code	UID	Password identifier	Password	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	32 bits	16 bits	-

Table 54. Password Identifier

Password identifier	Password
01h	Read
02h	Write
04h	Privacy
08h	Destroy
10h	EAS/AFI
20h	Configuration memory

Table 55. WRITE PASSWORD response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 56. WRITE PASSWORD response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

### 8.5.3.4 LOCK PASSWORD

#### Command code = B5h

The LOCK PASSWORD command is used to lock the addressed password if the related password has been transmitted with a SET PASSWORD command already. A locked password cannot be changed.

The different passwords are addressed with the password identifier.

The timing of the command is write alike.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

**Note:** Setting the related OTP bit to 1 with the WRITE CONFIG command to blocks 26, 27 and 29 of the configuration memory also locks the passwords. See [Table 9](#) and [Table 24](#).

Table 57. LOCK PASSWORD request format

SOF	Flags	LOCK PASSWORD	IC Mfg code	UID	Password identifier	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	16 bits	-

Table 58. Password identifier

Password identifier	Password
01h	Read
02h	Write
04h	Privacy
08h	Destroy
10h	EAS/AFI
20h	Configuration memory

Table 59. LOCK PASSWORD response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 60. LOCK PASSWORD response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

8.5.3.5 64-BIT PASSWORD PROTECTION

Command code = BBh

The 64-bit PASSWORD PROTECTION command instructs the Label IC that both the Read and Write passwords are required to get access to password-protected blocks (pages). This mode can be enabled if the Read and Write passwords have been transmitted first with a SET PASSWORD command.

If the 64-bit password protection is enabled, both passwords are required for read and write access to protected blocks (pages).

Once the 64-bit password protection is enabled, a change back to 32-bit password protection (read and write password) is not possible.

Note:

- 1. The retransmission of the passwords is not required after the execution of the 64-bit PASSWORD PROTECTION command.
- 2. The 64-bit PASSWORD PROTECTION does not include the 16-bit counter block.

The timing of the command is write alike.

Also, setting the OTP\_PWD64\_EN to 1 with a WRITE CONFIG command to block 31 in the configuration memory can enable the 64-bit PASSWORD PROTECTION. See [Table 9](#) and [Table 30](#).

Table 61. 64-BIT PASSWORD PROTECTION request format

SOF	Flags	64 BIT PASSWORD PROTECTION	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 62. 64-BIT PASSWORD PROTECTION response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 63. 64-BIT PASSWORD PROTECTION response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-



### 8.5.3.6 PROTECT PAGE

#### Command code = B6h

The PROTECT PAGE command defines the protection pointer address of the user memory. The user memory is divided into two arbitrarily sized pages. The command is used to define the access conditions for the two pages.

The protection pointer address defines the base address of the higher user memory segment Page H. All block addresses smaller than the protection pointer address are in the user memory segment Page L.

[Table 64](#) shows an example of the user memory segmentation with the protection pointer address 20 (0x14).

Table 64. Memory organization

Block	Byte 0	Byte 1	Byte 2	Byte 3	Description
0					Page L
1					
2					
:	:	:	:	:	
18					
19					
20					Page H
21					
:	:	:	:	:	
77					
78					
79	C0	C1	0x00	Protection	Counter

**Note:** If the protection pointer address is set to block 0, the entire user memory (block 0 to block 74) is defined as Page H.

The access conditions and the protection pointer address can be changed under the following circumstances:

- The related passwords (Read and Write password) have been transmitted first with the SET PASSWORD command.
- The page protection condition is not locked (see [Section 8.5.3.7 "LOCK PAGE PROTECTION CONDITION"](#)).

The timing of the command is write alike.

Table 65. POTECT PAGE request format

SOF	Flags	PROTECT PAGE	IC Mfg code	UID	Protection pointer address	Extended protection status	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	8 bits	16 bits	-

**Remark:** The label IC only accepts protection pointer address values from 0x00 (block 0) to 0x4A (block 74). Block 75 (containing the 24-bit counter) is excluded from the standard user memory password protection scheme.

**Note:** You can use the WRITE CONFIG command to block 20 in the configuration memory to write the protection pointer address PPC\_PNTR. See [Table 9](#).

Table 66. Extended Protection status byte

Bit	Name	Value	Description
b1 (LSB)	RL	0	Page L is not read protected
		1	Page L is read protected
b2	WL	0	Page L is not write protected
		1	Page L is write protected
b3	-	0	RFU
b4	-	0	RFU
b5	RH	0	Page H is not read protected
		1	Page H is read protected
b6	WH	0	Page H is not write protected
		1	Page H is write protected
b7	-	0	RFU
b8 (MSB)	-	0	RFU

Also, the protection status bits can be set in the configuration memory with a WRITE CONFIG command to configure the related bits in the PPC\_CTRL byte ([Table 11](#)).

Table 67. Protection status bits definition

Wx	Rx	32-bit password protection	64-bit password protection
0	0	Public	Public
0	1	Read and Write protected by the Read password	Read and Write protected by the Read plus Write password
1	0	Write protected by the Write password	Write protected by the Read plus Write password
1	1	Read protected by the Read password <b>and</b> Write protected by the Read and Write password	Read and Write protected by the Read plus Write password

Table 68. POTECTION PAGE response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 69. POTECTION PAGE response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

The information about the stored settings of the protection pointer address and access conditions can be read with the GET NXP SYSTEM INFORMATION command (refer to [Section 8.5.3.18 "GET NXP SYSTEM INFORMATION"](#)).

8.5.3.7 LOCK PAGE PROTECTION CONDITION

Command code = B7h

The LOCK PAGE PROTECTION CONDITION command locks the protection pointer address and the status of the page protection conditions. The Read and Write passwords must be transmitted first with the SET PASSWORD command.

The timing of the command is write alike.

Also, setting the OTP\_PPC\_LOCK bit to 1 with a WRITE CONFIG command to block 27 of the configuration memory can lock the protection pointer address and the status of the page protection conditions. See [Table 9](#) and [Table 22](#).

**Note:** Lock the Page Protection condition at the end of the initialization of the IC (recommendation).

Table 70. LOCK PAGE PROTECTION CONDITION request format

SOF	Flags	LOCK PAGE PROTECTION CONDITION	IC Mfg code	UID	Protection pointer address	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	16 bits	-

**Note:** If the transmitted protection pointer address does not match the stored address, the label responds according to the error handling (see [Section 8.6 "Error handling"](#)).

Table 71. LOCK PAGE PROTECTION CONDITION response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 72. LOCK PAGE PROTECTION CONDITION response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

8.5.3.8 DESTROY

Command code = B9h

The DESTROY command is used to destroy ICODE 3 Label IC. The Destroy password must be correct. This command is irreversible and the ICODE 3 never responds to any command again.

The DESTROY command can only be executed in addressed or selected mode.

The XOR password must be calculated with the password and twice the received random number from the last GET RANDOM NUMBER command:

$$\text{XOR\_Password}[31:0] = \text{Password}[31:0] \text{ XOR } \{ \text{Random\_Number}[15:0], \text{Random\_Number}[15:0] \}.$$

The timing of the command is write alike.

Table 73. DESTROY request format

SOF	Flags	DESTROY	IC Mfg code	UID	XOR password	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	32 bits	16 bits	-

Table 74. DESTROY response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 75. DESTROY response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

### 8.5.3.9 ENABLE PRIVACY

#### Command code = BAh

The ENABLE PRIVACY command sets the ICODE 3 Label IC to Privacy mode, if the Privacy password is correct. In the Privacy mode, the ICODE 3 is not traceable by its UID nor by the data stored in the user memory.

The two privacy modes of ICODE 3 are defined with the PRIVACY\_MODE\_SEL bit (see [Table 32](#)) in the configuration memory, and with the WRITE CONFIG command.

- Privacy mode 1  
In privacy mode 1, the ICODE 3 does not respond to any command except GET RANDOM NUMBER and SET PASSWORD.
- Privacy mode 2  
In privacy mode 2, the ICODE 3 responds to an Inventory command with the UID 0x E0 04 00 00 00 00 00 00. The IC reference in Get System Information command response is changed to 0x00. ICODE 3 labels in privacy mode 2 only support the following commands:
  - INVENTORY
  - SELECT
  - STAY QUIET
  - GET SYSTEM INFORMATION
  - PICK RANDOM ID
  - SET PASSWORD
  - GET RANDOM NUMBER
  - STAY QUIET PERSISTANT
  - RESET TO READY
  - READ SINGLE BLOCK
  - READ MULTIPLE BLOCKS

Read access to data from the user memory depends on the read password protection settings.

With the command PICK\_RANDOM\_ID ([Section 8.5.3.23 "PICK RANDOM ID"](#)), the ICODE 3 generates a random ID to respond to the inventory commands and to support the anti-collision feature. The random ID includes the CID to identify the group-key to disable the privacy mode.

The XOR password must be calculated with the password and twice the received random number from the last GET RANDOM NUMBER command:

$\text{XOR\_Password}[31:0] = \text{Password}[31:0] \text{ XOR } \{\text{Random\_Number}[15:0], \text{Random\_Number}[15:0]\}.$

To get out of the Privacy status, the valid Privacy password must be transmitted to the IC with the SET PASSWORD command.

The timing of the command is write alike.

**Table 76. ENABLE PRIVACY request format**

SOF	Flags	ENABLE PRIVACY	IC Mfg code	UID	XOR password	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	32 bits	16 bits	-

**Table 77. ENABLE PRIVACY response format when Error\_flag set**

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 78. ENABLE PRIVACY response format when Error\_ flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

8.5.3.10 INVENTORY READ

Command code = A0h

When receiving the INVENTORY READ request, the ICODE 3 IC performs the anticollision sequence, but instead of the UID and the DSFID in the response, there are additional options.

The INVENTORY READ command generates two modes, which are defined by the most significant bit of the mask length byte as follows:

- Standard mode (MSB mask length byte equal 0)  
The standard mode of the INVENTORY READ command is fully backward-compatible to the ICODE SLI and ICODE SLIX ([Standard mode](#)).
- Extended mode (MSB mask length byte equal 1)  
The extended mode supports additional features to optimize the inventory procedure for different requirements ([Extended Mode](#)).

Standard mode

If MSB mask length byte equals 0, the INVENTORY READ command is used in the standard mode.

If the Inventory\_flag is set to 1 and an error is detected, the ICODE 3 IC remains silent.

If the Option flag is set to logic 0, n blocks of data are retransmitted. If the Option flag is set to 1, n blocks of data and the part of the UID, which is not part of the mask are retransmitted.

The request contains:

- Flags
- INVENTORY READ command code
- IC manufacturer code
- AFI (if AFI flag is set)
- Mask length (most significant bit equal 0)
- Mask value (if mask length > 0)
- First block number to be read
- Number of blocks to be read
- CRC 16

Table 79. INVENTORY READ request format

SOF	Flags	INVENTORY READ	IC Mfg code	AFI	Mask length	Mask value	First block number	Number of blocks	CRC16	EOF
-	8 bits	8 bits	8 bits	8 bits optional	8 bits	0 to 64 bits	8 bits	8 bits	16 bits	-

If the Inventory\_flag is set to logic 1, only the tags in the READY or SELECTED state respond (the same behavior as in the INVENTORY command). The meaning of flags 5 to 8 is in accordance with table 5 in ISO/IEC 15693-3 [ref.\[3\]](#).

The INVENTORY READ command can be transmitted also in the addressed or selected mode ([Addressed and selected mode](#)).

The number of blocks in the request is one less than the number of blocks that the ICODE 3 IC returns in the response.

If the Option flag in the request is set to logic 0 the response contains:

**Table 80. INVENTORY READ response format: Option flag logic 0**

SOF	Flags	Data	CRC16	EOF
-	8 bits	Block length	16 bits	-
		Repeated as needed		

The ICODE 3 IC reads the requested block(s) and sends back their value in the response. The mechanism and timing of the INVENTORY READ command are similar to the INVENTORY command described in clause 8 of ISO/IEC 15693-3.

If the Option flag in the request is set to logic 1, the response contains:

**Table 81. INVENTORY READ response format: Option flag logic 1**

SOF	Flags	Rest of UID, which is not part of the mask and slot number	Data	CRC16	EOF
-	8 bits	0 to 64 bit	Block length	16 bits	-
		Multiple of 8 bits	Repeated as needed		

The ICODE 3 IC reads the requested block(s) and sends back their value in the response. The bytes of the UID, which are not parts of the mask, and the slot number in case of 16 slots, are returned. Instead of padding with zeros up to the next byte boundary, the corresponding bits of the UID are returned. The mechanism and timing of the INVENTORY READ command are similar to the INVENTORY command described in clause 8 of ISO/IEC 15693-3.

**Note:** The number of bits of the retransmitted UID are calculated as:

- 16 slots: 60 bits (bit 64 to bit 4) - mask length rounded up to the next byte boundary
- 1 slot: 64 bits - mask length rounded up to the next byte boundary

If the sum of the first block number and number of blocks exceeds the total number available user blocks, the number of transmitted blocks is less than the requested number of blocks. The last returned block is the highest available user block, followed by the 16-bit CRC and the EOF.

**Example:** mask length = 30 bits

Returned: bit 64 to bit 4 (30 bits) = 30 gives 4 bytes

**Table 82. Example: mask length = 30**

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	UID
mask value including padding with zeros				-				transmitted by interrogator
				returned value				transmitted by ICODE 3 IC



## Extended Mode

If the most significant bit of the Mask Length byte is equal to 1, the response format is defined by the extended option byte.

The request contains:

- Flags
- Inventory Read command code
- IC Manufacturer code
- AFI (if the AFI flag is set)
- Mask length (most significant bit equal 1)
- Extended Options
- Mask value (if mask length > 0)
- First Block Number, if specified in extended options byte
- Number of Blocks, if specified in extended options byte
- CRC 16

**Table 83. Inventory Read (extended mode) request format**

SOF	Flags	Inventory Read	IC Mfr. code	AFI	Mask Length	ext. Options	opt. CID	Mask Value	First block number	Number of blocks	CRC 16	EOF
	8 bits	8 bits	8 bits	8 bits optional	8 bits MSB = 1	8 bits	16 bits	0 to 64 bits	8 bits optional	8 bits optional	8 bits	

If the Inventory\_flag is set to logic 1, only tags in the READY or SELECTED state respond (similar behavior as INVENTORY command). The meaning of flags 5 to 8 is in accordance with table 5 in ISO/IEC 15693-3 [ref.\[3\]](#).

The INVENTORY READ command can be transmitted in the addressed or selected mode also ( [Addressed and selected mode](#) ).

**Table 84. Extended options**

Bit number	Bit name	Value	Feature
1 (LSB)	EAS_MODE	0	Label responds independent from the EAS status
		1	Only labels will respond which have the EAS enabled
2	UID_MODE	0	UID will be transmitted as in regular mode (truncated reply depending on least significant 7 bits value of mask length and the mask value)
		1	Complete UID will be transmitted (independent from mask length)
3	CID_COMPARE	0	No CID is transmitted in the command
		1	16 bit CID will be transmitted in the command and only labels with the same CID will respond
4	CID_RESPONSE	0	CID will NOT be transmitted in the response from the label
		1	CID will be transmitted in the response from the label
5	SKIP_DATA	0	Tag will add the user memory blocks in the response as requested with first block number byte and number of blocks byte in the command
		1	No user memory data are requested from the tag, first block number byte and number of blocks byte shall not be transmitted in the command
6	QUIET	0	refer to <a href="#">Table 85</a>

Table 84. Extended options...continued

Bit number	Bit name	Value	Feature
7	PERSISTENT QUIET	0	refer to <a href="#">Table 85</a>
8 (MSB)	-	0	RFU

Table 85. QUIET and PERSISTANT QUIET bit in Extended options

QUIET bit [6]	PERSISTENT QUIET bit [7]	Feature
0	0	remain in current state
1	0	go to Quiet State after response (refer to <a href="#">Section 8.5.1.2 "STAY QUIET"</a> )
0	1	go to Persistent Quiet State after Response (refer to <a href="#">Section 8.5.3.19 "STAY QUIET PERSISTENT"</a> )
1	1	only tags in the PERSISTENT QUIET state will respond to the command

If the option flag in the request is set to 1, the response contains the truncated or the complete UID depending on the extended option flag 2.

If the option flag in the request is set to 0, the UID is not part of the response.

Table 86. Inventory Read (extended mode) response format: Option flag logic 1

SOF	Flags	Option CID	Optional truncated UID OR complete UID	Optional data	CRC16	EOF
-	8 bits	16 bits	0 to 64 bit	Block length	16 bits	-
			Multiple of 8 bits	Repeated as needed		

The mechanism and timing of the INVENTORY READ command are similar to the INVENTORY command described in clause 8 of ISO/IEC 15693-3.

If the UID is requested in the truncated format, the retransmitted UID can be calculated as follows:

16 slots: 64 - 4 - mask length rounded up to the next byte boundary

1 slot: 64 - mask length rounded up to the next byte boundary

**Example:** mask length = 30

Returned: 64 - 4 - 30 = 30 gives 4 bytes

Table 87. Example

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	UID
mask value incl. padding with zeros								transmitted by Interrogator
				returned value				transmitted by ICODE 3 IC

## Addressed and selected mode

The INVENTORY READ command can be transmitted also in the addressed or selected mode. In this case, the Inventory\_flag is set to 0, and the meaning of flags 5 to 8 is in accordance with table 4 in ISO/IEC 15693-3 [ref. \[3\]](#).

In the addressed or selected mode, the INVENTORY READ command behaves like a READ or READ MULTIPLE BLOCK command.

In the addressed mode, it is recommended to address the label IC with a mask length of 64 and to transmit the complete UID in the mask value field.

In the selected mode (label IC has been selected with a valid SELECT command before), it is recommended to address the label IC with a mask length of 0 (and do not transmit the mask value field).

**Note:** *If the INVENTORY READ command is used in the addressed mode or in the selected mode, the AFI is not transmitted. The label IC only responds in the first-time slot.*

### 8.5.3.11 FAST INVENTORY READ

#### Command code = A1h

When receiving the FAST INVENTORY READ command, the ICODE 3 IC response is the same as with the INVENTORY READ command. Exceptions are:

- The data rate from the ICODE 3 IC to the interrogator is twice the data rate defined in ISO/IEC 15693-3. The rate depends on the Datarate\_flag 53 kbit (high data rate) or 13 kbit (low data rate).
- The data rate from the interrogator to the ICODE 3 IC, and the time between the rising edge of the EOF from the interrogator to the ICODE 3 IC remain unchanged. That is, same as defined in ISO/IEC 15693-3.
- In the direction of ICODE 3 IC to the interrogator, only the single subcarrier mode is supported.

### 8.5.3.12 SET EAS

#### Command code = A2h

The SET EAS command enables the EAS mode, if the EAS mode is not locked. If the EAS mode is password protected, the EAS password must be transmitted first with the SET PASSWORD command.

The timing of the command is write alike.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

Table 88. SET EAS request format

SOF	Flags	SET EAS	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 89. SET EAS response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 90. SET EAS response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

8.5.3.13 RESET EAS

Command code = A3h

If the EAS mode is not locked, the RESET EAS command disables the EAS mode. If the EAS mode is password protected, the EAS password must be transmitted first with the SET PASSWORD command.

The timing of the command is write alike.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

Table 91. RESET EAS request format

SOF	Flags	RESET EAS	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 92. RESET EAS response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 93. RESET EAS response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

8.5.3.14 LOCK EAS

Command code = A4h

The LOCK EAS command locks the current state of the EAS mode and the EAS ID. If the EAS mode is password protected, the EAS password must be transmitted first with the SET PASSWORD command.

The timing of the command is write alike.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is supported.

Setting the OTP\_EAS\_LOCK bit to 1 with a WRITE CONFIG command to block 30 of the configuration memory also locks the EAS mode and the EAS ID. See [Table 9](#) and [Table 28](#).

Table 94. LOCK EAS request format

SOF	Flags	LOCK EAS	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 95. LOCK EAS response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 96. LOCK EAS response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

## 8.5.3.15 EAS ALARM

## Command code = A5h

The EAS ALARM command can be used in the following configurations:

- Option flag is set to 0:  
EAS ID mask length and the EAS ID value are not transmitted.  
If the EAS mode is enabled, the EAS response is returned from the ICODE 3 IC.
- Option flag is set to 1:  
Within the command, the EAS ID mask length must be transmitted to identify how many bits of the following EAS ID value are valid (multiple of 8 bits). If the EAS Mode is set, the ICODE 3 ICs responds. The response includes the EAS sequence corresponding to the data in the EAS ID configuration (selective EAS).  
If the EAS ID mask length is set to 0, the ICODE 3 IC responds with its EAS ID.

Table 97. EAS ALARM Request format

SOF	Flags	EAS ALARM	IC Mfg code	UID	EAS ID mask length	EAS ID value	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits optional	0, 8 or 16 bits optional	16 bits	-

If an error is detected, the ICODE 3 IC remains silent.

Option flag is set to logic 0 or Option flag is set to logic 1 and the EAS ID mask length is not equal to 0:

Table 98. EAS ALARM Response format (Option flag logic 0)

SOF	Flags	EAS sequence	CRC16	EOF
-	8 bits	256 bits	16 bits	-

EAS sequence (starting with the LSB, which is transmitted first; read from left to right):

11110100	11001101	01000110	00001110	10101011	11100101	00001001	11111110
00010111	10001101	00000001	00011100	01001011	10000001	10010010	01101110
01000001	01011011	01011001	01100001	11110110	11110101	11010001	00001101
10001111	00111001	10001011	01001000	10100101	01001110	11101100	11110111

Option flag is set to logic 1 and the EAS ID mask length is equal to 0:

Table 99. EAS ALARM Response format (Option flag logic 1)

SOF	Flags	EAS ID value	CRC16	EOF
-	8 bits	16 bits	16 bits	-

If the EAS mode is disabled, the ICODE 3 IC remains silent. See RESET EAS command in [Section 8.5.3.13 "RESET EAS"](#).

**Note:** Labels in the QUIET state do not respond to an EAS ALARM command except if the addressed flag is set. Labels in the PERSISTANT QUIET mode respond even if the addressed flag is not set (refer to [Section 8.4 "State diagram"](#)).

### 8.5.3.16 PASSWORD PROTECT EAS/AFI

#### Command code = A6h

The PASSWORD PROTECT EAS/AFI command enables the password protection for EAS and/or AFI. The EAS/AFI password must be transmitted first with the SET PASSWORD command.

Option flag set to logic 0: EAS is password protected.

Option flag set to logic 1: AFI is password protected.

Both password protections (AFI and EAS) can be enabled separately.

**Note:** Independent of the Option flag, the write-alike command is executed like a write command with Option flag 0. That is, option flag not set.

Once the EAS/AFI password protection is enabled, it is not possible to change back to unprotected EAS and/or AFI.

The timing of the command is write alike (as write command with Option flag 0).

The password protection for EAS and/or AFI can be enabled also with a WRITE CONFIG command to set the following bits set to 1 in the configuration memory:

OTP\_EAS\_PWD\_EN bit in block 29: EAS is password protected.

OTP\_AFI\_PWD\_EN bit in block 28: AFI is password protected.

**Note:** To avoid the unauthorized change of the EAS and AFI settings, password protect the EAS and AFI functionality.

Table 100. PASSWORD PROTECT EAS/AFI request format

SOF	Flags	PASSWORD PROTECT EAS/AFI	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 101. PASSWORD PROTECT EAS/AFI response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 102. PASSWORD PROTECT EAS/AFI response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-



8.5.3.17 WRITE EAS ID

Command code = A7h

The command WRITE EAS ID stores a new EAS Identifier in the corresponding configuration memory. If EAS is password protected (for Set and Reset EAS) the EAS password must be transmitted first with the SET PASSWORD command.

The timing of the command is write alike.

Option 1 (Option flag set) is supported.

Option 0 (Option flag not set) is supported.

Also, a WRITE CONFIG command to block 18 of the configuration memory can write the EAS ID. See [Table 9](#).

Table 103. WRITE EAS ID request format

SOF	Flags	WRITE EAS ID	IC Mfg code	UID	EAS ID value	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	16 bits	-

Table 104. WRITE EAS ID response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 105. WRITE EAS ID response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

## 8.5.3.18 GET NXP SYSTEM INFORMATION

## Command code = ABh

The command GET NXP SYSTEM INFORMATION command is used to get information about the IC access conditions and supported features.

Table 106. GET NXP SYSTEM INFORMATION request format

SOF	Flags	Get NXP System Info	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 107. GET NXP SYSTEM INFORMATION response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 108. GET NXP SYSTEM INFORMATION response format when Error\_flag NOT set

SOF	Flags	PP pointer	PP conditions	Lock bits	Feature flags	CRC16	EOF
-	8 bits	8 bits	8 bits	8 bits	32 bits	16 bits	-

On a valid received command, the label IC responds with the following information:

- Actual protection pointer address (PP pointer)
- Actual protection conditions for the password protection (PP conditions)
- Actual lock bits settings (Lock bits)
- Supported commands and features (Feature flags)

The bit values value in [Table 111](#) indicate if the related feature is enabled or disabled:

- 0: feature disabled
- 1: feature enabled

Table 109. PP conditions bits

Bit	Name	Feature
1 (LSB)	RL	Page L read password protection status
2	WL	Page L write password protection status
3-4	-	RFU
5	RH	Page H read password protection status
6	WH	Page H write password protection status
7-8 (MSB)	-	RFU

Table 110. Lock bits

Bit	Name	Feature
1 (LSB)	AFI	AFI lock bit
2	EAS	EAS lock bit
3	DSFID	DSFID lock bit
4	PPL	Password protection pointer address and access conditions lock bit
5-8 (MSB)	-	RFU

Table 111. Feature flags bits

Bit	Name	Feature
1 (LSB)	UM PP	User memory password protection supported (refer to <a href="#">Section 8.5.3.6 "PROTECT PAGE"</a> )
2	COUNTER	Counter feature supported
3	EAS ID	EAS ID supported by EAS ALARM command (refer to <a href="#">Section 8.5.3.17 "WRITE EAS ID"</a> )
4	EAS PP	EAS password protection supported (refer to <a href="#">Section 8.5.3.16 "PASSWORD PROTECT EAS/AFI"</a> )
5	AFI PP	AFI password protection supported (refer to <a href="#">Section 8.5.3.16 "PASSWORD PROTECT EAS/AFI"</a> )
6	INVENTORY READ EXT	Extended mode supported by INVENTORY READ command (refer to <a href="#">Section 8.5.3.10 "INVENTORY READ"</a> )
7	EAS IR	EAS selection supported by extended mode in INVENTORY READ command (refer to <a href="#">Section 8.5.3.10 "INVENTORY READ"</a> )
8	CID	Customer ID (CID) supported
9	ORIGINALITY SIG	READ SIGNATURE command supported (refer to <a href="#">Section 8.5.3.20 "READ SIGNATURE"</a> )
10	TAGTAMPER	TagTamper feature supported
11	P QUIET	STAY QUIET PERSISTENT command supported (refer to <a href="#">Section 8.5.3.19</a> )
12	NFC MIRROR	NFC mirror feature supported (refer to <a href="#">Section 8.2.3.2 "NFC ASCII mirror feature"</a> )
13	PRIVACY	ENABLE PRIVACY command supported (refer to <a href="#">Section 8.5.3.9 "ENABLE PRIVACY"</a> )
14	DESTROY	DESTROY command supported (refer to <a href="#">Section 8.5.3.8 "DESTROY"</a> )
15	WRITE CID	Programming of the Customer ID (CID) supported
16	HIGH DATA RATES	High data rates are supported (refer to <a href="#">Section 8.5.2.13 "FAST READ MULTIPLE BLOCK"</a> )
17 - 31	-	RFU
32 (MSB)	EXT	Additional 32 bits feature flags are transmitted

8.5.3.19 STAY QUIET PERSISTENT

Command code = BCh

When receiving the STAY QUIET PERSISTENT command, the label IC enters the persistent quiet state and does not send back a response.

**Note:** The STAY QUIET PERSISTENT command has the same behavior as the mandatory STAY QUIET command. The only difference is at reset (power off). If the power off time exceeds the persistent time, the label IC switches to the ready state,.

When in PERSISTENT QUIET state:

- The label IC does not process any request where the Inventory\_flag is set, except:
  - If the AFI\_flag is set, or
  - If the QUIET and PERSTENT QUIET flags in the extended mode of the (Fast) Inventory command are both set.
- The label IC processes any EAS ALARM request, and any addressed or selected request.

The label IC exits the persistent quiet state when:

- Reset (power off) exceeds the persistent time.
- Receiving a SELECT request. The IC goes to the Selected state.
- Receiving a RESET TO READY request. The IC goes to the Ready state.

The STAY QUIET PERSISTENT command must be executed in addressed mode (Select\_flag is set to 0 and Address\_flag is set to 1).

Table 112. STAY PERSISTENT QUIET request format

SOF	Flags	STAY QUIET PER SISTENT	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	

8.5.3.20 READ SIGNATURE

Command code = BDh

The READ SIGNATURE command returns an IC specific 32-byte or 48-byte ECC signature, to verify NXP Semiconductors as the silicon vendor. The signature length is defined with the OS\_CFG\_MODE bit ([Table 38](#)).

The originality signature can also be read with a READ CONFIG command to

- blocks 0-7 if the 32 byte signature length is enabled or
- block 0-11 if the 48 byte signature length is enabled.

Table 113. READ SIGNATURE request format

SOF	Flags	READ SIG NATURE	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	

Table 114. READ SIGNATURE response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 115. READ SIGNATURE response format when Error\_flag NOT set

SOF	Flags	Originality Signature	CRC16	EOF
-	8 bits	256 or 384 bits	16 bits	-

Details on how to check the signature value will be provided in the application note *ICODE 3 Originality Signature Validation*. The document describes how to verify the originality of ICODE 3.

### 8.5.3.21 READ CONFIG

#### Command code = C0h

The READ CONFIG command reads the requested number of blocks (n-1). The reading starts with the first block defined by the block address of the configuration memory.

Access to the configuration blocks depends on the status and definition of the related block within the configuration memory (see [Section 8.2.3 "Configuration memory"](#)).

If one of the requested configuration blocks is not accessible due to the actual status, the ICODE 3 responds with Error\_flag set (see [Table 117](#)).

Within one command execution, a READ\_CONFIG command can read one or multiple blocks of the following areas of the configuration memory:

- Block 0 to block 127
- Passwords cannot be read and are masked with 0x00 in the response
  - Block 41: CFG\_PWD (Configuration password)
  - Block 42: READ\_PWD (Read password)
  - Block 43: WRITE\_PWD (Write password)
  - Block 44: PRIVACY\_PWD (Privacy password)
  - Block 45: DESTROY\_PWD (Destroy password)
  - Block 46: EASAFI\_PWD (EAS/AFI password)

Block 47 (TT\_OPEN\_MSG) can only be read if it is not write-locked with the OTP\_TT\_OPEN\_MSG\_LOCK bit (see [Table 30](#)) otherwise it is locked with all bytes 0x00.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) is not supported.

**Table 116. READ CONFIG request format**

SOF	Flags	READ_CONFIG	IC Mfg code	UID	Block Address	Number of Blocks	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	8 bits	16 bits	-

**Table 117. READ CONFIG response format when Error\_flag set**

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

**Table 118. READ\_CONFIG response format when Error\_flag NOT set**

SOF	Flags	Data	CRC16	EOF
-	8 bits	32 bits repeated as needed	16 bits	-

8.5.3.22 WRITE CONFIG

Command code = C1h

The WRITE\_CONFIG command writes the 4-byte data to the requested block address of the configuration memory.

Access to the configuration blocks depends on the status and definition of the related block within the configuration memory (see [Section 8.2.3 "Configuration memory"](#)).

If the configuration memory is password protected, write access is only possible after the valid authentication with the SET PASSWORD command with the Configuration password.

If the requested configuration block is not write accessible due to the actual status, the ICODE 3 responds with Error\_flag set ([Table 120](#)).

If the Configuration memory is write-locked with the OTP\_CFG\_LOCK bit (see [Table 27](#)), ICODE 3 responds with Error\_flag set.

The timing of the command is write alike.

Option 1 (Option flag set) is supported.

Option 0 (Option flag not set) is supported.

Table 119. WRITE\_CONFIG request format

SOF	Flags	WRITE_CONFIG	IC Mfg code	UID	Block Address	Data	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	8 bits	32 bits	16 bits	-

Table 120. WRITE\_CONFIG response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 121. WRITE\_CONFIG response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

## 8.5.3.23 PICK RANDOM ID

**Command code = C2h**

The PICK RANDOM ID instructs an ICODE 3 in privacy mode to generate a random ID. After a valid PICK RANDOM ID command, the ICODE 3 responds with the random ID to INVENTORY commands or to Get System Information command, until a power-on reset.

Option 0 (Option flag not set) is supported.

Option 1 (Option flag set) not is supported.

Table 122. PICK\_RANDOM\_ID request format

SOF	Flags	PICK_RANDOM_ID	IC Mfg code	UID	CRC16	EOF
-	8 bits	8 bits	8 bits	64 bits optional	16 bits	-

Table 123. PICK\_RANDOM\_ID response format when Error\_flag set

SOF	Flags	Error code	CRC16	EOF
-	8 bits	8 bits	16 bits	-

Table 124. PICK\_RANDOM\_ID response format when Error\_flag NOT set

SOF	Flags	CRC16	EOF
-	8 bits	16 bits	-

After a successful PICK\_RANDOM\_ID, the ICODE 3 responds to an INVENTORY command with a random ID defined in [Table 125](#).

Table 125. Random ID

MSB							LSB
64:57	56:49	48:41	40:33	32:25	24:17	16:1	
"E0"	"04"	"00"	"00"	CID_1	CID_0	16-bit random ID	
RID 7	RID 6	RID 5	RID 4	RID 3	RID 2	RID 1	RID 0



### 8.5.3.24 24-bit counter

Block 75 of the user memory contains the 24-bit counter. The block can be accessed with the standard READ and WRITE commands but special data considerations are required.

The standard password protection mechanisms for the user memory are not valid for block 75.

The 24-bit counter (block 75) can be:

- Read.
- Increased by one with the option of read password protection.
- Preset to the initial start value with the write password protection.

The counter can be read with any read command including block 75. The 4-byte data from block 75 provide the following information:

Table 126. COUNTER BLOCK data structure

Byte	Name	Value	Description
0	C0	0x00 - 0xFF	LSB of the counter value
1	C1	0x00 - 0xFF	—
2	C2	0x00 - 0xFF	MSB of the counter value
3	PROT	0x00	Incrementing of the counter value is not password protected
		0x01	Incrementing of the counter value is protect with the read password

The counter can be preset to a start value with a WRITE SINGLE BLOCK command to block 75. As the counter preset is password protected with the write password, a SET PASSWORD command with the write password is required before executing the Preset (refer to [Section 8.5.3.2 "SET PASSWORD"](#)).

The PROT byte (data byte 3) value defines whether the password protection to increment the counter is enabled or disabled. If the password protection is enabled, the read password is required to increment the counter value.

The data for the WRITE SINGLE BLOCK command to preset the counter are defined in [Table 127](#).

**Note:** The Preset counter value of 0x0001 is not possible. A WRITE SINGLE BLOCK command with 0x0001 value only increments the counter.

Table 127. Preset counter data structure

Byte	Name	Value	Description
0	C0	0x00, 0x02 - 0xFF	LSB of the counter value
1	C1	0x00 - 0xFF	—
2	C2	0x00 - 0xFF	MSB of the counter value
3	PROT	0x00	Disable the password protection to increment the counter
		0x01	Enable the password protection to increment the counter with read password

To increment the counter by one with a WRITE SINGLE BLOCK command to block 75. If the password protection to increment the counter is enabled, the read password needs to be transmitted to the label IC with the SET PASSWORD command before (refer to [Section 8.5.3.2 "SET PASSWORD"](#)).

The data for the WRITE SINGLE BLOCK command to increment the counter are defined in [Table 127](#).

**Note:** The counter can be incremented only with the C0, C1 and C2 values defined in [Table 128](#). If the write password has been transmitted earlier with a SET PASSWORD command, the other values preset the counter or lead to an error message.

Table 128. Increment counter by 1 data structure

Byte	Name	Value	Description
0	C0	0x01	LSB of the counter value
1	C1	0x00	—
2	C2	0x00	MSB of the counter value
3	PROT	0x00	PROT value of 0x00 only accepts incrementing by 1

To increment the counter by up to 255 (0xFF), issue a WRITE SINGLE BLOCK command to block 75. If the password protection to increment the counter is enabled, the read password must be transmitted to the label IC with the SET PASSWORD command first (refer to [Section 8.5.3.2 "SET PASSWORD"](#)).

The data for the WRITE SINGLE BLOCK command to increment the counter are defined in [Table 127](#).

**Note:** The counter can be incremented only with the C0, C1 and C2 values defined in [Table 128](#). If the write password has been transmitted earlier with a SET PASSWORD command, the other values preset the counter or lead to an error message.

Table 129. Increment counter by up to 0xFF data structure

Byte	Name	Value	Description
0	C0	0x01 - 0xFF	LSB of the counter value
1	C1	0x00	
2	C2	0x00	MSB of the counter value
3	PROT	0x80	PROT value of 0x80 allows incrementing from 0x01 up to 0xFF

## 8.6 Error handling

### 8.6.1 Transmission errors

In compliance with ISO/IEC 15693[ref.\[1\]](#), the label IC does not respond if a transmission error is detected. Examples of transmission errors are CRC, bit coding, bit count, or wrong framing. The device waits for the next correct received command.

### 8.6.2 Commands not supported or options

If the received command or option is not supported, the behavior of the label IC depends on the addressing mechanism.

#### 8.6.2.1 Non-addressed Mode

The label IC remains silent.

#### 8.6.2.2 Addressed or Selected Mode

In addressed mode or in selected mode, the label IC responds with the error code "0Fh" (error with no information given or error code is not supported).

If the Inventory flag or the Protocol Extension flag is set, the label IC does not respond if the command or option is not supported.

### 8.6.3 Parameter out of range

#### 8.6.3.1 Read commands

If the sum of the first block number and the number of blocks exceeds the total number of available user blocks, the number of transmitted blocks is less than the requested number of blocks. The last returned block is the highest available user block, followed by the 16-bit CRC and the EOF.

#### 8.6.3.2 Write and lock commands

If the address of a block to be written does not exist, or if a block to be written is locked, the behavior of the label IC depends on the addressing mechanism.

#### Non-addressed Mode

- The label IC remains silent and aborts the command without writing anything.

#### Addressed Mode or Selected Mode

- The addressed or selected label IC responds with the error code "0Fh" (error with no information given or error code is not supported).

## 8.7 Data integrity

The following mechanisms ensure the reliable transmission of data between the interrogator and label IC:

- 16-bit CRC per block
- Bit count checking
- Bit coding to distinguish between logic 1, logic 0, and no information
- Channel monitoring (protocol sequence and bit stream analysis)

## 8.8 RF interface

The definition of the RF interface is according to the standard ISO/IEC 15693-2 [ref.\[2\]](#) and ISO/IEC 15693-3 [ref.\[3\]](#).


## 9 Limiting values

Table 130. Limiting values (Wafer)[1][2]  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	+125	°C
P <sub>tot</sub>	total power dissipation			-	125	mW
T <sub>j</sub>	junction temperature			-40 [3]	+105	°C
I <sub>i(max)</sub>	maximum input current	LA to LB; peak	[4]	-	±60	mA
I <sub>I</sub>	input current	LA to LB; RMS		-	30	mA
V <sub>ESD</sub>	electrostatic discharge voltage	human body model (HBM) [5]	[6]	-	±2	kV

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the operating conditions and electrical characteristics sections of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Under extreme conditions (negative temperatures and tag stays a long time at the maximum operating range) the use of HF Resets is recommended.
4. The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I<sub>I</sub>).
5. According to ANSI/ESDA/JEDEC JS-001.
6. For ESD measurement, the IC was mounted in a SO28 package.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10 Characteristics

### 10.1 Wafer memory characteristics

Table 131. Wafer EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{ret}}$	retention time	$T_{\text{amb}} \leq 55\text{ }^{\circ}\text{C}$	50	-	-	year
$N_{\text{endu(W)}}$	write endurance	—	100000	-	-	cycle

### 10.2 Interface characteristics

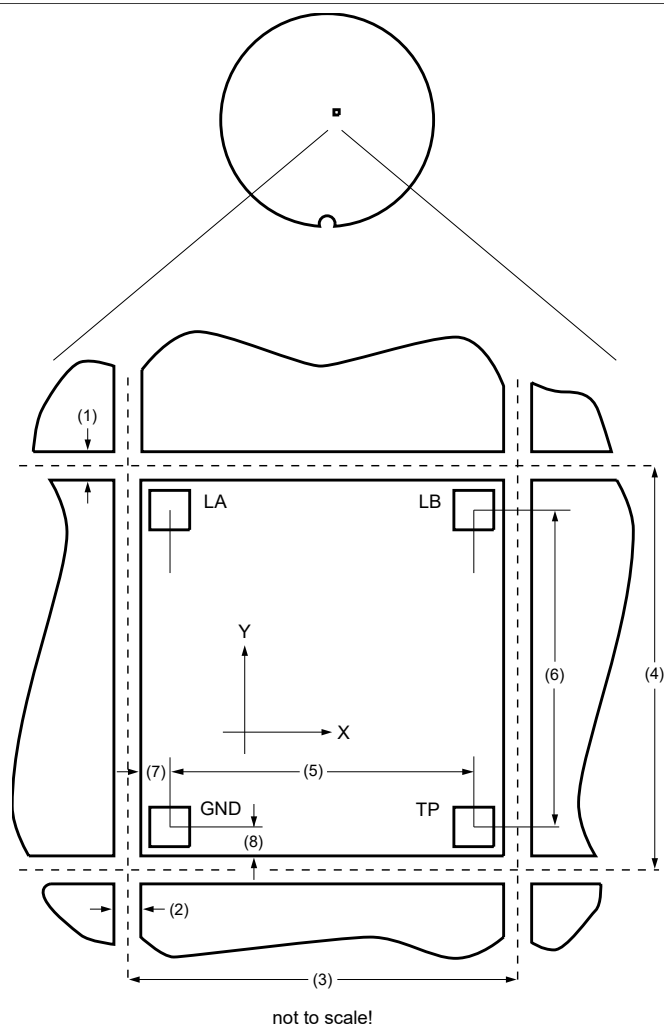
Table 132. Interface characteristics

Typical ratings are not guaranteed. The values listed are at room temperature.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_i$	input frequency		[1]	13.553	13.56	13.567	MHz
$V_{i(\text{RMS})\text{min}}$	minimum RMS input voltage	operating read/ write		1.1	-	1.3	V
$P_{i(\text{min})}$	minimum input power	operating	[2]	-	40	-	$\mu\text{W}$
$C_i$	input capacitance	between LA and LB	[3]	92.1	97	101.9	pF
$t_{\text{persist}}$	persistent time	$T_{\text{amb}} \leq 55\text{ }^{\circ}\text{C}$	[4]	2	-	-	s

1. Bandwidth limitation ( $\pm 7\text{ kHz}$ ) according to ISM band regulations.
2. Including losses in the resonant capacitor and rectifier.
3. Measured with an HP4285A LCR meter at 13.56 MHz and 1.1 V RMS.
4. The maximum persistent time strongly depends on the ambient temperature.

## 11 Bare die outline



- (1) X-scribe line width: 35  $\mu\text{m}$
- (2) Y-scribe line width: 35  $\mu\text{m}$
- (3) Chip step, X-length: 675  $\mu\text{m}$
- (4) Chip step, Y-length: 695  $\mu\text{m}$
- (5) Bump to bump distance X (LA - LB): 530  $\mu\text{m}$
- (6) Bump to bump distance Y (LB - GND): 550  $\mu\text{m}$
- (7) Distance GND bump to nitride edge X: 55  $\mu\text{m}$
- (8) Distance GND bump to nitride edge Y: 55  $\mu\text{m}$
- Bump size LA and LB (X  $\times$  Y): 80  $\mu\text{m}$   $\times$  80  $\mu\text{m}$
- Bump size TP and GND (X  $\times$  Y): 80  $\mu\text{m}$   $\times$  80  $\mu\text{m}$

**Figure 4. Wafer SL2S3103 bare die layout**

## 12 Abbreviations

Table 133. Abbreviations

Acronym	Description
AFI	Application Family Identifier
CRC	Cyclic Redundancy Check
DSFID	Data Storage Format Identifier
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
EOF	End Of Frame
IC	Integrated Circuit
LCR	Inductance, Capacitance, Resistance
LSB	Least Significant Byte/Bit
MSB	Most Significant Byte/Bit
RF	Radio Frequency
SOF	Start Of Frame
UID	Unique IDentifier



## 13 References

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- [1] ISO Standard – ISO/IEC 15693 - Identification cards - Contactless integrated circuit cards - Vicinity cards.
- [2] ISO Standard – ISO/IEC 15693-2 -Identification cards - Contactless integrated circuit cards - Vicinity cards - Part 2: Air interface and initialization.
- [3] ISO Standard – ISO/IEC 15693-3 -Identification cards - Contactless integrated circuit cards - Vicinity cards - Part 3: Anticollision and transmission protocol.
- [4] ISO Standard – ISO/IEC 7816-6 - Identification cards - Integrated circuit cards - Part 6: Inter-industry data elements for interchange.
- [5] Specification – General specification for 12" wafer on UV-tape with electronic fail die marking  
Delivery type description – BU-ID document number: 1862\*\*<sup>2</sup>.
- [6] Publication – Certicom Research. SEC 2  
Recommended Elliptic Curve Domain Parameters, version 2.0, January 2010.
- [7] Application note – AN11600 - ICODE Originality Signature Verification

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2 \*\* ... document version number

## 14 Revision history

Table 134. Revision history

Document ID	Release date	Description
SL2S3103 v.3.2	4 June 2025	Product data sheet <ul style="list-style-type: none"><li>Editorial changes</li><li>Correction from "NFC counter value" to "counter value" in <a href="#">Section 8.2.3.2 "NFC ASCII mirror feature"</a> and <a href="#">Table 17 "NFC_MIRROR_CTR byte configuration parameter descriptions"</a></li></ul>
SL2S3103 v.3.1	29 May 2024	Product data sheet <ul style="list-style-type: none"><li><a href="#">Section 2.1 "ICODE 3 RF interface (ISO/IEC 15693)"</a>: updated</li><li><a href="#">Section 10.2 "Interface characteristics"</a>: updated</li></ul>
SL2S3103 v.3.0	28 May 2024	Product data sheet <ul style="list-style-type: none"><li>Initial version</li></ul>

Legal information

Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.  
[2] The term 'short data sheet' is explained in section "Definitions".  
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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