S32N5

S32N55 and S32N53 Data Sheet

Rev. 4.0 — 27 April 2026 Product data sheet

- This document provides electrical specifications for S32N55 and S32N53.
- For functional characteristics and the programming model, see S32N5 Reference Manual

1 Introduction

1.1 Applications

S32N5 is the initial chip in NXP's next generation 5 nm S32N family of products. S32N5 is a real-time processor for multi-SoC domain control applications, and supports multi-application ASIL D control through advanced real-time processing, hardware isolation, and virtualization.

2 Block diagram

The following figure represents the block diagram for this device.

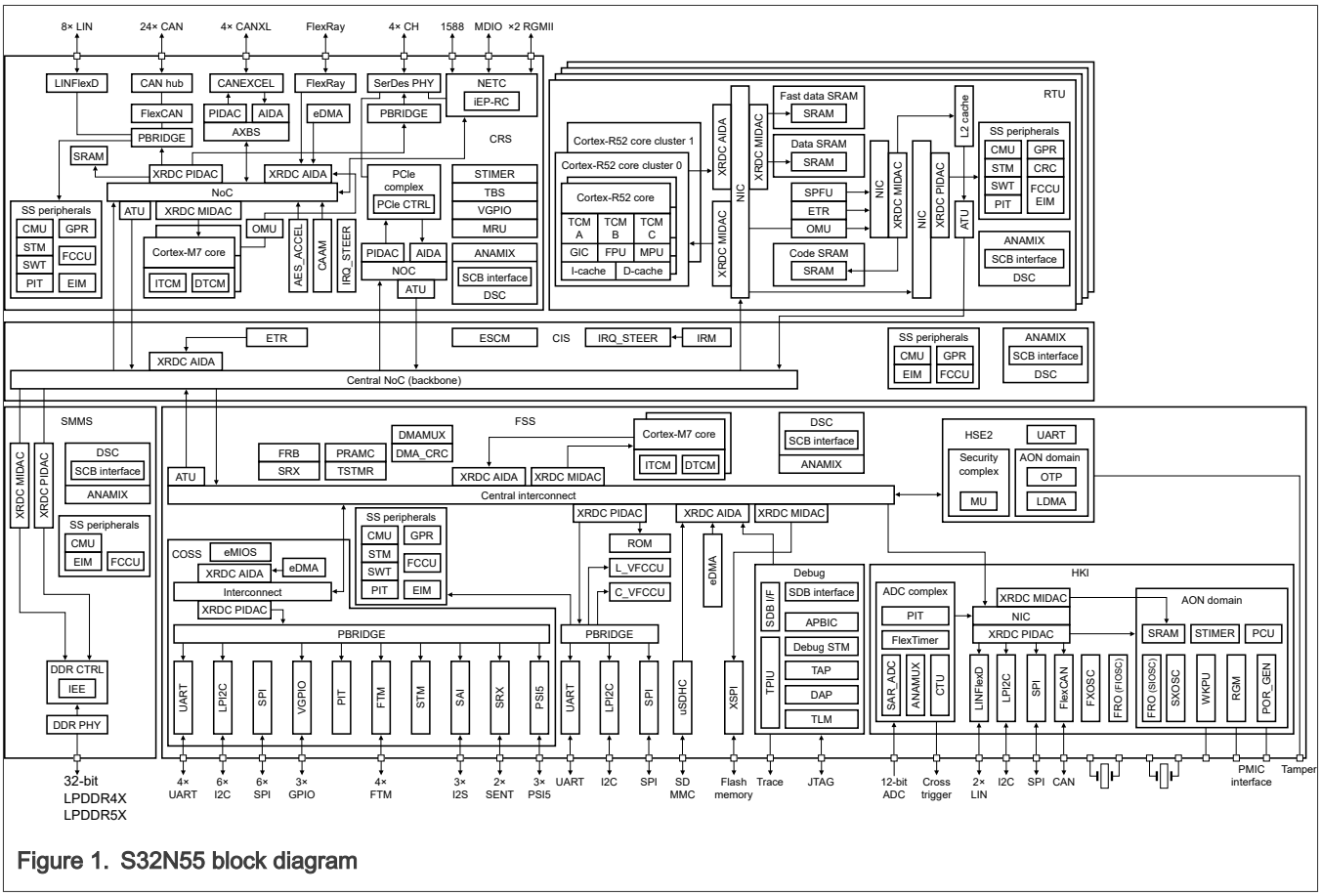

Figure 1. S32N55 block diagram

3 Features

Table 1. Feature summary

Feature	Specifications	
	S32N55	S32N53
Compute and bus modules		
Functional safety	Configurable up to ASIL D	
CPUs: real-time	16× Arm Cortex-R52 cores arranged in 8× pairs of two cores Core pairs can be run in lock or split modes	12× Arm Cortex-R52 cores arranged in 6× pairs of two cores Core pairs can be run in lock or split modes[1]
System manager CPU	1× Arm Cortex-M7 core in lockstep	
CRS	1× Arm Cortex-M7 core in lockstep	
Interrupt controller (RT cores)	Lockstep GIC interrupt controller per RT core cluster	
DMA	eDMA (supporting lockstep) 10× eDMAs (7× COS, 1× FSS-main, 2× CRS)	
DMAMUX	Included	
Debug: run control	Included	
Debug: trace via TPIU and PCIe	Included	
Memory modules		
Internal RAM	48 MB	36 MB[1]
NVM interface	Two channels: • Both supporting serial, quad, and octal NOR • One of them supporting eMMC 5.1 and SDHC NAND	
Real-time memory expansion	1× 32-bit LPDDR4X and LPDDR5X	
Security modules		
Hardware Security Engine, version 2	HSE2	
Crypto accelerators	1× CAAM (high performance, feature rich, look-aside crypto accelerator) 1× AES_ACCEL (for functionally safe SecOC CMAC generation and checking)	
Resource isolation	XRDC	
DDR controller IEE	Inline PRINCE crypto engine on real-time memory expansion interface	
Artificial intelligence and machine learning (AI/ML)		
AI/ML	Arm Cortex Neon (76 Gflops)	Arm Cortex Neon (57 Gflops)
Communication interface modules		
CAN-FD	24	

Table continues on the next page...

Table 1. Feature summary...*continued*

Feature	Specifications	
	S32N55	S32N53
CAN XL	4	
FlexRay (2-channel)	1	
LINFlexD	10	
UART	6 (4× COS, 1× FSS main, 1× HSE2)	
SPI	8	
SENT	2	
PSI5	2	
PSI5 serial	2	
I2C	7 (+1 for PMIC)	
I2S (2-channel)	3	
Ethernet acceleration	2-port TSN switch 5 Gbps line-rate	
Ethernet MACs	2× 2.5G, 1G, 100M, 10M Ethernet MAC	
Ethernet I/F	MII, RMII, RGMII, SGMII, and SGMII 2.5G	
PCIe	1× PCIe, up to Gen4 (X1/X2)	
SerDes	Four lanes	
Timers and analog		
FlexTimer	4 × 4 channels 2 × 3 channels	
PIT	Yes	
STM	One per CPU	
SWT	One per CPU	
ADC	1× 12-channel, 12-bit SAR_ADC	
Clocking, power, and reset modules		
FIRC	Included	
SIRC	Included	
FXOSC	Included	
SXOSC	Included	
Low-Power mode	Included	
Application programming interface (API)	Included	
Miscellaneous		

Table continues on the next page...

Table 1. Feature summary...*continued*

Feature	Specifications	
	S32N55	S32N53
Package	19×19mm FC-BGA with minimum ball pitch of 0.65mm	
Temperature range	-40℃ to 105℃ Ta (125℃ Tj)	

[1] RTU3 cores and RAM are not available on S32N53.

4 Ordering Information

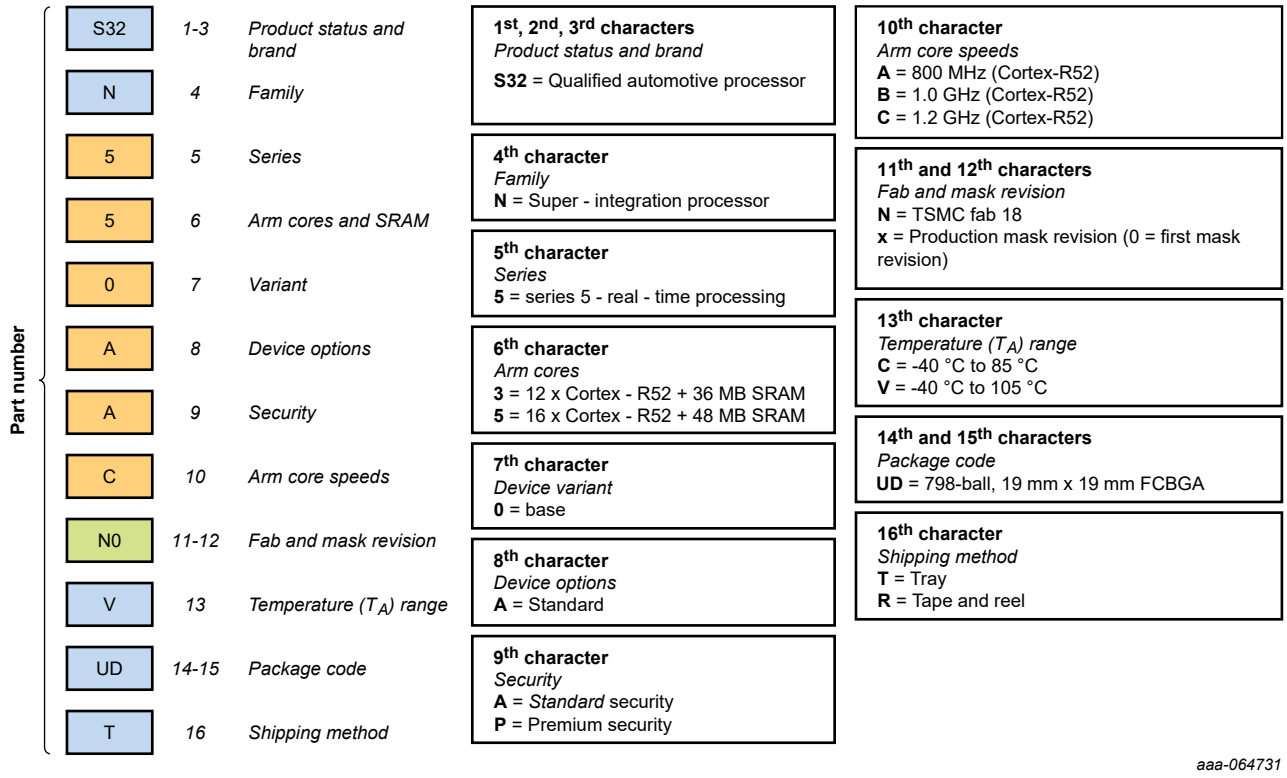

Figure 2. S32N55 ordering information

5 Electrostatic Discharge (ESD) Characteristics

The following table gives the ESD ratings and test conditions for the device.

Table 2. Electrostatic Discharge (ESD) Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
—	ESD Human Body Model (HBM) [1][2][3]	—	—	2000	V	All pins
—	ESD Charged Device Model (CDM) [1][2][4]	—	—	250	V	All pins

[1] All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
[2] Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements."
[3] This parameter is tested in conformity with AEC-Q100-002
[4] This parameter is tested in conformity with AEC-Q100-011.

6 Absolute Maximum Ratings

This table defines the absolute maximum ratings for the device in terms of reliability characteristics. Absolute maximum rating specifications are stress ratings only, and functional operation is not guaranteed under these conditions. Functional operating conditions are given in the Operating Conditions section of this document.

Note: *All specifications associated with VIN are measured at the SoC pin.*

Table 3. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD2H_1PX_IO_SMMS0	VDD2H IO supply for DDR PHY - Main [1]	-0.3	—	1.32	V	—
VDDA_1PX_VDD2H_SMMS0	Analog Supply for DDR PHY PLL - Main [1]	-0.3	—	1.32	V	—
VDDQ_0PX_IO_SMMS0	VDDQ IO supply for DDR PHY - Main [1]	-0.3	—	0.72	V	—
VDD_IO_SD0	SerDes0 IO supply -Main [1][2]	-0.3	—	0.93	V	—
VDD_IO_1P5_SD0	SerDes supply (int regulation) - Main [1][3]	-0.3	—	1.8	V	—
VDDA_1P5_FSS_FOSC	FOSC voltage supply [1][3]	-0.3	—	1.8	V	—
VDDA_1P5_ANAx	Common Analog Supply for Anamixes - Main [1][3]	-0.3	—	1.8	V	—
VDD_IO_1P8_AO	IO Supply - Always-On [1][4]	-0.3	—	2.16	V	—
VDD_1P8_EFUSE	Supply for Fuse Block [1][4]	-0.3	—	2.16	V	—
VDD_IO_1P8_CAN	IO supply - Main for CAN, LIN, FR IO [1][4]	-0.3	—	2.16	V	—
VDD_IO_1P8_ETH	NWS LVCMOS IO supply for Networking SS IO [1][4]	-0.3	—	2.16	V	—
VDD_IO_1P8_MAIN_FSIO	FSS IO supply - Main [1][4]	-0.3	—	2.16	V	—
VDD_IO_1P8_MAIN_MSIO	COS IO supply - Main [1][4]	-0.3	—	2.16	V	—
VDD_RTU	RTU Core Supply - Switchable [1][2]	-0.3	—	0.93	V	—
VREFH_1P5_ADC	ADC Reference High Voltage (VREFH_ADC) [1][3]	-0.3	—	1.8	V	—
VREFL_1P5_ADC	ADC Reference Low Voltage (V REFL_ADC) [1]	-0.3	—	0.3	V	—
VDD	SoC Core Supply - Main [1][2]	-0.3	—	0.93	V	—
VDD_AO	FSS Core Supply - Always On [1][2]	-0.3	—	0.93	V	—
VSS	Ground Supply [1]	-0.3	—	0.3	V	—

Table continues on the next page...

Table 3. Absolute Maximum Ratings*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VEXTAL	FXOSC EXTAL input voltage range [1][3][5]	-0.3	—	1.8	V	—
VXTAL	FXOSC XTAL input voltage range [1][3][5]	-0.3	—	1.8	V	—
VAD_INPUT	ADC input voltage range [1][6][7]	VREFL_1P5_ADC - 0.3	—	VREFH_1P5_ADC + 0.3	V	—
VIN	GPIO input voltage range [1][8]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—
IINJ_D	Maximum DC current injection digital I/O pin [1]	-1	—	1	mA	Unpowered
IINJ_D	Maximum DC current injection digital I/O pin [1]	0	—	0	mA	Powered
IINJ_A	Maximum DC current injection SAR ADC input pin [1][7][9]	-1	—	1	mA	—
TSTG	Storage temperature range [1]	-55	—	150	C	—
TSDR	Maximum solder temperature [1] [10]	—	—	260	C	Pb free
MSL	Moisture Sensitivity Level [1][11]	—	—	3	—	—
V_OS_US_10	Voltage at 10 % of tSIGNAL [12]	-0.7	—	2.31	V	1.8V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below

[1] Absolute maximum ratings are stress ratings only, and functional operation beyond the operating condition maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device. See the operating conditions table for functional specifications.
[2] Allowed 0.825V – 0.93V for 60 seconds cumulative over lifetime with no operating restrictions, 2.0 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C.
[3] Allowed 1.65V – 1.8V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C.
[4] Allowed 1.92V - 2.16V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C
[5] VEXTAL/ VXTAL (min) is for powered condition. VEXTAL/VXTAL (min) can be lower in unpowered condition.
[6] The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
[7] Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum Tj, with VREFH_1P5_ADC <= 1.65 V, VREFL_1P5_ADC = 0V. Allowed for unlimited duration if the device is unpowered.
[8] DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of tSIGNAL.
[9] Non-disturb of ADC channels during current injection cannot be guaranteed. The degradation in channel performance cannot be specified due to the dynamic operation of the ADC input mux and potential for varying charge distribution. For the max 1 mA DC injection quoted here, VAD_INPUT would be +/-0.84 V relative to VREFH_1P5_ADC/VREFL_1P5_ADC at max Tj. ADC Output of the channel into which injection occurs will saturate depending on the direction of injection and for the channels not subject to current injection Offset error would be -6 LSB to 6 LSB and TUE would be -10 LSB to 10 LSB.
[10] Solder profile per IPC/JEDEC J-STD-020D.
[11] Moisture sensitivity per JEDEC test method A112.
[12] For AC Signals in a 1.8V supply domain, max VIN overshoot is limited to VDD_IO+20% for 10% of tSIGNAL.

Note: *The maximum current supported on all interfaces is governed by the maximum total load capacitance driven as shown in the "reference load diagram" in “GPIO pads output characteristics” section at the maximum speed of the IO specified for that interface.*

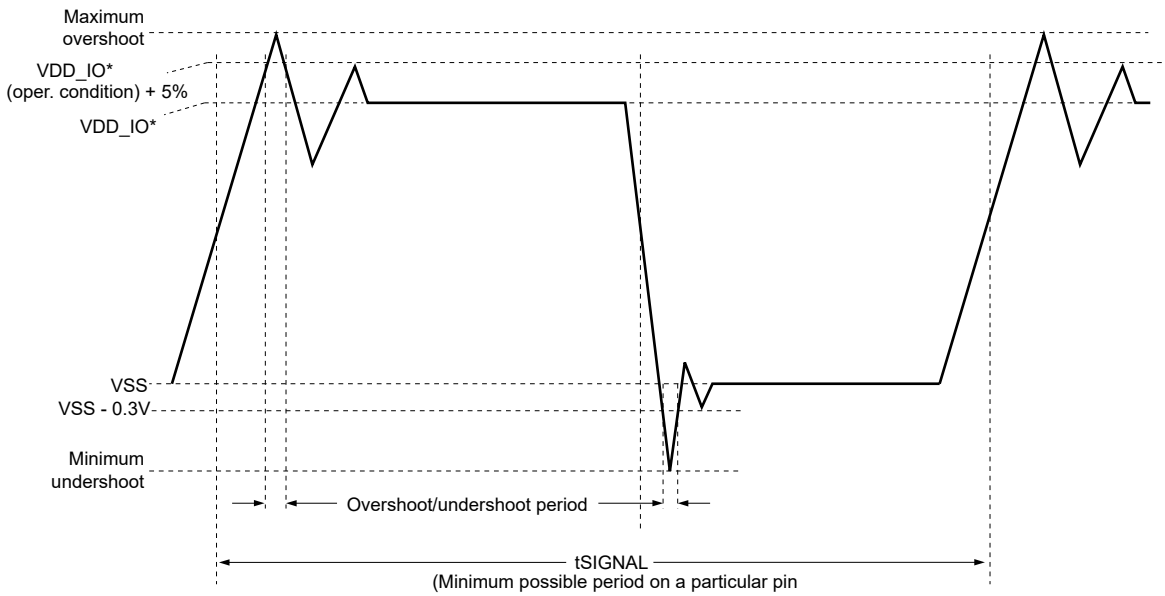

Figure 3. Soc-pin overshoot/undershoot voltage for each GPIO pad type

7 Operating Conditions

7.1 Operating Conditions

The following table describes the functional operating conditions for the device, and for which all specifications in this datasheet are valid, except where explicitly noted. Device behavior is not guaranteed for operation outside of the conditions in this table.

Note: *All specifications associated with VIN are measured at the SoC pin.*

Table 4. Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
fSYS_R52	Cortex-R52 core operating frequency [1][2][3]	—	—	1200	MHz	—
fSYS_M7	FSS Cortex-M7 core operating frequency [1][2][3]	—	400	400	MHz	—
fSYS_AUX	Aux Core operating frequency [1][2][3]	300	600	600	MHz	—
Tj	Junction Temperature Range [1][4]	-40	—	125	C	—
Ta	Ambient Temperature Range [1]	-40	—	105	C	—
VDD	SoC Core Supply - Main [1][5]	0.737	0.77	0.825	V	DIE_PROCESS[1:0] fuse setting = b00
VDD	SoC Core Supply - Main [1][5]	0.707	0.74	0.825	V	DIE_PROCESS[1:0] fuse setting = b01
VDD_AO	FSS Core Supply - Always On [1][5]	0.737	0.77	0.825	V	DIE_PROCESS[1:0] fuse setting = b00

Table continues on the next page...

Table 4. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_AO	FSS Core Supply - Always On [1][5]	0.707	0.74	0.825	V	DIE_PROCESS[1:0] fuse setting = b01
VSS	Ground Supply [1]	—	0	—	V	—
VDD2H_1PX_IO_SMMS0	LPDDR4X VDD2H IO supply for DDR PHY - Main [1]	1.06	1.1	1.17	V	—
VDD2H_1PX_IO_SMMS0	LPDDR5X VDD2H IO supply for DDR PHY - Main [1]	1.01	1.05	1.12	V	—
VDDA_1PX_VDD2H_SMMS0	LPDDR4X Analog Supply for DDR PHY PLL - Main [1]	1.06	1.1	1.17	V	—
VDDA_1PX_VDD2H_SMMS0	LPDDR5X Analog Supply for DDR PHY PLL - Main [1]	1.01	1.05	1.12	V	—
VDDQ_0PX_IO_SMMS0	LPDDR4X VDDQ IO supply for DDR PHY - Main [1]	0.57	0.6	0.65	V	—
VDDQ_0PX_IO_SMMS0	LPDDR5X VDDQ IO supply for DDR PHY - Main [1]	0.47	0.5	0.57	V	—
VDD_IO_1P5_SD0	SerDes supply (int regulation) - Main [1][6]	1.42	1.5	1.65	V	—
VDD_IO_SD0	SerDes0 IO supply -Main [1][5][6]	0.737	0.77	0.825	V	DIE_PROCESS[1:0] fuse setting = b00
VDD_IO_SD0	SerDes0 IO supply -Main [1][5][6]	0.707	0.74	0.825	V	DIE_PROCESS[1:0] fuse setting = b01
VDDA_1P5_ANAx	Common Analog Supply for Anamixes - Main [1]	1.42	1.5	1.65	V	—
VDD_IO_1P8_AO	IO Supply - Always-On [1]	1.7	1.8	1.92	V	—
VDD_1P8_EFUSE	Supply for Fuse Block [1][7][8][9]	1.7	1.8	1.92	V	—
VDD_IO_1P8_CAN	IO supply - Main for CAN, LIN, FR IO [1]	1.7	1.8	1.92	V	—
VDD_IO_1P8_ETH	NWS LVCMOS IO supply for Networking SS IO [1]	1.7	1.8	1.92	V	—
VDD_IO_1P8_MAIN_FSIO	FSS IO supply - Main [1]	1.7	1.8	1.92	V	—
VDD_IO_1P8_MAIN_MSIO	COS IO supply - Main [1]	1.7	1.8	1.92	V	—
VDDA_1P5_FSS_FOSC	FSS analog supply for FXOSC - Main [1]	1.42	1.5	1.65	V	—
VDD_RTU	RTU Core Supply - Switchable [1][5]	0.737	0.77	0.825	V	DIE_PROCESS[1:0] fuse setting = b00
VDD_RTU	RTU Core Supply - Switchable [1][5]	0.707	0.74	0.825	V	DIE_PROCESS[1:0] fuse setting = b01

Table continues on the next page...

Table 4. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VREFH_1P5_ADC	ADC Reference High Voltage (VREFH_ADC) [1]	1.42	1.5	1.65	V	—
VREFL_1P5_ADC	ADC Reference Low Voltage (V REFL_ADC) [1]	—	0	—	V	—
VIN_18	1.8V GPIO input voltage range [1][10][11][12]	VSS - 0.3	—	VDD_IO_ * + 0.3	V	—
ΔVDD	0.77V supply voltage differential [1][13]	-25	—	25	mV	Applies to all 0.77V supplies on the device.
ΔVDD_HV_18	1.8V supply voltage differential group [1][7][8][13]	-25	—	25	mV	—
ΔVDD_HV_15_ ANA	1.5V analog supply voltage differential group [1][13][14]	-25	—	25	mV	Applies to all 1.5V analog supplies on the device.
VRAMP_LV	LV supply voltage ramp-up rate [1]	0.001	—	20	V / ms	Applies to 0.77V supplies
VRAMP_HV_15	1.5V supply voltage ramp-up rate [1]	0.001	—	20	V / ms	Applies to 1.5V supplies
VRAMP_HV_18	1.8V supply voltage ramp-up rate [1]	0.001	—	50	V / ms	Applies to 1.8V supplies
VRAMP_DDR	DDR supply voltage ramp-up rate	0.001	—	50	V / ms	VDD2H_1PX_IO_ SMMS, VDDA_1PX_ VDD2H_SMMS, VDDQ_0PX_IO_SMMS
TDISCHARGE_ STDBY	Supply discharge time during Stop/ Sleep mode entry [1]	—	2.5	—	ms	Applies to all switchable supplies during Stop/ sleep mode entry
VAD_INPUT	ADC input voltage range [1][15]	VREFL_1 P5_ADC	—	VREFH_ 1P5_AD C	V	—
IINJ_D	GPIO Input DC Injection Current [1]	-1	—	1	mA	Unpowered
IINJ_D	GPIO Input DC Injection Current [1]	0	—	0	mA	Powered
IINJ_A	SAR ADC Input DC Injection Current [1][16][17]	-1	—	1	mA	—

[1] The operating conditions in this table apply as required conditions for all other specifications in this document, unless explicitly noted as an exception in another section of this document.
[2] The stated maximum operating frequency must be observed when using the PLL with frequency modulation enabled. Center-spread modulation is supported in cases where the nominal operating frequency plus half the modulation depth is less than the stated maximum frequency.
[3] A table of valid values for this clock can be found in the Clocking Chapter in the Reference Manual. Values not listed in the said reference manual table are not supported.
[4] Lifetime operation at Tj max not guaranteed. Automotive Mission Profile Input per AEC standard, assumed for performance and warrant the reliability.
[5] SVS guidelines apply to all LV supplies on the device. See power management chapter of device reference manual for details on SVS.
[6] SerDes supplies must ramp for the SerDes PHY to safely power up into its reset state. Until both supplies are ramped, the SerDes PHY will be in an undefined state.

[7] VDD_1P8_EFUSE must be grounded when not actively programming the fuses. This supply is not required to be powered for fuse reads. See device hardware design guidelines document for more details.
[8] See "Power Sequencing" section for the relationship of VDD_1P8_EFUSE powering up/down relative to the core, high-voltage, and I/O supplies.
[9] The VDD_1P8_EFUSE supply must be maintained within specification during fuse programming. Failure to do this may result in improper functionality of the device after fuse programming
[10] For AC signals, allowed max VIN ≤ VDD_IO* for lifetime operation. If AC overshoot beyond VDD_IO* occurs, then refer to the Abs Max duration constraints as a function of the amount of overshoot. For DC signals ≥ VDD_IO, VIN-VDD_IO* ≤ 0.3V is allowed for lifetime operation.
[11] The min DC VIN level for a powered device is -0.3V. If AC undershoot below -0.3V occurs, then refer to the Abs Max duration constraints as a function of the amount of undershoot.
[12] DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of tSIGNAL.
[13] The "voltage differential" refers to the difference between the lowest and highest voltages across all supplies within the supply group as defined under Condition column.
[14] VREFH_1P5_ADC allows a differential voltage of 100 mV.
[15] The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
[16] The SAR ADC electrical specifications are not guaranteed during any period when the operating injection current limit is violated. These specifications are at maximum Tj and VREFH_1P5_ADC=1.5V; the injected current will reduce with reduced Tj.
[17] Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum Tj, with VREFH_1P5_ADC <= 1.65 V, VREFL_1P5_ADC = 0V. Allowed for unlimited duration if the device is unpowered.

The “fuse setting” values/conditions in above table correspond with the DIE_PROCESS[1:0] fuses which NXP programs during manufacturing. See Reference Manual and it’s Fuse Map for further details about the purpose. Example: Value “b01” represents DIE_PROCESS[1]=0 and DIE_PROCESS[0]=1”.

VDD must ramp for the DDR to safely power up into its reset state. Until VDD supply is ramped, the DDR will be in undefined state.

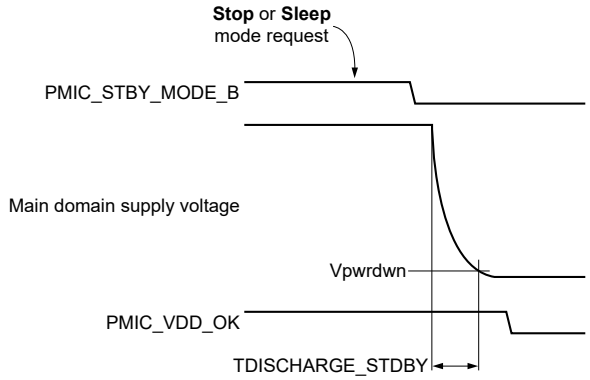

Figure 4. TDISCHARGE STDBY definition

7.2 Clock frequency ranges

The following table gives the frequency range minimum and maximums to use when programming the clock dividers on the device.

Table 5. Clock frequency ranges

Symbol	Description	Min	Typ	Max	Unit	Condition
fLBIST_CLK	LBIST clock frequency	—	—	400	MHz	LBIST_CLK
fXBAR_CLK	XBAR clock frequency [1]	—	—	800	MHz	XBAR_CLK
fDAPB_CLK	Debug clock (FSS) frequency	—	—	189	MHz	fDAPB_CLK
fFRAY_CHI	FlexRay CHI clock frequency	—	200	200	MHz	—
fPCIe_CTRL_CLK	PCIe control clock frequency	250	300	300	MHz	PCIE_CLK (Gen4)
fPCIe_CTRL_CLK	PCIe control clock frequency	125	300	300	MHz	PCIE_CLK (Gen3)
fPCIe_CTRL_CLK	PCIe control clock frequency	62.5	300	300	MHz	PCIE_CLK (Gen2)

Table continues on the next page...

Table 5. Clock frequency ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fSERDES_REF_CLK	SERDES reference clock frequency	—	100	100	MHz	SERDES_REF_CLK
fFSS_PER_CLK	FSS Peripheral clock frequency	—	—	100	MHz	FSS_PER_CLK
fHKI_FTM0_CLK	FlexTimer 0 external clock frequency	—	—	24	MHz	HKI_FTM0_CLK
fHKI_FTM1_CLK	FlexTimer 1 external clock frequency	—	—	24	MHz	HKI_FTM1_CLK
fTPIU_CLK	TPIU clock frequency	320	—	400	MHz	—
fTRACE_TS_CLK	Trace TS clock frequency	—	—	50	MHz	—
fSAI_CLK	SAI clock frequency	—	—	49.152	MHz	—
fFLEXRAY_PE_CLK	FlexRay PE clock frequency	40	80	160	MHz	FLEXRAY_PE_CLK
fCAN_FD_PE_CLK	CAN-FD PE clock frequency	40	80	80	MHz	CAN_FD_PE_CLK
fCAN_XL_PE_CLK	CAN-XL PE clock frequency	40	160	200	MHz	CAN_XL_PE_CLK
fLIN_BAUD_CLK	LIN baud clock frequency	—	—	133	MHz	LIN_BAUD_CLK
fLINFLEXD_CLK	LIN clock frequency	—	—	100	MHz	LINFLEXD_CLK
fNETC_CLK	NETC clock frequency	—	—	400	MHz	NETC_CLK
fNETC_1588_CLK	NETC 1588 clock frequency	—	—	200	MHz	NETC_1588_CLK
fCAAM_AES_CLK	CAAM AES clock frequency	—	—	300	MHz	CAAM_AES_CLK
fETH_MAC_0_TX_CLK	MAC_0 transmit clock frequency	2.5	—	312.5	MHz	ETH_MAC_0_TX_CLK
fETH_MAC_0_RX_CLK	MAC_0 receive clock frequency	2.5	—	312.5	MHz	ETH_MAC_0_RX_CLK
fETH_MAC_0_REF_CLK	MAC_0 reference clock frequency	—	—	50	MHz	ETH_MAC_0_REF_CLK
fETH_MAC_0_TX_CLK	MAC_1 transmit clock frequency	2.5	—	312.5	MHz	ETH_MAC_0_TX_CLK
fETH_MAC_0_RX_CLK	MAC_1 receive clock frequency	2.5	—	312.5	MHz	ETH_MAC_0_RX_CLK
fETH_MAC_0_REF_CLK	MAC_1 reference clock frequency	—	—	50	MHz	ETH_MAC_0_REF_CLK
fDSPI_CLK	DSPI clock frequency	10	—	160	MHz	DSPI_CLK
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	400	MHz	QSPI_2X_CLK - DDR 200MHz
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	333	MHz	QSPI_2X_CLK - DDR 166MHz

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Table 5. Clock frequency ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	266	MHz	QSPI_2X_CLK - DDR / SDR 133MHz
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	208	MHz	QSPI_2X_CLK - SDR 104MHz
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	200	MHz	QSPI_2X_CLK - SDR 100MHz
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	133	MHz	QSPI_2X_CLK - DDR 66MHz
fSDHC_CLK	uSDHC clock frequency	133	—	200	MHz	SDHC_CLK - DDR HS400
fSDHC_CLK	uSDHC clock frequency	—	—	200	MHz	SDHC_CLK - SDR HS200
fSDHC_CLK	uSDHC clock frequency	—	—	100	MHz	SDHC_CLK - SDR 100MHz
fSDHC_CLK	uSDHC clock frequency	—	—	50	MHz	SDHC_CLK - DDR / SDR 52MHz

[1] A table of valid values for this clock can be found in the Clocking Chapter in the Reference Manual. Values not listed in the said reference manual table are not supported.

8 Thermal Characteristic

Table 6. Thermal Attributes

Board Type[1]	Symbol	Description	Value	Unit
JESD51-9, 2s2p	$R_{\theta JA}$	Junction to Ambient Thermal Resistance1[2]	12.1	°C/W
JESD51-9, 2s2p	Ψ_{JT}	Junction-to-Top of Package Thermal Characterization Parameter [2]	0.2	°C/W
N/A	$R_{\theta JC}$	Junction to Case Thermal Resistance[3]	0.4	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9)
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the top side lid temperature

9 DC electricals

9.1 Total power specifications for 0.77V core and 1.5V Analog Domains

The following table contains the individual max and thermal 0.77V power figures for each phantom in the S32N device as well as a 1.5V analog total which applies to all devices. For I/O power specifications please see dedicated I/O table.

Table 7. Total power specifications for 0.77V core and 1.5V Analog Domains

Symbol	Description	Min	Typ	Max	Unit	Condition
—	0.77V Main Supply Rail Power: S32N55 Thermal Usecase [1]	—	—	4.5	W	Tj=125C, Typical Voltage, All core voltage supplies except VDD_RTU and VDD_AO; Sum of VDD, VDD_IO_SD0 (main supply).
—	0.77V Switchable Supply Rail Power: S32N55 Thermal Usecase [1]	—	—	3.2	W	Tj=125C, fSYS_R52=1.2 GHz, Typical Voltage, VDD_RTU supply
—	0.77V Switchable Supply Rail Power: S32N55 Thermal Usecase [1]	—	—	3	W	Tj=125C, fSYS_R52=1.0 GHz, Typical Voltage, VDD_RTU supply
—	0.77V Switchable Supply Rail Power: S32N55 Thermal Usecase [1]	—	—	2.8	W	Tj=125C, fSYS_R52=800 MHz, Typical Voltage, VDD_RTU supply
—	0.77V Switchable Supply Rail Power: S32N53 Thermal Usecase [1]	—	—	2.5	W	Tj=125C, fSYS_R52=1.2 GHz, Typical Voltage, VDD_RTU supply, 1x RTU clock gated and SRAM in shutdown mode
—	0.77V Switchable Supply Rail Power: S32N53 Thermal Usecase [1]	—	—	2.4	W	Tj=125C, fSYS_R52=1.0 GHz, Typical Voltage, VDD_RTU supply, 1x RTU clock gated and SRAM in shutdown mode
—	0.77V Switchable Supply Rail Power: S32N53 Thermal Usecase [1]	—	—	2.2	W	Tj=125C, fSYS_R52=800 MHz, Typical Voltage, VDD_RTU supply, 1x RTU clock gated and SRAM in shutdown mode
—	0.77V AON Supply Rail Power: S32N55 Thermal Usecase [1]	—	—	10.9	mW	Tj=125C, Typical Voltage, VDD_AO supply, Functional mode
—	1.5V Analog Supply Rail power: All devices [1]	—	—	0.17	W	Tj=125C, Sum of VDDA_1P5_CIS, VDDA_1P5_ANA1, VDDA_1P5_

Table continues on the next page...

Table 7. Total power specifications for 0.77V core and 1.5V Analog Domains...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						ANA2, VDDA_1P5_ ANA3, VDDA_1P5_ FSS_FOSC

[1] Thermal usecase: This is provided for designing a thermal solution. This is a realistic maximum sustained usecase which would be maintained for a longer duration.

9.2 Static power specifications for I/O Domains

The following table contains the static power consumption for each I/O power domain. This data does not include the usage dependent dynamic current of GPIO-pins. To estimate the dynamic GPIO current for a specific use-case, an IO calculator tool is available. For IO calculator, contact your NXP sales representative. The " Device Power and Operating Current Specifications" table contains pre-calculated total I/O power (static + dynamic) for common usecases.

Table 8. Static power specifications for I/O Domains

Symbol	Description	Min	Typ	Max	Unit	Condition
SPVDD_IO_SMM0	1.1V Static Power on VDD2H_1PX_IO_SMMS0 - LPDDR4x	—	—	0.14	mW	VDD2H_1PX_IO_ SMMS0 = 1.1V
SPVDD_IO_SMM0	1.05V Static Power on VDD2H_1PX_IO_SMMS0 - LPDDR5x	—	—	0.13	mW	VDD2H_1PX_IO_ SMMS0 = 1.05V
SPVDDQ_IO_ SMM0	0.6V Static Power on VDDQ_0PX_IO_SMMS0 - LPDDR4x	—	—	3.5	mW	VDDQ_0PX_IO_ SMMS0 = 0.6V
SPVDDQ_IO_ SMM0	0.5V Static Power on VDDQ_0PX_IO_SMMS0 - LPDDR5x	—	—	2.1	mW	VDDQ_0PX_IO_ SMMS0 = 0.5V
SPVDD_IO_1P5_ SD0	1.5V Static power on VDD_IO_1P5_SD0	—	—	1.7	mW	VDD_IO_1P5_SD0 = 1.5V
SPVDD_IO_1P8_ ETH	1.8V Static power on VDD_IO_1P8_ETH	—	—	10.7	mW	VDD_IO_1P8_ETH = 1.8V
SPVDD_IO_1P8_ CAN	1.8V Static power on VDD_IO_1P8_CAN	—	—	4.1	mW	VDD_IO_1P8_CAN = 1.8V
SPVDD_IO_1P8_ AO	1.8V Static power on VDD_IO_1P8_AO	—	—	6.1	mW	VDD_IO_1P8_AO = 1.8V
SPVDD_IO_1P8_ MAIN_FSIO	1.8V Static power on VDD_IO_1P8_MAIN_FSIO	—	—	16.3	mW	VDD_IO_1P8_MAIN_ FSIO = 1.8V
SPVDD_IO_1P8_ MAIN_MSIO	1.8V Static power on VDD_IO_1P8_MAIN_MSIO	—	—	11.2	mW	VDD_IO_1P8_MAIN_ MSIO = 1.8V

9.3 Device Power and Operating Current Specifications

The device power consumption, operating current, and applicable conditions are given in the following table.

Note: *All measurements are at Tj=125C, unless otherwise specified.*

Table 9. Device Power and Operating Current Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
PVDD_AO	Stop/Sleep mode core supply power	—	215	—	uW	Tj = 25C, VDD_AO = 0.77V, typical silicon, all pull up/down disabled except for FSS WKUP [3:0] pads
PVDD_IO_1P8_AO	Stop/Sleep mode I/O supply power	—	35	—	uW	Tj = 25C, VDD_IO_1P8_AO = 1.8V, typical silicon, all pull up/down disabled except for FSS WKUP [3:0] pads
PVDD_IO_1P8_AO	HPRUN mode I/O supply power	—	20	—	mW	Tj = 125C, VDD_IO_1P8_AO = 1.8V, typical silicon, all pull up/down disabled except for FSS WKUP [3:0] pads, no outputs toggling (same as STOP/SLEEP).
IDD_FXOSC	VDDA_1P5_FSS_FOSC operating current	—	12	—	mA	VDDA_1P5_FSS_FOSC = 1.5V, 40MHz
IDD_VDDA_1PX_VDD2H_SMMS0	VDDA_1PX_VDD2H_SMMS0 operating current	—	7	—	mA	VDDA_1PX_VDD2H_SMMS0 = 1.1V for LPDDR4X
IDD_VDDA_1PX_VDD2H_SMMS0	VDDA_1PX_VDD2H_SMMS0 operating current	—	12	—	mA	VDDA_1PX_VDD2H_SMMS0 = 1.05V for LPDDR5X
IDD_EFUSE_PGM	VDD_EFUSE programming current	—	416	—	mA	VDD_1P8_EFUSE=1.8V
PVDD_IO_1P5_SD0	PVDD_IO_1P5_SD0 operating power	—	265	—	mW	All circuits enabled, VDD_IO_1P5_SD0=1.5V, 2 lanes PCIe Gen4, 2 lanes 2.5G SGMII
PVDD_IO_1P5_SD0	PVDD_IO_1P5_SD0 operating power	—	90	—	mW	All circuits enabled, VDD_IO_1P5_SD0=1.5V, 2 lanes idle, 2 lanes 1G SGMII
PVDD_IO_1P5_SD0	PVDD_IO_1P5_SD0 operating power	—	105	—	mW	All circuits enabled, VDD_IO_1P5_SD0=1.5V, 2 lanes idle, 2 lanes 2.5G SGMII

Table continues on the next page...

Table 9. Device Power and Operating Current Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
PVDD_IO_1P5_SD0	PVDD_IO_1P5_SD0 operating power	—	1.4	—	mW	VDD_IO_1P5_SD0=1.5V, all lanes disabled
PVDDQ_0PX_IO_SMMS0_MAX	VDDQ_0PX_IO_SMMS0 100% write operating power for LPDDR5X	—	185	—	mW	LPDDR5X, VDDQ_0PX_IO_SMMS0 = 0.5V, 100% Write operation, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load
PVDDQ_0PX_IO_SMMS0_IDLE	VDDQ_0PX_IO_SMMS0 idle power for LPDDR5X	—	85	—	mW	LPDDR5X, VDDQ_0PX_IO_SMMS0= 0.5V, Tj=25C
PVDDQ_0PX_IO_SMMS0_MAX	VDDQ_0PX_IO_SMMS0 100% write operating power for LPDDR4X	—	113	—	mW	LPDDR4X, VDDQ_0PX_IO_SMMS0 = 0.6V, 100% Write operation, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load
PVDDQ_0PX_IO_SMMS0_IDLE	VDDQ_0PX_IO_SMMS0 idle power for LPDDR4X	—	11.89	—	mW	LPDDR4X, VDDQ_0PX_IO_SMMS0 = 0.6V, Tj=25C
PVDD2H_1PX_IO_SMMS0_RET	VDD2H_1PX_IO_SMMS0 data retention power for LPDDR5X	—	0.02	—	mW	LPDDR5X, VDD2H_1PX_IO_SMMS0 = 1.05V, Stop/Sleep mode and DRAM in self-refresh, Tj=25C.
PVDD2H_1PX_IO_SMMS0_TYP	VDD2H_1PX_IO_SMMS0 typical operating power for LPDDR5X	—	7.95	—	mW	LPDDR5X, VDD2H_1PX_IO_SMMS0 = 1.05V, 75% Read, 25% Write, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load
PVDD2H_1PX_IO_SMMS0_RET	VDD2H_1PX_IO_SMMS0 data retention power for LPDDR4X	—	0.02	—	mW	LPDDR4X, VDD2H_1PX_IO_SMMS0 = 1.1V, Stop/Sleep mode and DRAM in self-refresh, Tj=25C.
PVDD2H_1PX_IO_SMMS0_TYP	VDD2H_1PX_IO_SMMS0 typical operating power for LPDDR4X	—	0.63	—	mW	LPDDR4X, VDD2H_1PX_IO_SMMS0 = 1.1V, 100% Write

Table continues on the next page...

Table 9. Device Power and Operating Current Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						operation, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load
PVDD_IO_1P8_MAIN_MSIO	VDD_IO_1P8_MAIN_MSIO operating power (COS IOs)	—	19	—	mW	1.8V, 100% clock rate, 50% data rate, 1/2 data switching per cycle
PVDD_IO_1P8_ETH0	VDD_IO_1P8_ETH operating power for Ethernet0 interface	—	125	—	mW	1.8V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, for Ethernet0, does not include power for other I/O pins on the VDD_IO_1P8_ETH supply. 15.5pF
PVDD_IO_1P8_ETH1	VDD_IO_1P8_ETH operating power for Ethernet1 interface	—	125	—	mW	1.8V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, for Ethernet1, does not include power for other I/O pins on the VDD_IO_1P8_ETH supply. 15.5pF
PVDD_IO_1P8_CAN	VDD_IO_1P8_CAN, LIN, FR operating power	—	7	—	mW	1.8V, Bit rate 5Mbps; Bus loaded 60%
PVDD_IO_1P8_MAIN_FSIO	VDD_IO_1P8_MAIN_FSIO operating power (FSS IOs)	—	14	—	mW	1.8V, 100% clock rate, 50% data rate, 1/2 data switching per cycle

Note: *PVDD_AO + PVDD_IO_1P8_AO provides the Stop/Sleep mode power.*

9.4 Leakage power

The following table contains the individual leakage power for the 0.77V core and switchable supplies at different temperatures.

Table 10. Leakage power

Symbol	Description	Min	Typ	Max	Unit	Condition
—	0.77V Main Supply leakage Power	—	—	1.9	W	Tj=125C, Typical Voltage, Sum of VDD and VDD_IO_SD0
—	0.77V Main Supply leakage Power	—	—	0.7	W	Tj=80C, Typical Voltage, Sum of VDD and VDD_IO_SD0

Table continues on the next page...

Table 10. Leakage power...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	0.77V Main Supply leakage Power	—	—	266	mW	Tj=40C, Typical Voltage, Sum of VDD and VDD_IO_SD0
—	0.77V Main Supply leakage Power	—	—	187	mW	Tj=25C, Typical Voltage, Sum of VDD and VDD_IO_SD0
—	0.77 switchable supply leakage power	—	—	1.9	W	Tj=125C, Typical Voltage, VDD_RTU supply
—	0.77V AON Supply leakage Power	—	—	13.1	mW	Tj=125C, Typical Voltage, VDD_AO supply
—	0.77V AON Supply leakage Power	—	—	3.3	mW	Tj=80C, Typical Voltage, VDD_AO supply
—	0.77V AON Supply leakage Power	—	—	1.0	mW	Tj=40C, Typical Voltage, VDD_AO supply
—	0.77V AON Supply leakage Power	—	—	600	uW	Tj=25C, Typical Voltage, VDD_AO supply
—	1.5V Analog Supply leakage power	—	—	2.7	mW	Tj=125C, Sum of VDDA_1P5_ ANA1, VDDA_1P5_ ANA2, VDDA_1P5_ ANA3, VDDA_1P5_ FSS_FOSC
—	1.5V Analog Supply leakage power	—	—	1.4	mW	Tj=80C, Sum of VDDA_1P5_ ANA1, VDDA_1P5_ ANA2, VDDA_1P5_ ANA3, VDDA_1P5_ FSS_FOSC
—	1.5V Analog Supply leakage power	—	—	1.2	mW	Tj=40C, Sum of VDDA_1P5_ ANA1, VDDA_1P5_ ANA2, VDDA_1P5_ ANA3, VDDA_1P5_ FSS_FOSC
—	1.5V Analog Supply leakage power	—	—	1.0	mW	Tj=25C, Sum of VDDA_1P5_ ANA1, VDDA_1P5_ ANA2, VDDA_1P5_

Table continues on the next page...

Table 10. Leakage power...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						ANA3, VDDA_1P5_FSS_FOSC

10 Power sequencing

10.1 Power-up

The following sequence has been validated by NXP and is to be followed when powering up the device. Each supply within a step must be within its specified operating voltage range before the next step in the sequence is started, except as noted below.

1. Set POR_B input to low value.

2. Ramp up VDD, VDD_IO_SD0 (Serdes supply), VDD_AO together

3. Ramp up always-on IO (VDD_IO_1P8_AO)

4. Ramp up

Note: *While powering up the device, the VDD_1P8_EFUSE supply pin must be kept powered down. While the device is already powered up, the VDD_1P8_EFUSE supply pin can be powered up/down independent of the other supplies on the device. The VDD_1P8_EFUSE supply pin must be powered down prior to Stop/Sleep mode entry or, at the latest, powered down together with the other 1.8V supplies during Stop/sleep mode entry.*

- IO Main (VDD_IO_1P8_ETH, VDD_IO_1P8_CAN, VDD_IO_1P8_MAIN_FSIO, VDD_IO_1P8_MAIN_MSIO, VDD_1P8_EFUSE),

- DDR IO (VDD2H_1PX_IO_SMMS0, VDDA_1PX_VDD2H_SMMS0) and

- VDDQ (VDDQ_0PX_IO_SMMS0)

- Analog (VDDA_1P5_ANAx, VDDA_1P5_FSS_FOSC, VDD_IO_1P5_SD0, VREFH_1P5_ADC)

The different supply groups listed in step 4 (IO Main, DDR IO, VDDQ and Analog) can also be ramped up separately and in any order as long as they begin to ramp up only after all the supplies in step 3 have ramped up.

5. Set POR_B and PMIC_VDD_OK inputs to high value once all supplies have reached their specified levels.

Note: *If VDD_RTU is supplied by a regulator that can be turned on and off separately from VDD, it remains turned off until the SoC application instructs the PMIC to turn it on. Otherwise it is ramped up together with VDD in step 2.*

Note: *If VDD_IO_1P8_AO is supplied by the same voltage regulator as the IO Main supply mentioned above, it is turned on in the same step. In this case, it should be ensured that the Analog supply is powered after the IO Main and VDD_IO_1P8_AO supply.*

The power-up sequence on stop/sleep exit is the same as before, with the following exceptions:

- VDD_AO and VDD_IO_1P8_AO are already on

- POR_B input is kept high throughout the sequence.

10.2 Power-down

When powering down the SoC, it is recommended to use the reverse order from the power-up sequence. If this cannot be achieved, ensure that all supplies are below the Vpwrdwn level before powering up again.

Table 11. Power-down

Symbol	Description	Min	Typ	Max	Unit	Condition
Vpwrdwn	Maximum voltage on a supply pin in powerdown mode	—	—	100	mV	—

10.3 Recommended NXP PMIC

The recommended NXP PMIC for this device is FS04 and PF53.

For more information on the PMIC, see product webpage on nxp.com or contact NXP sales representative.

11 I/O Pad Characteristics

11.1 GPIO pads general characteristics

There are four GPIO types on the device:

- FSIO Fast Speed IO: Typically used for hi-speed serial interfaces (1.8V)
- MSIO Medium Speed IO: Used for serial interfaces like SPI (1.8V)
- SSIO Slow Speed IO. DC input and slow switching interfaces (1.8V)
- SSRx Slow Speed Receiver: Input only used for wakeup from stop/sleep and slow switching inputs (1.8V)

SRE=0 is applicable to pad type 1.8V FSIO only. For all other pad types (MSIO & SSIO) SRE is non configurable (SLOW by default), and changing SRE will have no impact.

Table 12. GPIO pads general characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
R_PUPD	GPIO pull up/down resistance	9	15	21	kΩ	pull up @ 0.25 * VDD_IO_*, pull down @ 0.75 * VDD_IO_*
VISE_18	Pad indeterminate state end threshold	—	—	1.2	V	FSIO | MSIO | SSIO | SSRx See GPIO pad detailed behavior diagram below

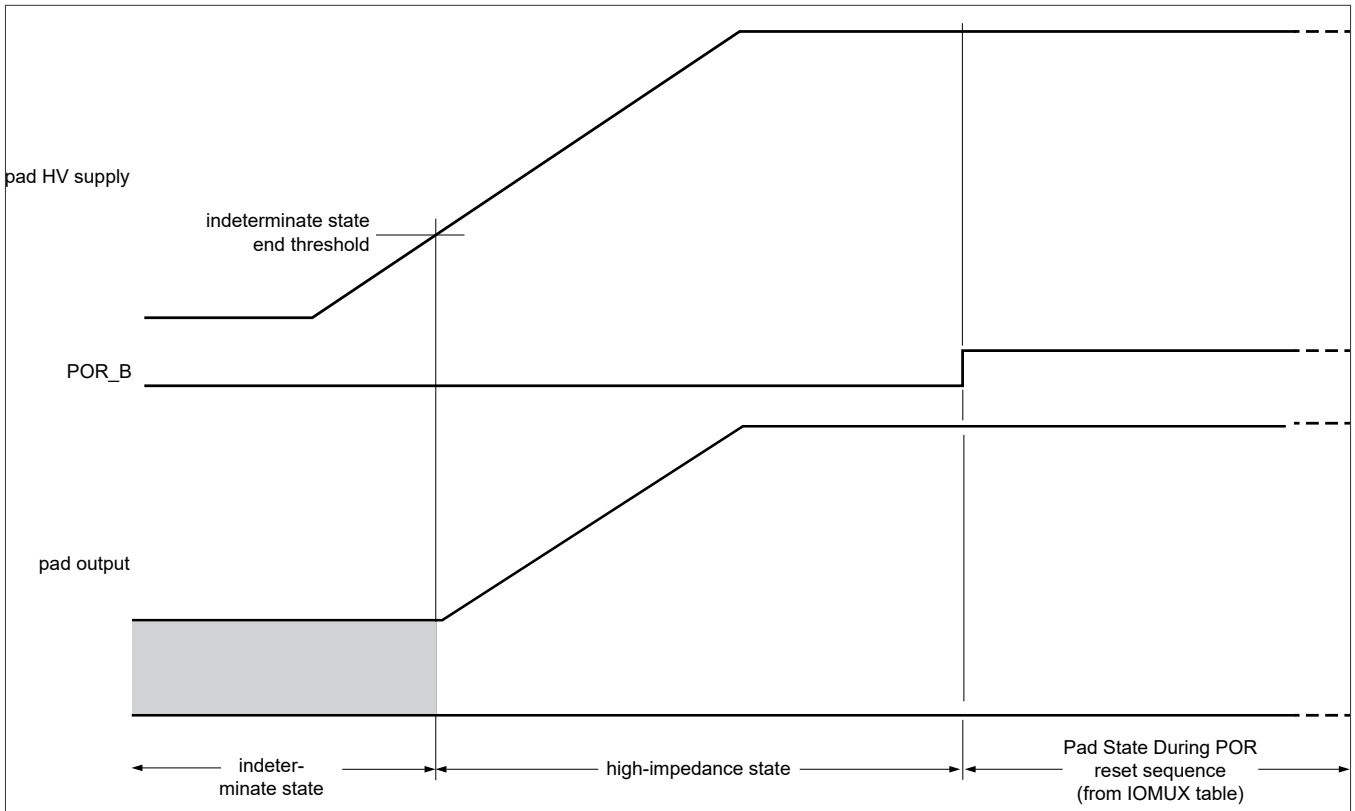


Figure 5. GPIO pad detailed behavior during power up

11.2 GPIO pads input characteristics

Table 13. GPIO pads input characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH (min)	Input high level DC voltage threshold	75	—	—	% of VDD_IO_*	Applies to all IO types
VIL (max)	Input low level DC voltage threshold	—	—	25	% of VDD_IO_*	Applies to all IO types
VHYS	Input hysteresis voltage	100	—	—	mV	Applies to all pad types except FSIO.
ILKG	Input leakage current	-30	—	30	uA	FSIO 1.8V + 7%, 125C
ILKG	Input leakage current	-30	—	30	uA	MSIO 1.8V + 7%, 125C
ILKG	Input leakage current	-5	—	5	uA	SSIO 1.8V + 7%, 125C
ILKG	Input leakage current	-0.5	—	0.5	uA	SSRx 1.8V + 7%, 125C
CIN	Input capacitance	—	—	6	pF	FSIO | MSIO | SSIO Includes pad and package components

Table continues on the next page...

Table 13. GPIO pads input characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN	Input capacitance	—	—	5	pF	SSRx Includes pad and package components
ISLEW	Input signal slew rate [1][2]	1.6	—	4	V / ns	FSIO
ISLEW	Input signal slew rate [2]	1	—	4	V / ns	MSIO | SSIO | SSRx
FMAX_IN	Input frequency	—	—	208	MHz	FSIO
FMAX_IN	Input frequency	—	—	50	MHz	MSIO
FMAX_IN	Input frequency	—	—	20	MHz	SSIO | SSRx
TPW_MIN	Input minimum pulse width	1 / (2 * FMAX_IN)	—	—	ns	Applies to all IO types
TFILT	Input glitch filter max filtered pulse width [3][4][5]	—	—	20	ns	SSRx
TUNFILT	Input glitch filter min unfiltered pulse width [3][5][6]	400	—	—	ns	SSRx

[1] Fastest slew rate constraint required to meet high-speed interface timing such as QSPI, RGMII, and uSDHC. Slower input transitions can be used for input signals with slow switching rates (<40 MHz).
[2] Input slew rate limits must be adhered to in conjunction with the max input frequency limits given for proper operation.
[3] An input signal pulse is defined by the duration of the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
[4] Pulses shorter than defined by the maximum are guaranteed to be filtered (not passed).
[5] Pulses in between the max filtered and min unfiltered may or may not be passed through the filter.
[6] Pulses larger than defined by the minimum are guaranteed not to be filtered (passed).

11.3 GPIO pads output characteristics

Table 14. GPIO pads output characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
R_RSTOUT_PD	Reset Output pull-down resistance	40	—	300	Ω	—
RDSON	Output impedance (NMOS & PMOS)	28	40	56	Ω	FSIO measured at 50% * (VDDIO_18 - VSS)
RDSON	Output impedance (NMOS & PMOS)	37	50	75	Ω	MSIO measured at 50% * (VDDIO_18 - VSS)
RDSON	Output impedance (NMOS & PMOS)	37	50	75	Ω	SSIO measured at 50% * (VDDIO_18 - VSS)
IOL	Output low current [1]	6	—	12	mA	FSIO, 20% of of applied supply voltage
IOL	Output low current [1]	4	—	9	mA	MSIO, 20% of of applied supply voltage
IOL	Output low current [1]	3.5	—	8.75	mA	SSIO, 20% of of applied supply voltage

Table continues on the next page...

Table 14. GPIO pads output characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IOH	Output high current [1]	-12	—	-6	mA	FSIO, 80% of applied supply voltage
IOH	Output high current [1]	-9	—	-4	mA	MSIO, 80% of applied supply voltage
IOH	Output high current [1]	-8.75	—	-3.5	mA	SSIO, 80% of applied supply voltage
VOL	Output low voltage	—	—	20	% * VDD_IO_18	FSIO @ 4mA (~81 ohms @ 1.62*0.2x)
VOL	Output low voltage	—	—	20	% * VDD_IO_18	MSIO / SSIO @ 2mA (~162 ohms @ 1.62*0.2x)
VOH	Output high voltage	80	—	—	% * VDD_IO_18	FSIO @ 4mA (~81 ohms @ 1.62*0.8x)
VOH	Output high voltage	80	—	—	% * VDD_IO_18	MSIO | SSIO @ 2mA (~162 ohms @ 1.62*0.8x)
FMAX_OUT	Output frequency [2][3][4]	—	—	208	MHz	FSIO FAST slew rate setting
FMAX_OUT	Output frequency [2][3][4]	—	—	100	MHz	FSIO SLOW slew rate setting
FMAX_OUT	Output frequency [2][3][4]	—	—	50	MHz	MSIO
FMAX_OUT	Output frequency [2][3][4]	—	—	20	MHz	SSIO
TR_TF	Output rise/fall time [2][3][4][5]	1	—	6	V / ns	FSIO FAST slew rate setting
TR_TF	Output rise/fall time [2][3][4][5]	0.5	—	4	V / ns	FSIO SLOW slew rate setting
TR_TF	Output rise/fall time [2][3][4][5]	0.28	—	5	V / ns	MSIO
TR_TF	Output rise/fall time [2][3][4][5]	0.28	—	5	V / ns	SSIO

[1] The IOL and IOH must not be used to drive those current levels into DC loads. IO specifications are for driving capacitive loads and if there is a need to DC drive loads, contact NXP sales representative for further guidance.
[2] GPIO output transistion time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
[3] I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
[4] Output timing valid for maximum external load C L = 20pF (includes PCB trace, package trace, and flash input load).
[5] Rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDDIO* level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.

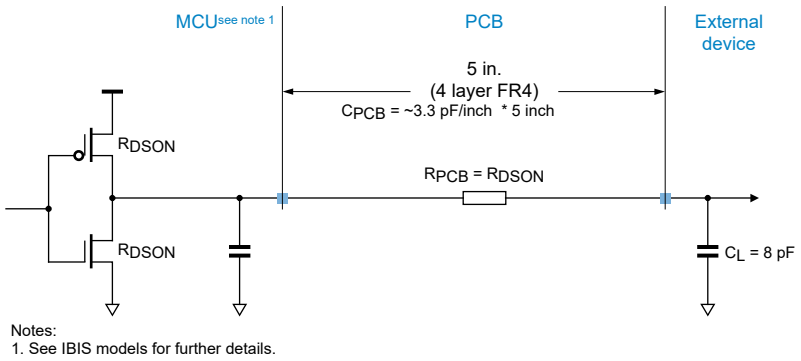


Figure 6. Reference Load Diagram

12 Power Management Controller (PMC)

12.1 PMC Bandgap

Table 15. PMC Bandgap

Symbol	Description	Min	Typ	Max	Unit	Condition
VBG_ADC	Bandgap reference voltage measured by SAR ADC [1]	0.882	0.9	0.918	V	After trimming

[1] ADC conversion error must be included when reading the bandgap reference voltage via the chip ADC.

All bandgap specifications are valid for supply noise less than 50mV pk-pk, 1kHz to 1MHz.

13 Reset

13.1 Reset Duration

The durations specified "Reset Duration" table and the corresponding figures refer to standard reset sequences. A reset sequence is no longer standard when it is interrupted by another power-on or destructive reset event, in which case the reset sequence restarts from the beginning of the reset sequence corresponding to that event, and the total duration is the time already spent in reset plus the duration of the new sequence.

The diagrams in this section are not to scale.

Table 16. Reset Duration

Symbol	Description	Min	Typ	Max	Unit	Condition
TFR	Functional Reset Sequence Duration	—	—	500	us	FIOSC_CLK, trimmed
TDR	Destructive Reset Sequence Duration	—	—	1500	us	FIOSC_CLK, trimmed during destructive reset phase
POR	Power On Reset Sequence Duration	—	—	2500	us	FIOSC_CLK, trimmed during destructive reset phase

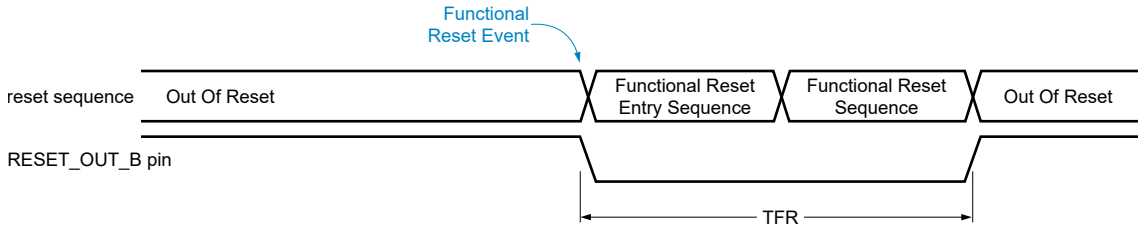


Figure 7. Functional reset

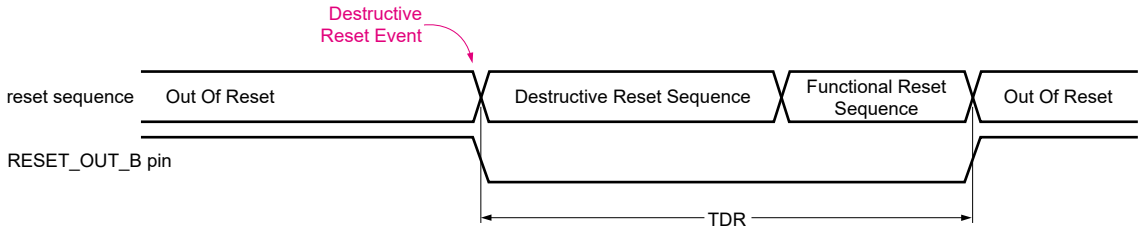


Figure 8. Destructive reset

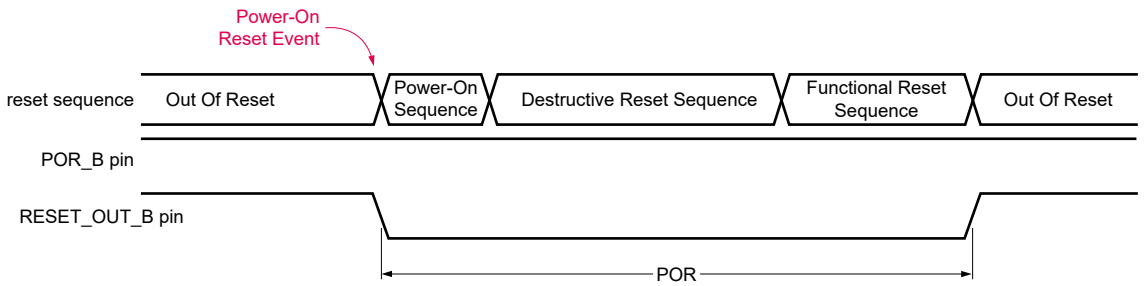


Figure 9. POR due to internal POR event

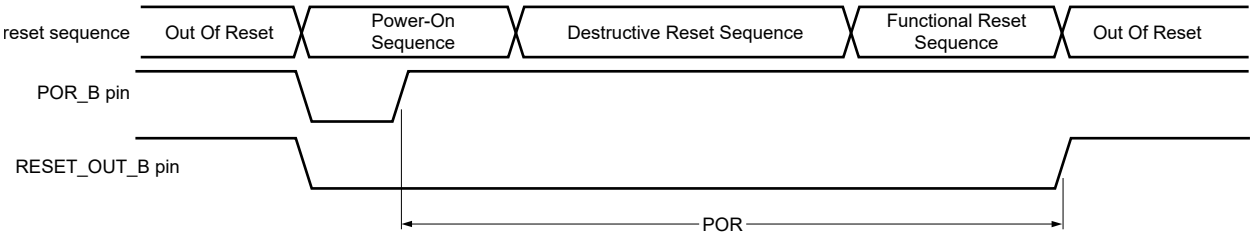


Figure 10. POR due to POR_B pin assertion

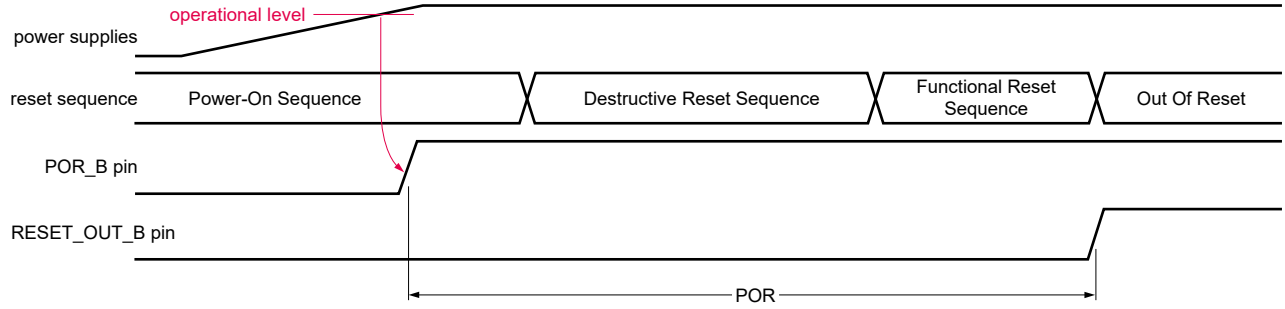


Figure 11. Initial power-up

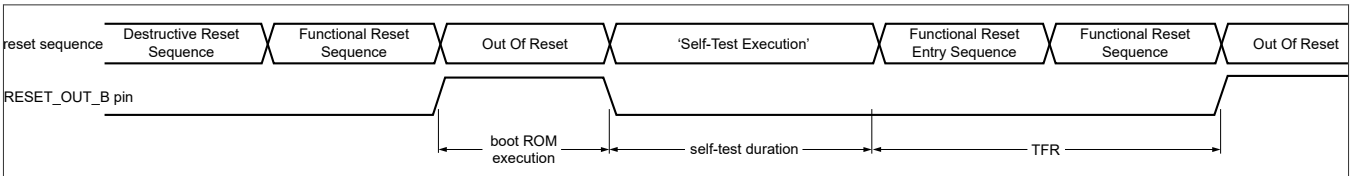


Figure 12. Start-up self-test

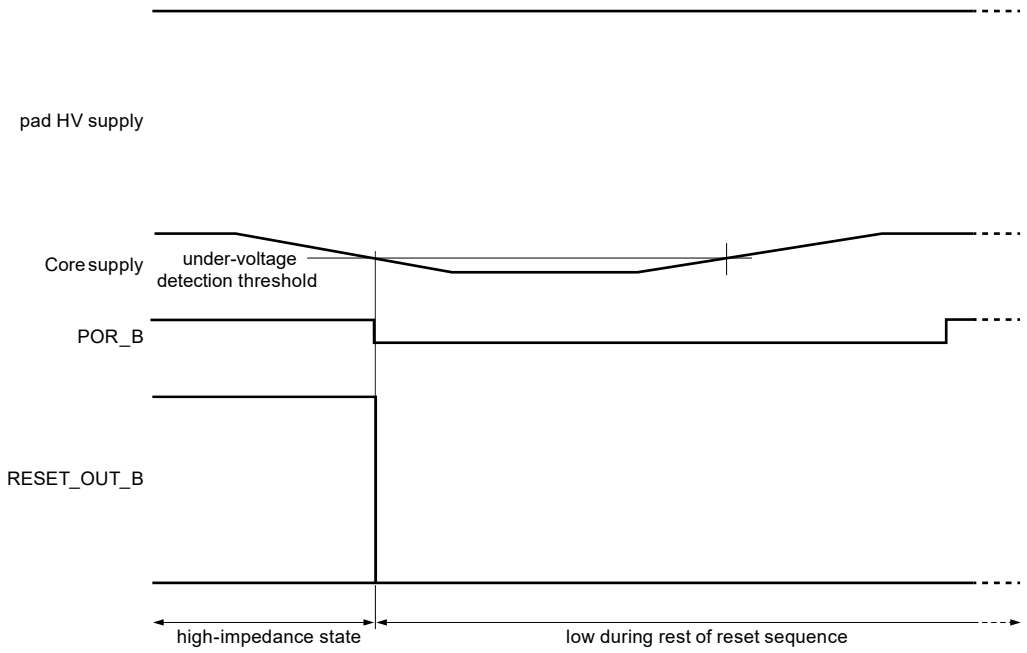


Figure 13. RESET_OUT_B pad detailed behavior during core supply brownout

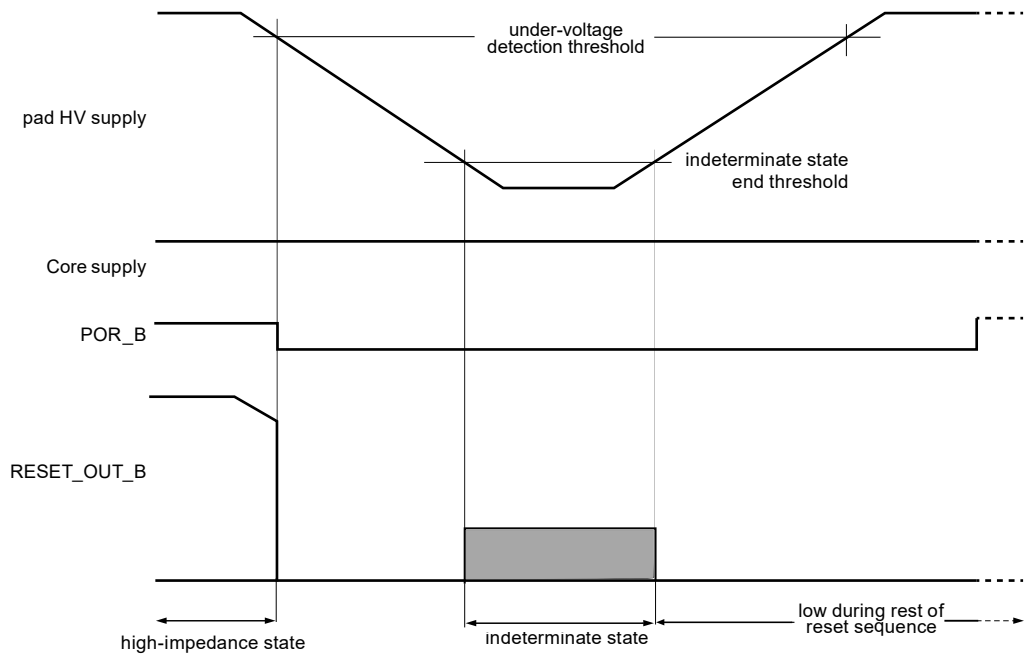


Figure 14. RESET_OUT_B pad detailed behavior during pad HV supply brownout

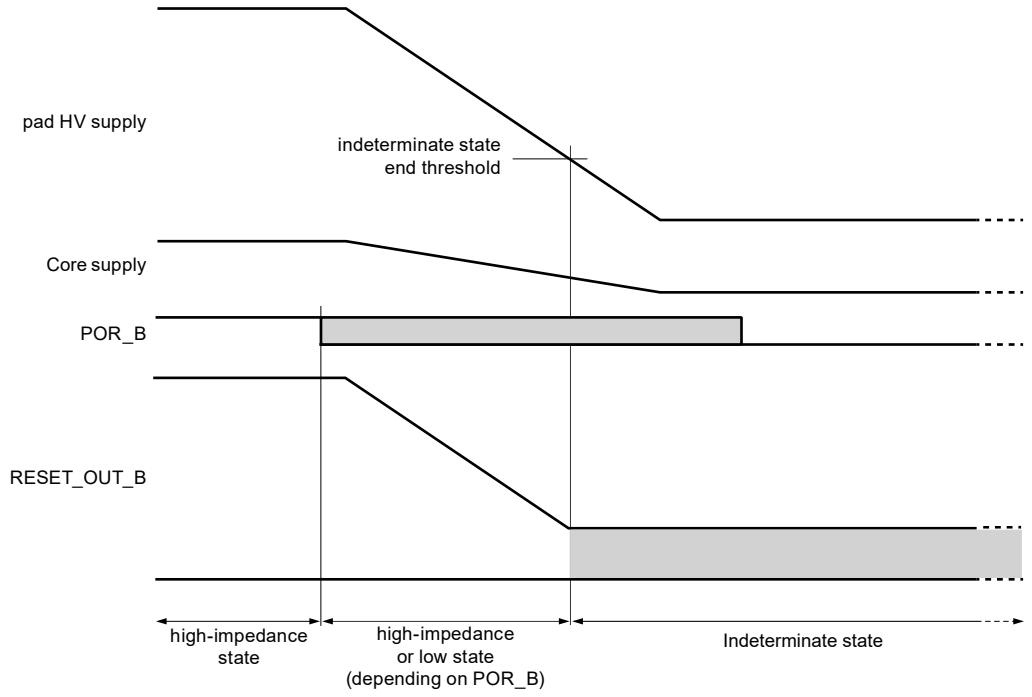


Figure 15. RESET_OUT_B pad detailed behavior during power down

13.2 Reset and Stop / Sleep related pad electrical characteristics

The following table gives the characteristics of the POR_B, RESET_IN_B, RESET_OUT_B, POR_REQ, PMIC_STBY_MODE_B, and PMIC_VDD_OK pads.

Values not explicitly listed in this table can be found in the 'GPIO Pads' section.

Table 17. Reset and Stop / Sleep related pad electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
fPOR_REQ	POR_REQ frequency	12	24	36	kHz	—
dPOR_REQ	POR_REQ duty cycle	45	50	55	%	—
ISLEW_POR_B	POR_B slew rate	1	—	4	V/ns	—
ISLEW_RESET_IN_B	RESET_IN_B slew rate [1]	1	—	4	V/ns	Noise on RESET_IN_B <100mV peak-peak.
VISE_RESET_OUT_B	RESET_OUT_B pad indeterminate state end threshold	—	1.2	—	V	See RESET_OUT_B pad detailed behavior diagram below
WF_RESET_B	RESET_IN_B input filtered pulse	—	—	20	ns	—
WNF_RESET_B	RESET_IN_B input not filtered pulse	400	—	—	ns	—
MLP_POR_B	POR_B minimum low pulse	5	—	—	µs	—
MLP_PMIC_VDD_OK	PMIC_VDD_OK minimum low pulse	36	—	—	µs	during Stop and Sleep mode entry
MHP_PMIC_VDD_OK	PMIC_VDD_OK minimum high pulse	36	—	—	µs	during Stop and Sleep mode entry

[1] ISLEW_RESET_IN_B(Min) = MAX[30e-06, 0.002 * Vnoise_p_p * Fnoise], where Vnoise_p_p is peak-peak noise magnitude (in V) and Fnoise is max noise frequency (in MHz).

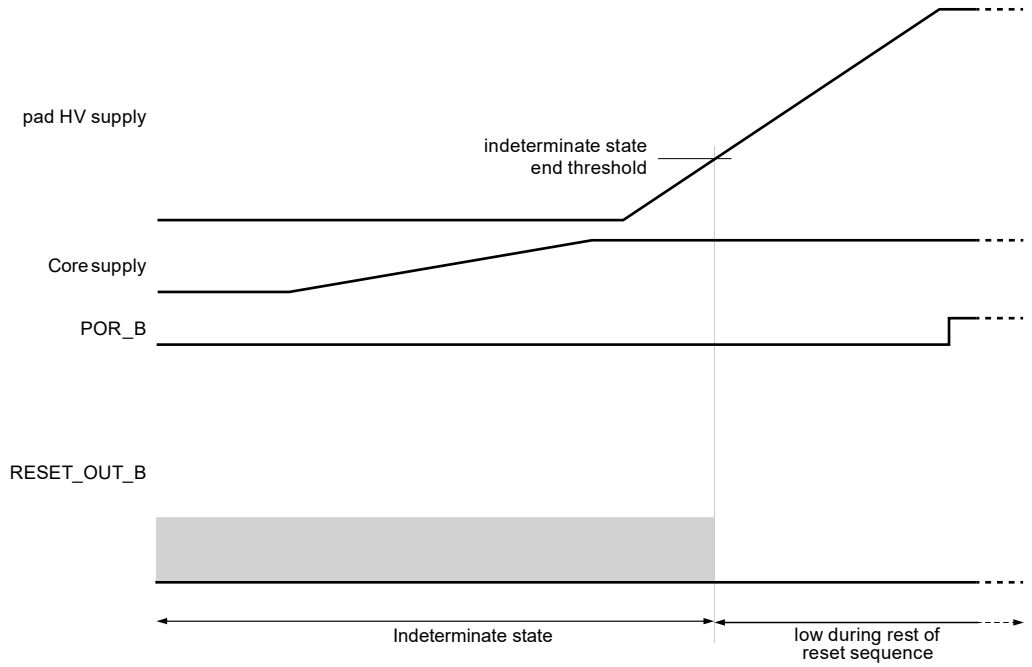


Figure 16. RESET_OUT_B pad detailed behavior during power up

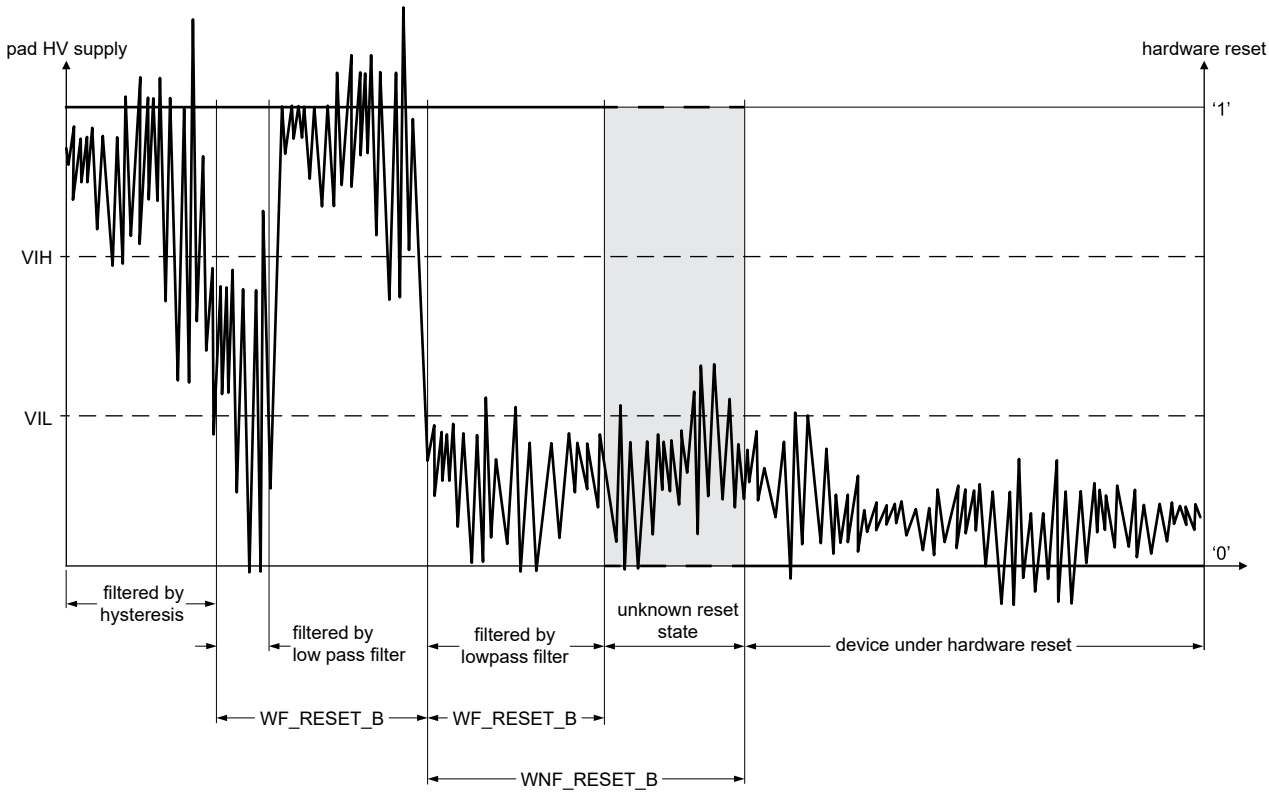


Figure 17. Noise filtering on RESET_IN_B pad

During SoC power-up, the PMIC asserts the POR_B input before the SoC supplies are turned on and kept asserted until all SoC supplies have reached their operational levels (i.e., all the corresponding voltage monitors in the PMIC have been satisfied) and any required PMIC BIST has completed. See the 'Power Sequencing' section for details.

The PMIC asserts the POR_B input whenever one of its voltage detectors detects an SoC supply's voltage is outside its operational range (i.e., a corresponding PMIC LVD or HVD event occurs).

13.3 PMIC Stop and Sleep Mode Entry / Exit Protocol

The PMIC_STBY_MODE_B output is:

1. asserted by the SoC when the power domains that are not needed during Stop / Sleep mode are to be turned off

2. deasserted by the SoC when the power domains that are not needed during Stop / Sleep mode are to be turned on

The PMIC_VDD_OK input is:

1. deasserted by the PMIC when the power domains that are not needed during Stop / Sleep mode have been turned off

2. asserted by the PMIC when the power domains that are not needed during Stop / Sleep mode have been turned on and have reached their operational levels (e.g., all the corresponding voltage monitors in the PMIC have been satisfied) and any required PMIC BIST has completed. See the "Power Sequencing" section for any exceptions.

This implies that the PMIC_VDD_OK input is asserted and deasserted together with the POR_B input during modes other than Stop or Sleep. Deasserting PMIC_VDD_OK during modes other than Stop or Sleep while not also asserting POR_B will cause the SoC to start a power-on reset sequence.

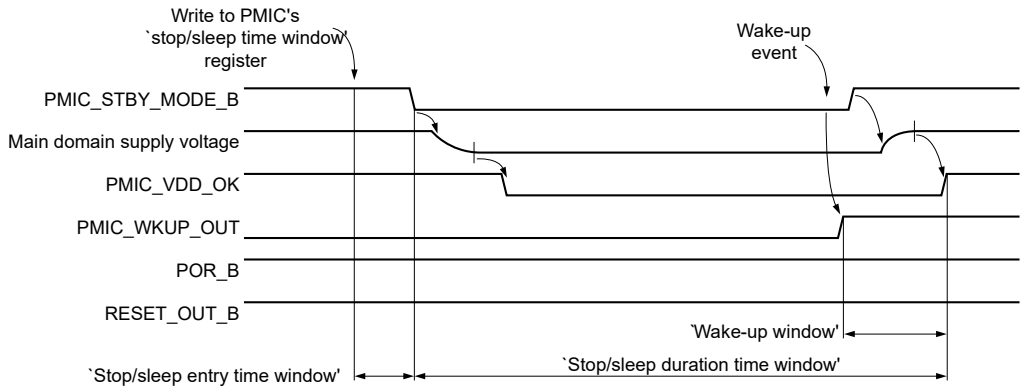


Figure 18. Stop/Sleep Mode Entry and Exit Sequence

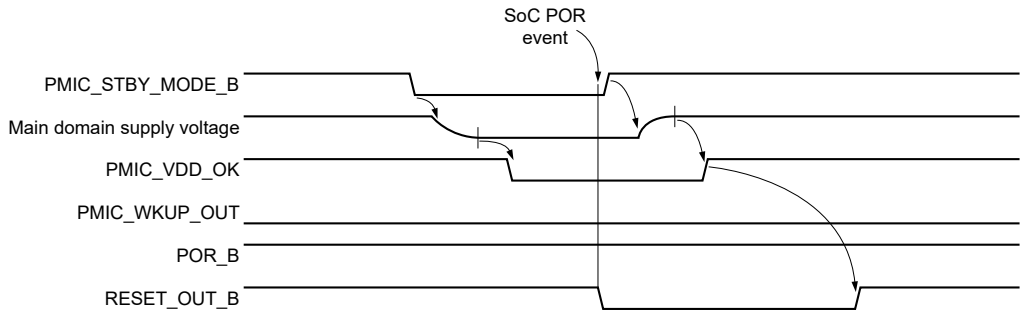


Figure 19. Stop/Sleep Mode Aborted by SoC POR Event Prior to PMIC_VDD_OK Deassertion

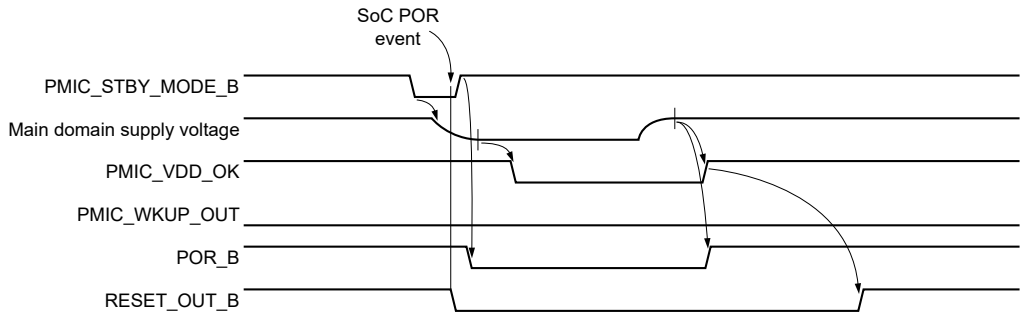


Figure 20. Stop/Sleep Mode Aborted by SoC POR Event After PMIC_VDD_OK Deassertion

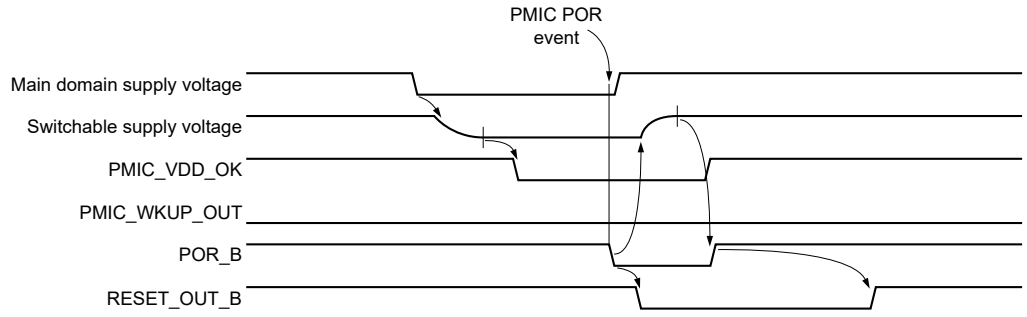


Figure 21. Stop/Sleep Mode Aborted by PMIC POR Event

14 Peripheral specifications

14.1 Analog Modules

14.1.1 SAR ADC

ADC performance specifications are only guaranteed when the injection current limits in the operating conditions table of this electrical specification are met.

Table 18. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition
VAD_INPUT	ADC Input Voltage [1]	VREFL_ ADC	—	VREFH_ ADC	V	on or off channels
fAD_CLK	ADC Clock Frequency	20	—	80	MHz	—
tSAMPLE	Input Sampling Time [2]	275	—	—	ns	—
tSAMPLE_C	SAR selftest C-algorithm sample time	300	—	—	ns	—
tSAMPLE_S	SAR selftest S-algorithm sample time	2	—	—	us	—
tSAMPLE_INT_CH	ADC sample time when converting internal channels using normal conversion modes	625	—	—	ns	—
tCONV	Total Conversion Time [3]	1	—	—	us	—
CAD_INPUT	Total Input Capacitance	—	—	7	pF	ADC component plus pad capacitance (~2pF)
RAD_INPUT	Input Series Resistance	—	—	1.25	kΩ	—
OFS	Offset Error [4]	-6	—	6	LSB	after calibration
GNE	Gain Error (full scale) [4]	-6	—	6	LSB	after calibration
DNL	Differential Non-linearity [4][5][6]	-1	—	2	LSB	after calibration
INL	Integral Non-linearity [4][5]	-3	—	3	LSB	after calibration

Table continues on the next page...

Table 18. SAR ADC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
TUE	Total Unadjusted Error [4][5]	-8	—	8	LSB	after calibration
SNR	Signal-to-Noise Ratio [4][7]	—	65	—	dBFS	after calibration input signal frequency <= 50kHz
THD	Total Harmonic Distortion [4][7]	—	72	—	dBFS	after calibration input signal frequency <= 50kHz
IAD_LKG	Input Leakage Current [8]	-1	—	1	uA	TJ = 125C, Dedicated input channel, channel selection switch open, VREFL_ADC <= VAD_INPUT =< VREFH_ADC + 100mV
IDD_ADC	ADC HV Supply Current Consumption	—	—	1.5	mA	ADC Enabled, @1Msps conversion rate
IDD_ADC	ADC HV Supply Current Consumption	—	—	10	uA	ADC Disabled
IDD_VREF	ADC Reference Current Consumption	—	—	100	uA	ADC Enabled, @1Msps conversion rate
CP1	Input Pin 1 Capacitance	—	2	—	pF	—
CP2	Input Pin 2 Capacitance	—	—	0.5	pF	—
CS	Input Sampling Capacitance	—	—	4	pF	—
RSW1	Internal Analog Source Resistance	—	—	700	Ω	—
RAD	Internal Analog Source Resistance	—	—	3000	Ω	—

[1] The reduced limits for VAD_INPUT in this table are recommended for normal operation
[2] During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within tSAMPLE.. After the end of the sample time tSAMPLE, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock tSAMPLE depend on programming.
[3] 1Msps is the ADC output rate and includes both sampling and analog to digital conversion.
[4] ADC performance specifications are guaranteed when calibration uses maximum averaging i.e. when AVGEN = 1 and NRSMPL = 3.
[5] This specification is taken with averaging through post process ADC data.
[6] During calibration, the ADC determines its (positive or negative) offset value and stores the result in an internal register. During each conversion, the offset value is subtracted from the raw result to compensate the individual ADC offset. Since the ADC cannot generate negative numbers, a negative calibration offset results in a minimum output code between 0 and 6. A positive calibration offset does not impact the max. code output of 4095. Calibration fails if it determines an offset larger than +/- 6 LSB.
[7] SNR and THD specification is not applicable with safe clock as ADC clock source i.e. FIOSC.
[8] The maximum and minimum leakage current values are reached when Vin=VREF and Vin=0, respectively.

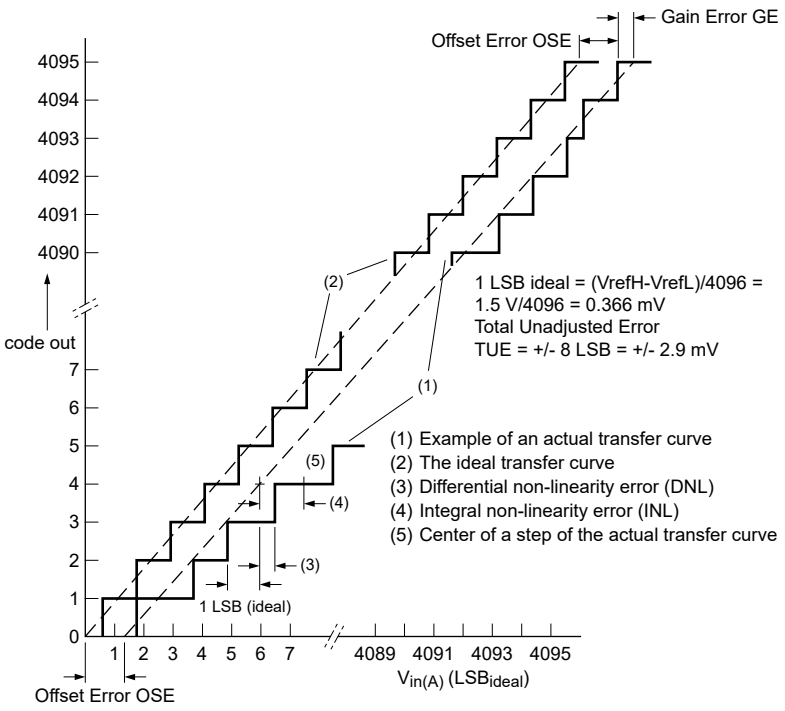


Figure 22. SAR ADC Specification Characteristics

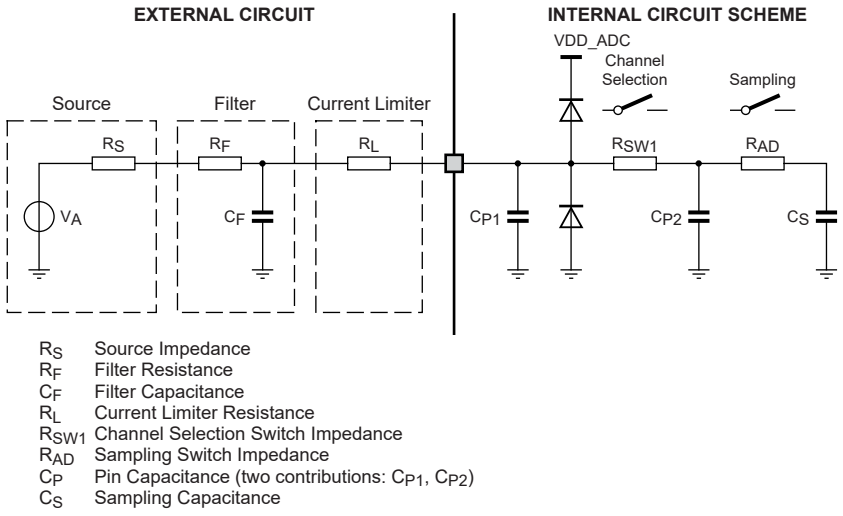


Figure 23. SAR ADC Input Circuit

14.1.2 Temperature Sensor

The table below gives the specification for the on-chip temperature sensors.

Table 19. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition
TRANGE	Temperature monitoring range	-40	—	125	C	—

Table continues on the next page...

Table 19. Temperature Sensor...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
T_ERR	Temperature sensor error	-2	—	2	C	TRANGE = 100C to 125C
T_ERR	Temperature sensor error	-3.6	—	3.6	C	TRANGE = -40C to 99C

14.1.3 IRQ

The following table gives the input specifications for external interrupts.

Table 20. IRQ

Symbol	Description	Min	Typ	Max	Unit	Condition
tIPWL	IRQ pulse width low	100	—	—	ns	—
tIPWH	IRQ pulse width high	100	—	—	ns	—

Few of the IOs support lower value, contact NXP sales representative for more details.

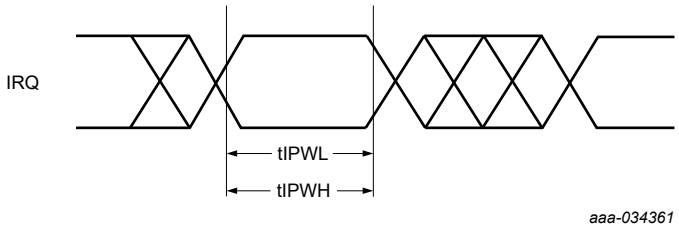


Figure 24. External Interrupt Timing (IRQ)

14.2 Clock and PLL Interfaces

14.2.1 FIOSC

Table 21. FIOSC

Symbol	Description	Min	Typ	Max	Unit	Condition
fFIOSC	FIOSC Trimmed Target Frequency	—	300	—	MHz	—
ðfVAR	FIOSC Frequency Variation [1]	-5	—	5	%	Frequency variation across voltage and temperature range (trimmed oscillator)
TSTART	FIOSC Startup Time	—	—	39	us	Startup time is defined as time from FIOSC IP enable to valid output clock (+/-5% of trimmed output clock frequency). It is assumed that valid supply levels have been reached.

[1] ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device.

14.2.2 SIOSC

Table 22. SIOSC

Symbol	Description	Min	Typ	Max	Unit	Condition
fSIOSC	SIOSC Target Frequency Trimmed	—	32.768	—	kHz	—
ðfVAR	SIOSC Frequency Variation [1]	-10	—	10	%	Frequency variation across voltage and temperature range (trimmed oscillator)
TSTART	Clock startup time	—	—	500	us	—

[1] ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device.

14.2.3 FXOSC

Table 23. FXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition
fXTAL	Input Frequency Range [1]	—	40	—	MHz	Crystal mode
TCST	Crystal Startup Time [2]	—	—	2	ms	Crystal mode - time from supplies valid to output clock stable.
fBYP_SE	FXOSC Bypass Frequency [3]	—	40	—	MHz	Single-ended input clock.
fBYP_DIFF	FXOSC Bypass Frequency [3]	—	40	—	MHz	Differential input clock.
VIH_EXTAL	EXTAL Input High Level [4]	Vref + 0.3	—	VDDA_1P5_FSS_FOSC	V	Vref = VDDA_1P5_FSS_FOSC / 2, Single-ended bypass mode
VIL_EXTAL	EXTAL Input Low Level [4]	0	—	Vref - 0.3	V	Vref = VDDA_1P5_FSS_FOSC / 2, Single-ended bypass mode
ΔfXTAL_CLK	Output Clock Duty Cycle	40	—	60	%	Crystal mode.
ΔfXTAL_CLK_BYP	Output Clock Duty Cycle	40	—	60	%	Bypass mode
ΔfXTAL_CLK_BYP	Input Clock Duty Cycle	47.5	—	52.5	%	Bypass mode
CLOAD	XTAL / EXTAL pin load capacitance [5]	—	8	—	pF	Crystal mode.
CS_XTAL	XTAL / EXTAL pin on-chip stray capacitance [5]	—	—	3	pF	—
VDIFFLVDS	Differential bypass mode voltage swing	350	—	1100	mV	Differential bypass mode.

Table continues on the next page...

Table 23. FXOSC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
CAC_DIFF	Differential bypass mode external AC coupling capacitance	—	2200	—	pF	Differential bypass mode.
RTERM_DIFF	Differential bypass mode external termination resistance	95	100	105	Ω	Differential bypass mode.
I_INJ	EXTAL injection current	-100	—	100	nA	Mean current flowing into EXTAL in crystal mode
I_LKG	External leakage on EXTAL pin	-50	—	50	nA	Bypass mode, 0.5 V.
EXTAL_AMP	EXTAL amplitude (pk-pk)	300	—	1100	mV	Crystal mode
VCM_SE	Common mode voltage for single ended bypass	—	VDDA_1P5_FSS_FOSC/2	—	mV	—

[1] All specifications only valid for this frequency range if the correct FXOSC transconductance setting is used. Please see the device reference manual for the correct setting per the crystal type.
[2] When FXOSC is in Crystal mode with Inverter Comparator ON, set CTRL0[PROG_HYST_EN]=0.
[3] The input clock must be 40 MHz nominal frequency.
[4] The input clock signal should be symmetric around common mode voltage. V common_mode= (VDDA_1P5_FSS_FOSC)/2
[5] Account for on-chip stray capacitance (CS_XTAL) and PCB capacitance in the total XTAL/EXTAL pin load capacitance. CS_XTAL don't include miller capacitance.

See Hardware design guide for recommended circuits for each mode.

In crystal mode, NX3225GA crystal at 40 MHz (ALC enable) has a load cap of 8 pF and configure gm_sel[3:0]=4'b1010.

External 100pF AC coupling capacitor can be used to account for common-mode voltage mismatch with the driver.

Duty cycle of the FXOSC clock when output on either the single-ended or LVDS CLKOUT pins is given in the I/O pad specifications.

RGMII specifications require clock source to have tolerance of +/- 50ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

PCIe specifications require clock source to have tolerance of +/- 300 ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

SGMII specifications require clock source to have tolerance of +/- 100 ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

Inverter comparator is more susceptible to supply noise. Only differential comparator is to be used with the crystal oscillator for Tie jitter spec of 240 ps.

14.2.4 SXOSC

Table 24. SXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition
fSXOSC	Crystal Frequency [1]	—	32.768	—	KHz	Crystal mode
TSTART	Startup Time	—	—	1.5	s	start up time is dependent upon board and crystal model.

[1] Supports single frequency

14.2.5 AVPLL

The following table gives the operating frequencies and characteristics of the PLL. Actual operating frequencies for the device are constrained to the values given below.

Table 25. AVPLL

Symbol	Description	Min	Typ	Max	Unit	Condition
fPLL_CLKIN	PLL Input Clock Frequency	20	—	100	MHz	Before PLL input divider.
fPLL_CLKIN_PFD	PLL Phase Detector Clock Frequency [1]	20	—	40	MHz	After PLL input divider
fPLL_VCO	System PLL VCO Frequency Range [2]	3250	—	6500	MHz	—
tLOCK	System PLL Lock Time	—	—	100	us	From PLL enabled to output clock within specification.
LT_jitter	System PLL Long Term Jitter (BER = 10-12) [3][4]	-150	—	150	ps	ref clock = 40MHz, 6-sigma
ΔfPLL_MOD	Spread Spectrum Clock Modulation Depth [5]	-2	—	+2	PFD clock periods	center spread PFD clock = clock after PLL input divider
ΔfPLL_MOD	Spread Spectrum Clock Modulation Depth	-4	—	—	PFD clock periods	down spread PFD clock = clock after the PLL input divider
fPLL_MOD	Spread Spectrum Clock Modulation Frequency	30	—	64	kHz	fPLL_CLKIN < 40MHz
fPLL_MOD	Spread Spectrum Clock Modulation Frequency	30	—	128	kHz	fPLL_CLKIN = 40MHz
fDFS_CLKOUT	Frac Div Output Clock Frequency Range	12.705	—	3250	MHz	—

[1] This specification is PLL input reference clock frequency after pre-divider.
[2] The frequencies are the nominal frequencies (i.e., what the PLL's VCO is configured to).
[3] Jitter is dependent on supply noise, the period of the PLL output clock, and the division ratio of the clock at the destination module. Specified jitter values are valid for the FXOSC reference clock input only - not valid for FIOSC reference clock input.
[4] This specification is valid when all clock sources are stable.
[5] Use of center-spread clock modulation must not cause a clock to reach a frequency that exceeds the maximum clock frequencies given in the operating conditions table. Only down-spread modulation is supported at the maximum clock frequencies.

Duty cycle of the system PLL clock when output on an external pin is given in the I/O pad specifications.

For chip clocks that are further divided down from the PLL output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the PLL output clock and destination clock periods.

The max frequency in case of center-spread SSCG enabled for a modulation depth can be calculated as: Maxfrequency(with center-spread SSCG disabled) – (Modulation Depth(in %)/(2*100))* Max frequency (with centerspreadSSCG disabled).

14.3 Communication modules

14.3.1 CAN

See GPIO pads for CAN specifications.

14.3.2 UART

See GPIO pads for UART specifications.

14.3.3 SAI Electrical Characteristics, Controller Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns .

Table 26. SAI Electrical Characteristics, Controller Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
S1	SAI_MCLK cycle time	20.345	—	—	ns	—
S2	SAI_MCLK pulse width high/low	45	—	55	%	—
S3	SAI_BCLK cycle time	80	—	—	ns	—
S4	SAI_BCLK pulse width high/low	45	—	55	%	—
S5	SAI_RXD input setup before SAI_BCLK	14	—	—	ns	—
S6	SAI_RXD input hold after SAI_BCLK	0	—	—	ns	—
S7	SAI_BCLK to SAI_TXD output valid	—	—	8	ns	—
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	—	ns	—
S9	SAI_FS input setup before SAI_BCLK	14	—	—	ns	—
S10	SAI_FS input hold after SAI_BCLK	0	—	—	ns	—
S11	SAI_BCLK to SAI_FS output valid	—	—	8	ns	—
S12	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—

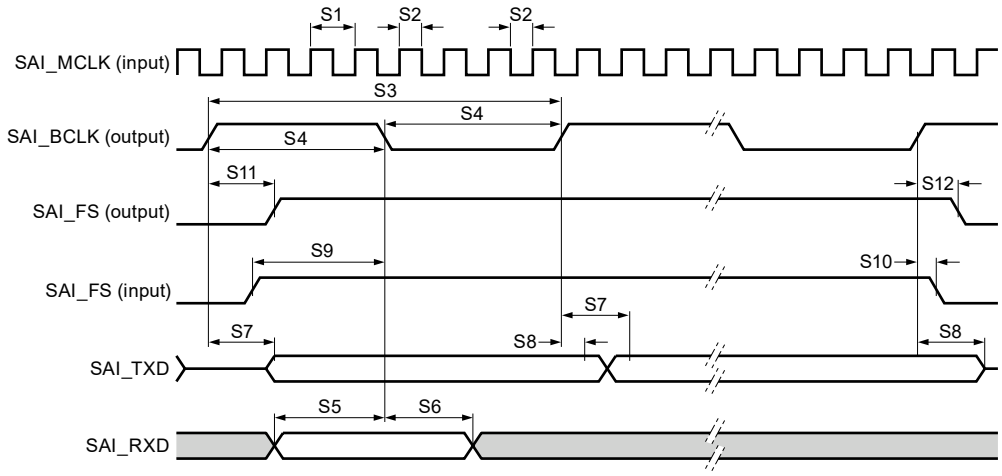


Figure 25. SAI controller mode

14.3.4 SAI Electrical Characteristics, Target Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns.

Table 27. SAI Electrical Characteristics, Target Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
S13	SAI_BCLK cycle time (input)	40.69	—	—	ns	—
S14	SAI_BCLK pulse width high/low (input) [1]	45	—	55	%	—
S15	SAI_RXD input setup before SAI_BCLK	8	—	—	ns	—
S16	SAI_RXD input hold after SAI_BCLK	2	—	—	ns	—
S17	SAI_BCLK to SAI_TXD output valid	—	—	14	ns	—
S18	SAI_BCLK to SAI_TXD output invalid	0	—	—	ns	—
S19	SAI_FS input setup before SAI_BCLK	8	—	—	ns	—
S20	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—
S21	SAI_BCLK to SAI_FS output valid	—	—	14	ns	—
S22	SAI_BCLK to SAI_FS output invalid	0	—	—	ns	—
S23	FX input assertion to TXD output valid [2]	—	—	25	ns	—

[1] The target mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the controller timing.

[2] Applies to the first bit in each frame and only if TCR4[FSE] is clear.

For the case of both controller and target being NXP S32x devices, frequency of operation will be reduced to [1000 /2* {S5 (Controller, SAI_RXD input setup before SAI_BCLK) + S17 (Target, SAI_BCLK to SAI_TXD output valid) + PCB delay}] in ns.

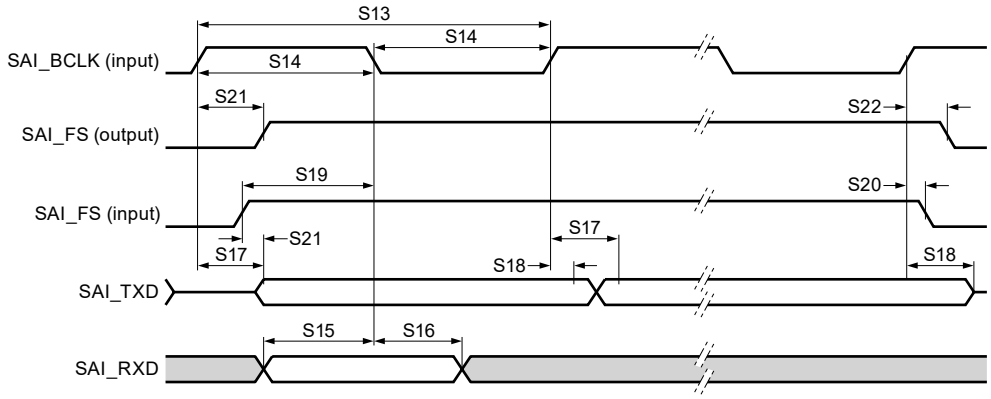


Figure 26. SAI target mode

14.3.5 SENT

Table 28. SENT

Symbol	Description	Min	Typ	Max	Unit	Condition
tFALL	Maximum SENT input signal fall time transition [1][2][3][4]	—	—	2.17	UI	SAE J2716 SENT standard complied with in the application, SAE J2716 recommended RC input filter used in the application

[1] By ensuring that the input fall transition is within the specification, SENT calibration and data bit errors are guaranteed not to occur as a result of variation in the input switching threshold level of the SENT input pin on the device. Switching threshold level variation is due to input signal noise, supply noise, and temperature drift.
[2] This value is the ratio of the maximum 6.5uS fall time and minimum 3uS clock (UI), and assumes the transmit, clock, and measurement error tolerances as defined by the SAE 2716 SENT standard.
[3] Input hysteresis enabled on I/O pads with selectable enable/disable (per the SAE 2716 SENT standard). Does not apply to pads without hysteresis control. In this case, the SENT module glitch filter should be used to reject false transitions. SRX programmable filter should be set to a value closest to 1/10th of a bit time where the max value of 128 is sufficient for long bit times.
[4] SENT inputs are supported at 1.8V on the device, with assumption that the input levels scale linearly for the recommended 1.8V circuit in the SAE 2716 SENT standard. The device does not support 5V SENT inputs.

14.3.6 SPI

Table 29. SPI

Symbol	Description	Min	Typ	Max	Unit	Condition
tSCK	SPI cycle time [1][2]	40	—	10000	ns	Controller, MTFE=0
tSCK	SPI cycle time [2]	25	—	10000	ns	Controller, MTFE=1
tSCK	SPI cycle time [2][3]	16.67	—	10000	ns	Peripheral Receive Mode
tSCK	SPI cycle time [2]	40	—	10000	ns	Peripheral Transmit Mode

Table continues on the next page...

Table 29. SPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tCSC	PCS to SCK delay [4]	20	—	10000	ns	—
tASC	After SCK delay [5]	20	—	10000	ns	—
tSDC	SCK duty cycle	40	—	60	%	—
tA	Peripheral access time	—	—	40	ns	SS active to SOUT valid
tDIS	Peripheral SOUT disable time	—	—	15	ns	SS inactive to SOUT hi-z or invalid
tPCSC	PCSx to PCSS time	13	—	—	ns	—
tPASC	PCSS to PCSx time	13	—	—	ns	—
tSUI	Input data setup time [6][7]	15	—	—	ns	Controller, MTFE=0
tSUI	Input data setup time [7][8]	15 - N * ipg_clk_dspi_period	—	—	ns	Controller, MTFE=1, CPHA=0, SMPL_PTR = 1
tSUI	Input data setup time [7]	15	—	—	ns	Controller, MTFE=1, CPHA=1, SMPL_PTR = 1
tSUI	Input data setup time [7]	2	—	—	ns	Peripheral Receive Mode
tHI	Input data hold time [7]	0	—	—	ns	Controller, MTFE=0
tHI	Input data hold time [7]	0 + N * ipg_clk_dspi_period	—	—	ns	Controller, MTFE=1, CPHA=0, SMPL_PTR = 1
tHI	Input data hold time [7]	0	—	—	ns	Controller, MTFE=1, CPHA=1, SMPL_PTR = 1
tHI	Input data hold time [7]	4	—	—	ns	Peripheral Receive Mode
tSUO	Output data valid time (after SCK edge) [9]	—	—	5	ns	Controller, MTFE=0 max CLOAD=25pF, max pad drive setting
tSUO	Output data valid time (after SCK edge) [9]	—	—	5 + ipg_clk_dspi_period	ns	Controller, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting
tSUO	Output data valid time (after SCK edge) [9]	—	—	5	ns	Controller, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting

Table continues on the next page...

Table 29. SPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tSUO	Output data valid time (after SCK edge) [6][9]	—	—	16	ns	Peripheral Transmit Mode
tHO	Output data hold time [9]	-2	—	—	ns	Controller, MTFE=0 max CLOAD=25pF, max pad drive setting
tHO	Output data hold time [9]	-2 + ipg_clk_dspi_period	—	—	ns	Controller, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting
tHO	Output data hold time [9]	-2	—	—	ns	Controller, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting
tHO	Output data hold time [9]	2.68	—	—	ns	Peripheral transmit mode

[1] SMPL_PTR should be set to 1. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 3
[2] The maximum SPI baud rate that is achievable in a dedicated controller-peripheral connection depends on several parameters that are independent of the SPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI peripheral clock-to-data delay, pad slew rate, etc.). The maximum achievable SPI baud rate needs to be evaluated in a corresponding SPI controller-peripheral setup.
[3] Peripheral Receive Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.
[4] This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h)
[5] This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h)
[6] For the case of both controller and peripheral being NXP S32x devices, maximum frequency of operation during Peripheral transmit mode will be Fmax= 1/[2* {tSUI_controller + tSUO_peripheral + PCB delay}]. For non-NXP devices, max frequency of operation needs to be calculated based on AC specifications of interfacing devices.
[7] Input timing assumes an input signal slew rate of 2ns (20%/80%).
[8] N is number of protocol clock cycles where the controller samples SIN in MTFE mode after SCK edge.
[9] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

Peripheral mode timing values given below are applicable when device is in MTFE=0.

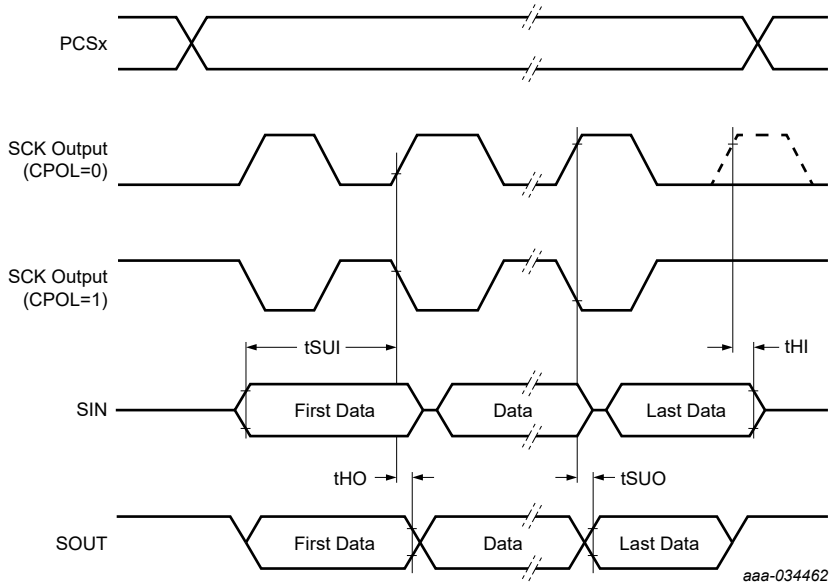


Figure 27. SPI Modified Transfer Format Timing - Controller, CPHA = 1, MTFE=1

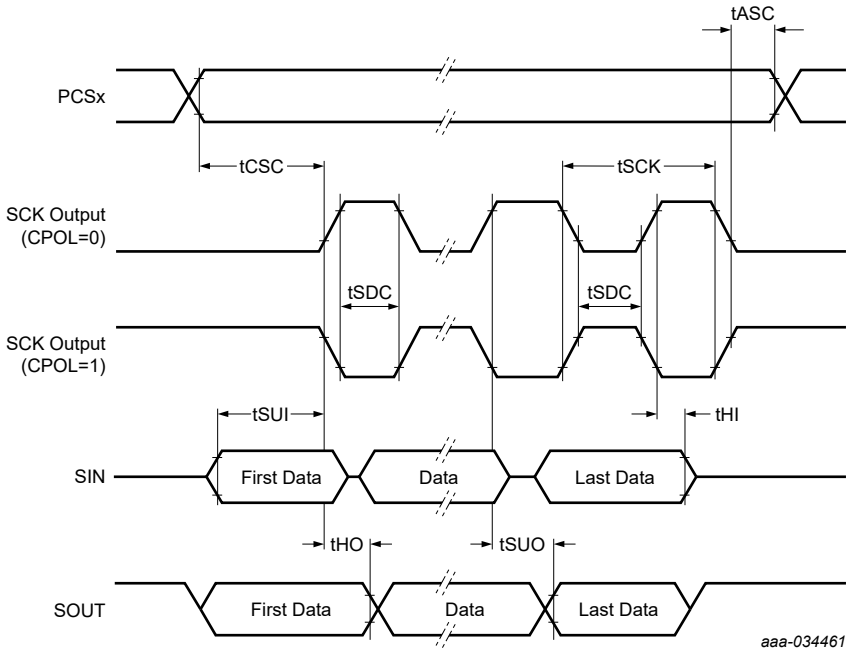


Figure 28. SPI Modified Transfer Format Timing - Controller, CPHA = 0, MTFE=1

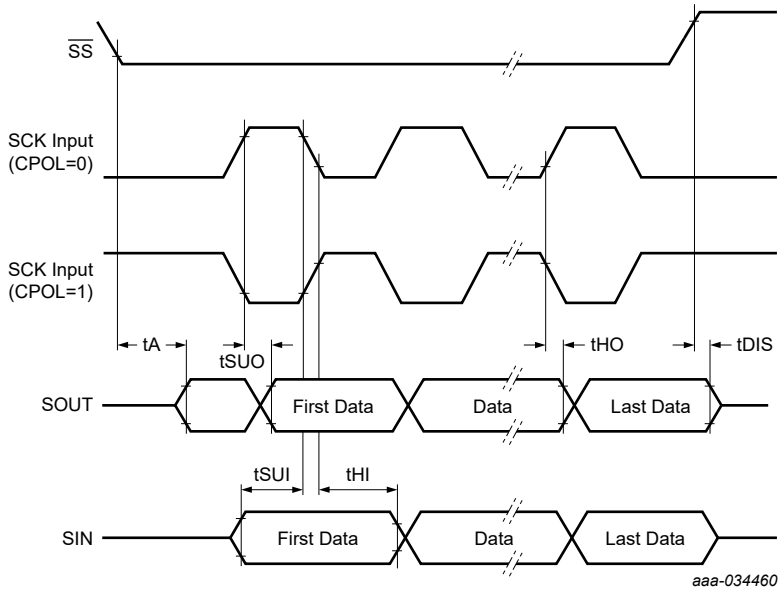


Figure 29. SPI Classic Timing - Peripheral CPHA = 1, MTFE=0

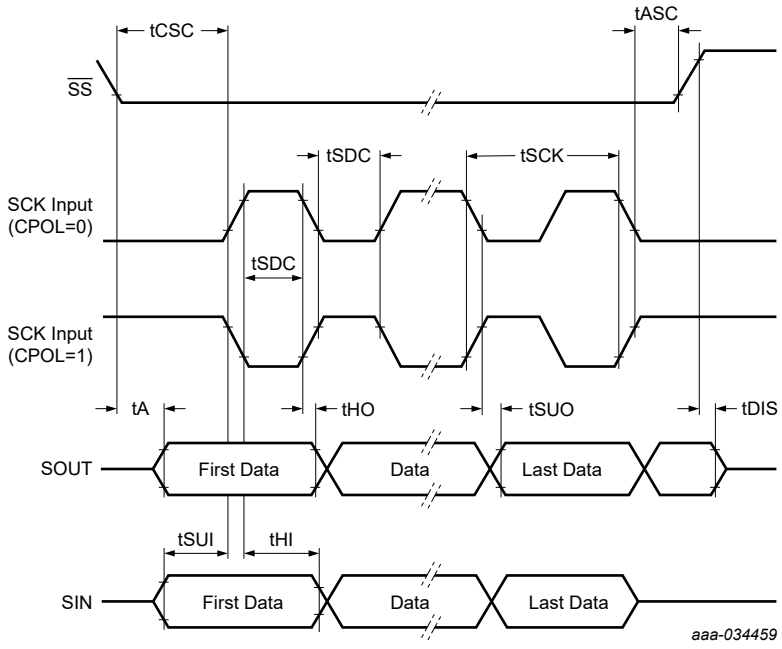


Figure 30. SPI Classic Timing - Peripheral CPHA = 0, MTFE=0

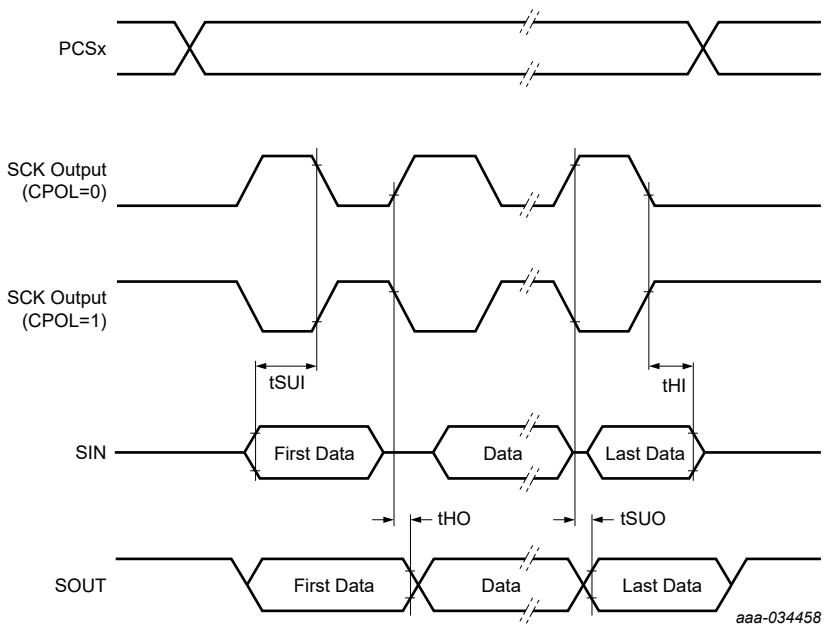


Figure 31. SPI Classic Timing - Controller, CPHA = 1, MTFE=0

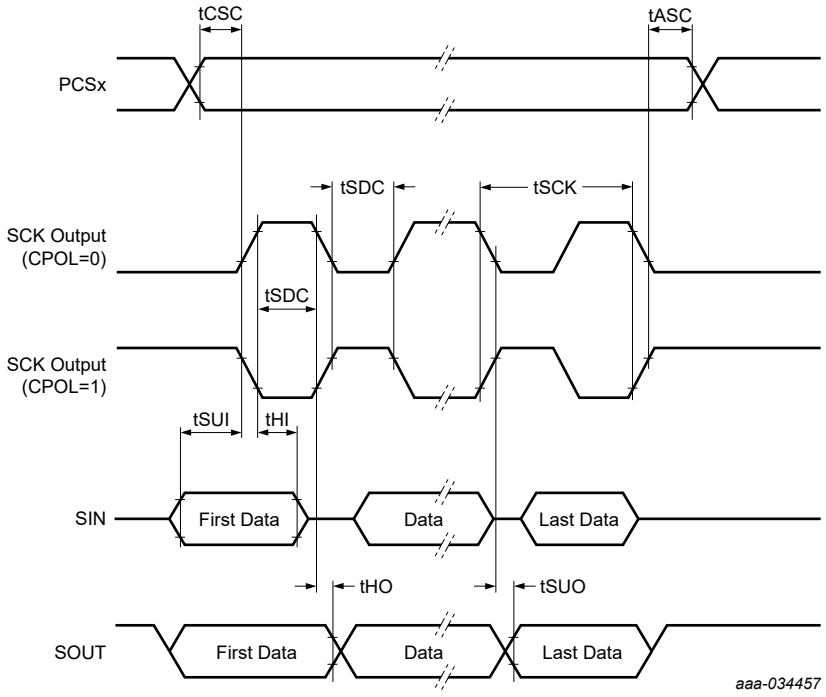


Figure 32. SPI Classic Timing - Controller, CPHA = 0, MTFE=0

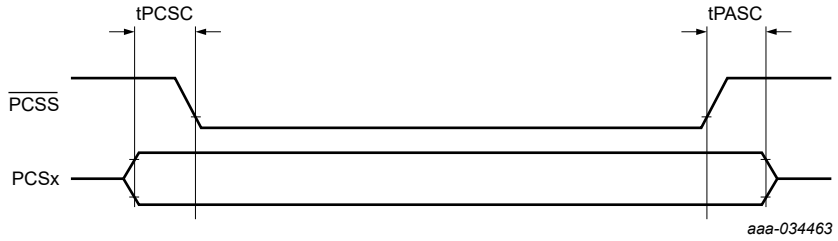


Figure 33. SPI PCS Strobe (PCSS) Timing

14.3.7 CANXL

Table 30. CANXL

Symbol	Description	Min	Typ	Max	Unit	Condition
tSymbolNom	CANXL PWM symbol length (PWMS + PWML)	50	—	200	ns	PWM Data rate= 5Mbps to 20Mbps
PWMS	PWM symbol period short phase [1]	5	—	0.5 *tSymbol Nom - 5	ns	50% VDD_IO
PWML	PWM symbol period long phase	tSymbol Nom - max(PWMS)	—	tSymbol Nom - min(PWMS)	ns	50% VDD_IO

[1] To guarantee a minimum of 5ns decode time at the transceiver, the CANXL internal PWM must be programmed to ensure 10ns <= PWMS <= 0.5 * tSymbolNom – 10ns.

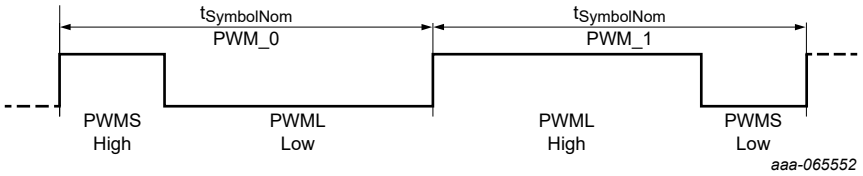


Figure 34. CANXL timing

14.3.8 I2C

14.3.8.1 I2C Input

Table 31. I2C Input

Symbol	Description	Min	Typ	Max	Unit	Condition
tIH_SC	Input Start condition hold time [1] [2]	2	—	—	MODULE_CLK cycle	—
tCL	Input Clock low time [1][2]	8	—	—	MODULE_CLK cycle	—

Table continues on the next page...

Table 31. I2C Input...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tIH	Input Data hold time [1][2]	0	—	—	ns	SDA transitions after SCL falling edge
tCH	Input Clock high time [1][2]	4	—	—	MODULE_CLK cycle	—
tISU	Input Data setup time (standard mode) [1][2][3]	250	—	—	ns	SDA transitions before SCL rising edge

[1] MODULE_CLK from the MC_CGM is the clock driving the I2C block.
[2] Input timing assumes an input signal slew rate of 3ns (20%/80%).
[3] MODULE_CLK frequency should be greater than 5 MHz for standard mode and 20 MHz for fast mode.

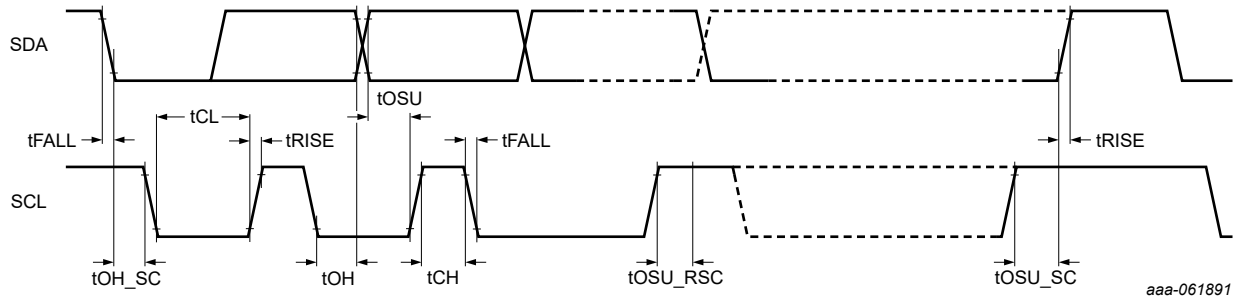


Figure 35. I2C Input/Output Timing

14.3.8.2 I2C Output

Programming IBFD (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBFD.

Table 32. I2C Output

Symbol	Description	Min	Typ	Max	Unit	Condition
tOH_SC	Output Start condition hold time [1][2]	6	—	—	MODULE_CLK cycle	—
tCL	Output Clock low time [1][2]	10	—	—	MODULE_CLK cycle	—
tRISE	SDA/SCL rise time [1][2][3]	—	—	100	ns	—
tOH	Output Data hold time [1][2]	7	—	—	MODULE_CLK cycle	—
tFALL	SDA/SCL fall time [1][2][3]	—	—	100	ns	—
tCH	Output Clock high time [1][2]	10	—	—	MODULE_CLK cycle	—

Table continues on the next page...

Table 32. I2C Output...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tOSU	Output Data setup time [1][2]	2	—	—	MODULE_CLK cycle	—
tOSU_RSC	Output repeated start condition setup time [1][2]	20	—	—	MODULE_CLK cycle	—
tOSU_SC	Output start condition setup time [1][2]	11	—	—	MODULE_CLK cycle	—

[1] MODULE_CLK from the MC_CGM is the clock driving the I2C block.
[2] Timing valid for maximum external load CL = 400pF, at the maximum clock frequency defined by the I2C clock high and low time specifications.
[3] Because SCL and SDA are open-drain outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values

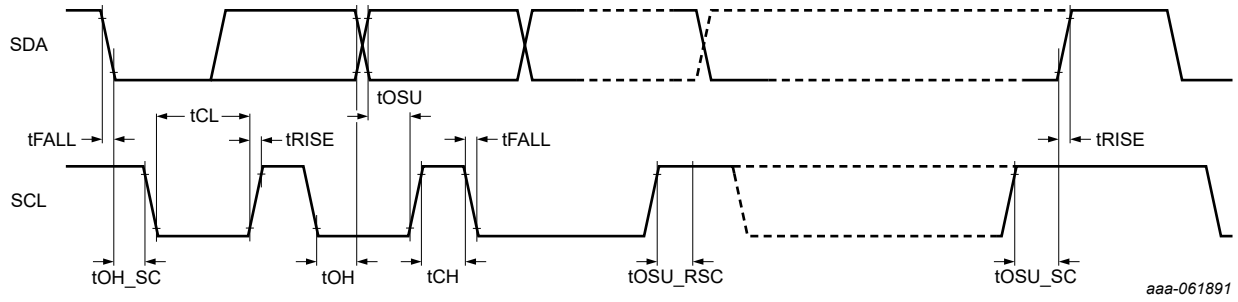


Figure 36. I2C Input/Output Timing

14.3.9 LIN

Table 33. LIN

Symbol	Description	Min	Typ	Max	Unit	Condition
RATE	Bit Rate	—	—	2.0	Mbps	UART mode
RATE	Bit Rate	4.8	—	20	Kbps	LIN mode

14.3.10 PSI5

Table 34. PSI5

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	—	3	us	—
—	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	—	2	us	—

Table continues on the next page...

Table 34. PSI5...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt [1]	—	—	1	cycles	—
—	Delay jitter from internal sync pulse to sync pulsetrigger at the SDOUT_PSI5_n pin. [2]	—	—	+/- (PSI5_1us_CLK + COSS_PERIPH_CLK)	cycles	—
DC	Duty Cycle [3]	35	—	65	%	—

[1] Measured in PSI5 clock cycles. Minimum PSI5 clock period is 20ns.
[2] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] PSI5 sensor input signals must meet the duty cycle requirement in order to be decoded properly.

14.3.11 SerDes

The PCI Express link conforms to the PCI Express Base Specification Gen 4. Consult the Base Specification for all the specs.

14.3.11.1 PCIe

PCIe Electricals are compatible with the PCI e Base Specification Rev 4.0, Version 1.0, Section 8 and Errata for the PCI Express Base Specification Rev. 4.0, Version 2.0

Table 35. PCIe

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval	399.88	—	400.12	ps	2.5 GT/s
UI	Unit Interval	199.94	—	200.06	ps	5 GT/s
UI	Unit Interval	124.9625	—	125.0375	ps	8 GT/s
UI	Unit Interval	62.48125	—	62.51875	ps	16 GT/s
CTX	AC Coupling Capacitor	176	—	265	nF	—
REXT	External Calibration Resistor [1]	—	649	—	Ohms	—

[1] REXT requires better than or equal to 1% precision connected to VSS.

14.3.11.1.1 PCIe Transmitter DC Specifications

Table 36. PCIe Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	—	1200	mVPP	2.5GT/s, 5.0GT/s
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	—	1300	mVPP	8.0GT/s, 16GT/s

Table continues on the next page...

Table 36. PCIe Transmitter DC Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400	—	1200	mVPP	2.5GT/s, 5GT/s
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400	—	1300	mVPP	8GT/s, 16GT/s

Vdiffpk-pk for full swing operation is configured according to 1.13*VDD15PHY*[Z0/(Ztx+Z0)] where Ztx = 60ohms and Z0 = 100ohms

Vdiffpk-pk for low swing operation is configured according to 0.70*1.13*VDD15PHY*[Z0/(Ztx+Z0)] where Ztx = 60ohms and Z0 = 100ohms

14.3.11.1.2 PCIE Transmitter AC Specifications

Table 37. PCIE Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
BWTX-PKG-PLL	Typical TX PLL Bandwidth	—	11	—	MHz	2.5GT/s
PKGTX-PLL	Typical TX PLL Peaking	—	0.25	—	dB	2.5GT/s
BWTX-PKG-PLL	Typical TX PLL Bandwidth	—	9	—	MHz	5GT/s
PKGTX-PLL	Typical TX PLL Peaking	—	0.26	—	dB	5GT/s
BWTX-PKG-PLL	Typical TX PLL Bandwidth	—	3.5	—	MHz	8GT/s
PKGTX-PLL	Typical TX PLL Peaking	—	0.6	—	dB	8GT/s
BWTX-PKG-PLL	Typical TX PLL Bandwidth	—	3.4	—	MHz	16GT/s
PKGTX-PLL	Typical TX PLL Peaking	—	0.6	—	dB	16GT/s
TTX-UTJ	TX Uncorrelated Total Jitter	—	—	100	ps PP @ 10e-12	2.5GT/s
TTX-UTJ	TX Uncorrelated Total Jitter	—	—	50	ps PP @ 10e-12	5GT/s
TTX-UTJ	TX Uncorrelated Total Jitter	—	—	31.25	ps PP @ 10e-12	8 GT/s
TTX-UTJ	TX Uncorrelated Total Jitter	—	—	12.5	ps PP @ 10e-12	16GT/s
TTX-UTJ-SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	—	—	100	ps PP @ 10e-12	2.5GT/s
TTX-UTJ-SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	—	—	66.51	ps PP @ 10e-12	5GT/s

Table continues on the next page...

Table 37. PCIE Transmitter AC Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
TTX-UTJ-SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	—	—	33.83	ps PP @ 10e-12	8GT/s
TTX-UTJ-SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	—	—	15.85	ps PP @ 10e-12	16GT/s
TTX-UDJDD	Tx uncorrelated Dj for non-embedded Refclk	—	—	100	ps PP	2.5GT/s
TTX-UDJDD	Tx uncorrelated Dj for non-embedded Refclk	—	—	30	ps PP	5GT/s
TTX-UDJDD	Tx uncorrelated Dj for non-embedded Refclk	—	—	12	ps PP	8GT/s
TTX-UDJDD	Tx uncorrelated Dj for non-embedded Refclk	—	—	6.25	ps PP	16GT/s
TTX-UPW-TJ	Total uncorrelated pulse width jitter	—	—	40	ps PP @10^-12	5GT/s
TTX-UPW-TJ	Total uncorrelated pulse width jitter	—	—	24	ps PP @10^-12	8GT/s
TTX-UPW-TJ	Total uncorrelated pulse width jitter	—	—	12.5	ps PP @10^-12	16GT/s
TTX-UPW-DJDD	Deterministic DjDD uncorrelated pulse width jitter	—	—	40	ps PP	5GT/s
TTX-UPW-DJDD	Deterministic DjDD uncorrelated pulse width jitter	—	—	10	ps PP	8GT/s
TTX-UPW-DJDD	Deterministic DjDD uncorrelated pulse width jitter	—	—	5	ps PP	16GT/s

14.3.11.1.3 PCIe Input Reference Clock Specifications

Table 38. PCIe Input Reference Clock Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
F-REFCLK_IN	Reference Clock Frequency	99.97	—	100.03	MHz	—

The differential PCIe reference clock inputs, SD0_REF_CLK_P/_N are designed to be compatible with the PCIe reference clock specifications as defined in in PCI Express® Base Specification Revision 4.0 Version 1.0, Section 8.6. As such the reference clock source must also be compatible with the in PCI Express® Base Specification Revision 4.0 Version 1.0, Section 8.6 and using the voltage levels described below.

The SD0_REF_CLK_P/_N inputs are unterminated as PCIe defines the termination at the system clock driver end. The inputs must be DC coupled at the system level as AC-coupling may violate the CLKREQ# functionality of PCIe. The SD0_REF_CLK_P and SD0_REF_CLK_N inputs should follow the voltage levels as pictured below.

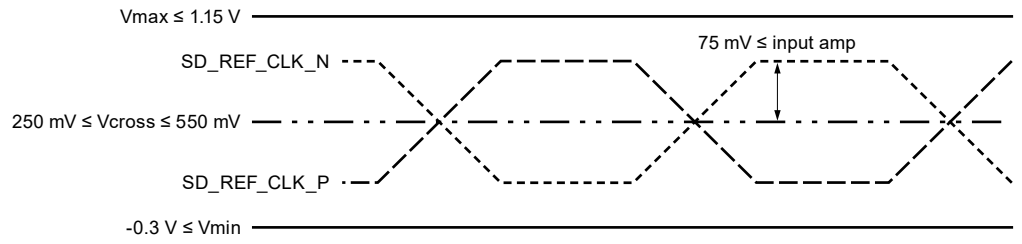


Figure 37. PCIe reference clock input

14.3.11.1.4 PCIe Output Reference Clock Specifications

DUT is configured such that SD_REF_CLK is an output.

The differential PCIe reference clock outputs, SD0_REF_CLK_P/_N are designed to be compatible with the PCIe reference clock specifications as defined in in PCI Express® Base Specification Revision 4.0 Version 1.0, Section 8.6 with Common reference clock jitter measurements performed using the Gen4 CBB/CLB from PCI-SIG. The differential outputs are designed to be compatible with HCSL (Host Controller Signal Level) timing applications. External PCB series or pulldown resistors are unnecessary due to on-die nominal 50ohm driver termination. See below for example application.

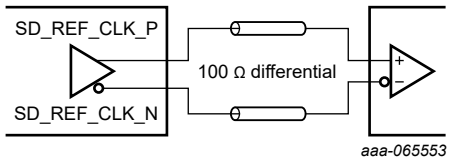


Figure 38. Load termination

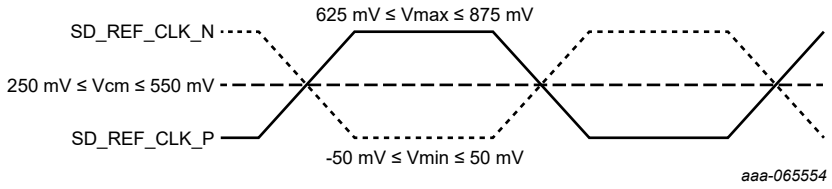


Figure 39. Single-ended output voltage levels as measured with unterminated load

14.3.11.2 SGMII

SGMII electrical specifications will be compatible with the 1000Base-KX electrical specifications based on IEEE802.3 Clause 70.7.

14.3.11.3 1000Base-KX

1000Base-KX Electricals are compatible with Electrical Specifications as defined in IEEE 802.3, Clause 70 and is intended for Backplane Applications

Table 39. 1000Base-KX

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval (mean)	799.92	800	800.08	ps	—
CTX	AC Coupling Capacitor	4.7	—	220	nF	—
REXT	External Calibration Resistor [1]	—	649	—	Ohms	—

[1] REXT requires better than or equal to 1% precision connected to VSS.

14.3.11.3.1 1000Base-KX Transmitter DC Specifications

Table 40. 1000Base-KX Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDIFF_PK-PK	Differential peak-to-peak output voltage	800	—	1600	mV	—

14.3.11.3.2 1000Base-KX Transmitter AC Specifications

Table 41. 1000Base-KX Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Trise_fall_typ	Transition Time (20% - 80%) [1]	—	30	—	ps	Measured on Typical Silicon at Nominal Voltages and Room Temperature
Dj	Deterministic Jitter (Max pk-pk)	—	—	0.1	UI	—
Rj	Random jitter	—	—	0.15	UI	—
Tj	Total jitter (Max pk-pk at BER 1E-12)	—	—	0.25	UI	—
TEYE-X1	TX Eye Mask X1 Time at 0mV Differential Amplitude	—	—	0.125	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12
TEYE-X2	TX Eye Mask X2 Time at +/-A1 Differential Amplitude	—	—	0.325	UI	See Eye Mask Figure at TP1, Specified at BER = 1E-12
TEYE-A2	TX Eye Mask A2 Differential Amplitude overall UI	-800	—	800	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12
TEYE-A1	TX Eye Mask A1 Differential Amplitude at X2 UI	-400	—	400	mV	See Eye Mask Figure at TP1, Specified at BER = 1E-12

[1] Trise_fall is faster than specified.

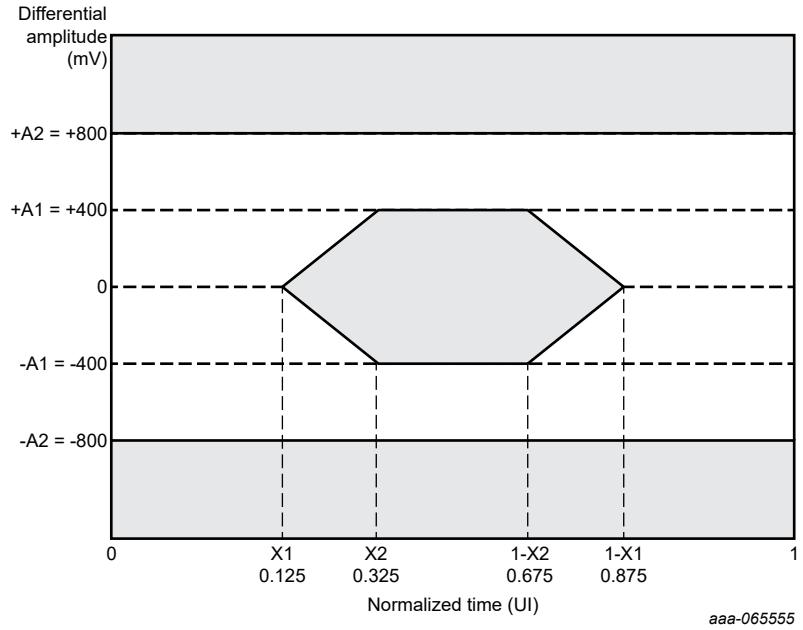


Figure 40. Eye Mask TP1

Table 42. 1000Base-KX Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1600	mV	—

14.3.11.4 2.5G SGMII

2.5GSGMII Electricals are compatible with Electrical Specifications as defined in IEEE 802.3-2018, Clause 47 (XAUI)

Table 43. 2.5G SGMII

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval (mean)	319.968	320	320.032	ps	—
CTX	AC Coupling Capacitor [1]	4.7	—	220	nF	—
REXT	External Calibration Resistor [2] [3]	—	649	—	Ohms	—

[1] If lane is used for multiple Ethernet rates, then capacitor value must be chosen to accomodate highest rate.
[2] REXT requires better than or equal to 1% precision connected to VSS
[3] Vdiffpk-pk for full swing operation is configured according to 1.13*VDD15PHY*[Z0/(Ztx+Z0)] where Ztx = 60ohms and Z0 = 100ohms

14.3.11.4.1 2.5G SGMII Transmitter DC Specifications

Table 44. 2.5G SGMII Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDIFF_PK-PK	Differential peak-to-peak output voltage	—	—	1600	mVp-p	—
DC_CM_Volt	Absolute Output Voltage Limits	-0.4	—	2.3	V	—

14.3.11.4.2 2.5G SGMII Transmitter AC Specifications

Table 45. 2.5G SGMII Transmitter AC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Trise_fall_typ	Transmit Vod transition time (20-80%) [1]	—	30	—	ps	Measured on Typical Silicon at Nominal Voltages and Room Temperature
Dj_NE	Near End Deterministic Jitter	—	—	0.17	UI	Peak to Peak
Tj_NE	Near End Total jitter	—	—	0.35	UI	Peak to Peak
TEYE-A2_NE	Near End TX Eye Mask A2 Differential Amplitude overall UI	-800	—	800	mV	at BER = 1E-12
TEYE-A1_NE	Near End TX Eye Mask A1 Differential Amplitude at X2 UI	-400	—	400	mV	at BER = 1E-12
TEYE-X1_NE	Near End TX Eye Mask X1 jitter at 0 Differential Amplitude	—	—	0.175	UI	measured from 0UI and 1UI cross points at BER = 1E-12
TEYE-X2_NE	Near End TX Eye Mask X2 jitter at A1 Differential Amplitude	—	—	0.390	UI	measured from 0UI and 1UI cross points at BER = 1E-12
TEYE-X1_FE	Far End TX Eye Mask X1 jitter at 0 Differential Amplitude	—	—	0.275	UI	measured from 0UI and 1UI cross points at BER = 1E-12
TEYE-X2_FE	Far End TX Eye Mask X2 jitter at A1 Differential Amplitude	—	—	0.400	UI	measured from 0UI and 1UI cross points at BER = 1E-12

[1] Exception: transition time is faster than recommended

14.3.11.4.3 2.5G SGMII Receiver DC Specifications

Table 46. 2.5G SGMII Receiver DC Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VINdiffpk-pk	Differential Input Pk-Pk amplitude	—	—	1600	mVp-p	—

14.3.11.5 Ethernet Reference Clock Input

DUT is configured such that SD_REF_CLK is an input for use with SGMII, 2.5x SGMII and/or 1000Base-KX Ethernet links

Table 47. Ethernet Reference Clock Input

Symbol	Description	Min	Typ	Max	Unit	Condition
F-REFCLK_IN	Reference Clock Frequency	156.234375	—	156.265625	MHz	—

Table continues on the next page...

Table 47. Ethernet Reference Clock Input...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
DUTY CYCLE_IN	Duty Cycle	40	—	60	%	—
VIH	Differential Input High Voltage	150	—	—	mV	—
VIL	Differential Input Low Voltage	—	—	-150	mV	—

14.4 FlexRay

14.4.1 FlexRay - RxD

Table 48. FlexRay - RxD

Symbol	Description	Min	Typ	Max	Unit	Condition
C_CCRxD	Input capacitance on RxD pin	—	—	8	pF	—
uCCLogic_1	Threshold for detecting logic high	35	—	70	%	—
uCCLogic_0	Threshold for detecting logic low	30	—	65	%	—
dCCRxD01	Sum of delay from actual input to the D input of the first FF, rising edge [1]	—	—	10	ns	—
dCCRxD10	Sum of delay from actual input to the D input of the first FF, falling edge [1]	—	—	10	ns	—
dCCRxAsymAccept15	Acceptance of asymmetry at receiving CC with 15pF load [1]	-31.5	—	44	ns	—
dCCRxAsymAccept25	Acceptance of asymmetry at receiving CC with 25pF load [1]	-30.5	—	43	ns	—

[1] FlexRay RxD timing assumes an input signal slew rate of 2ns (20%/80%).

14.4.2 FlexRay - TxD

Table 49. FlexRay - TxD

Symbol	Description	Min	Typ	Max	Unit	Condition
dCCTxAsym	Asymmetry of sending CC, dCCTxD50% - N x gdBit [1]	-2.45	—	2.45	ns	N=1, gdBit = 100ns, TxD load = 25pF max
dCCTxDRISE25 + dCCTxDFALL25	Sum of rise and fall time of TxD signal at the output pin [1]	—	—	9	ns	TxD load = 25pF max, Z = 50ohms, delay = 0.6ns
dCCTxD01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxD load = 25pF max
dCCTxD10	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge [1]	—	—	25	ns	TxD load = 25pF max

[1] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

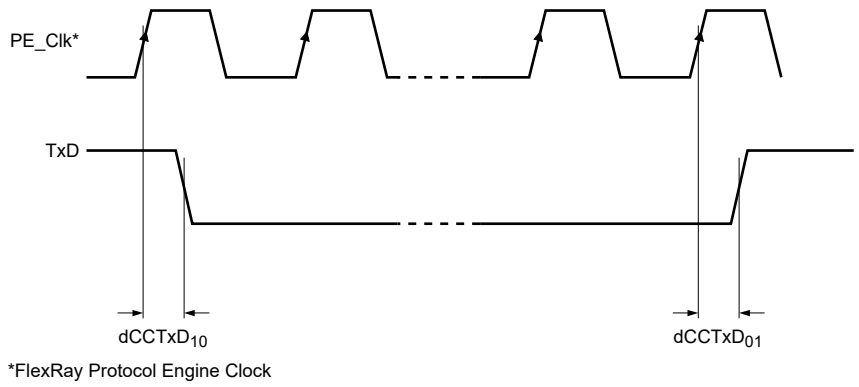


Figure 41. TxD Signal Propagation Delay

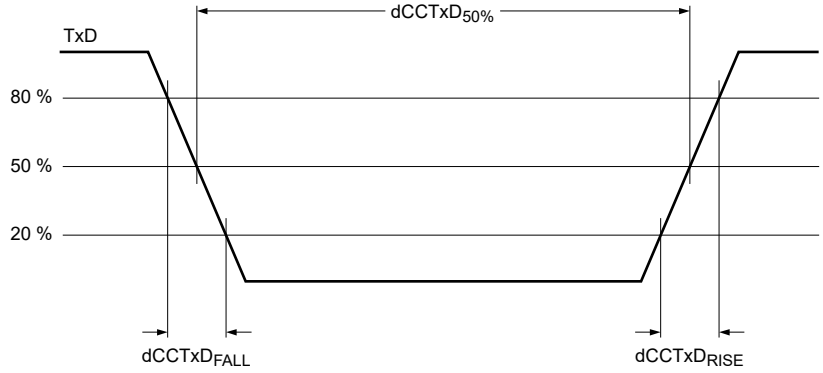


Figure 42. TxD Signal

14.4.3 FlexRay - TxEN

Table 50. FlexRay - TxEN

Symbol	Description	Min	Typ	Max	Unit	Condition
dCCTxENRISE25	Rise time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max
dCCTxENFALL25	Fall time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max
dCCTxEN01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxEN load = 25pF max
dCCTxEN10	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge [1]	—	—	25	ns	TxEN load = 25pF max

[1] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

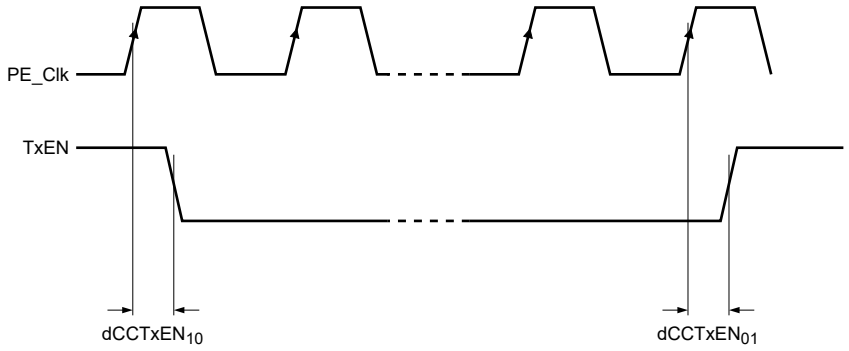


Figure 43. TxEN Signal Propagation Delay

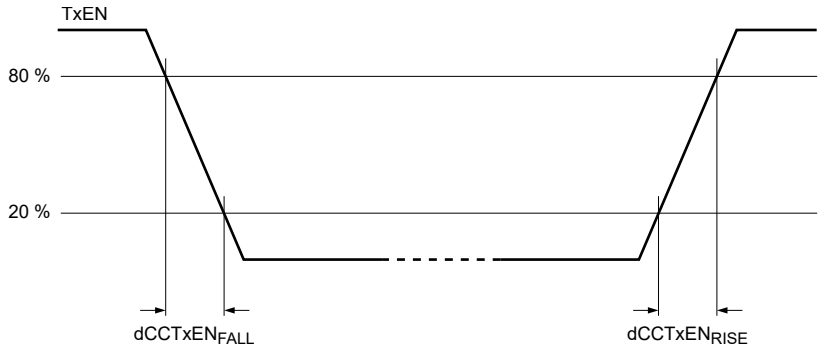


Figure 44. TxEN Signal

14.5 Ethernet

14.5.1 Ethernet Management Interface

Table 51. Ethernet Management Interface

Symbol	Description	Min	Typ	Max	Unit	Condition
fMDC	MDC clock frequency	—	—	5	MHz	—
MDIO_CH	MDC pulse width high time	40	—	60	%	—
MDIO_CL	MDC pulse width low time	40	—	60	%	—
tMDKHDX	MDC to MDIO delay [1]	((1+(2+6*EHOLD)*MDIO_HOLD) * tENET_CLK) – 3	—	((1+(2+6*EHOLD)*MDIO_HOLD) * tENET_CLK) + 8	ns	NEG=0
tMDKHDX	MDC to MDIO delay [1]	0.5 * (MDC clock) + 0.5 * tENET_CLK - 3	—	0.5 * (MDC clock) + 0.5 * tENET_CLK + 8	ns	NEG=1

Table continues on the next page...

Table 51. Ethernet Management Interface...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
MDIO_ISU	MDIO (input) to MDC rising edge setup time	8	—	—	ns	—
MDIO_IH	MDIO (input) to MDC rising edge hold time	1.32	—	—	ns	—

[1] In the equations provided for Min and Max values, tENET_CLK is the NETC system clock period in nanoseconds, EHOLD and MDIO_HOLD are the actual values programmed into these register fields, and "MDC clock" is the MDC clock period in nanoseconds.

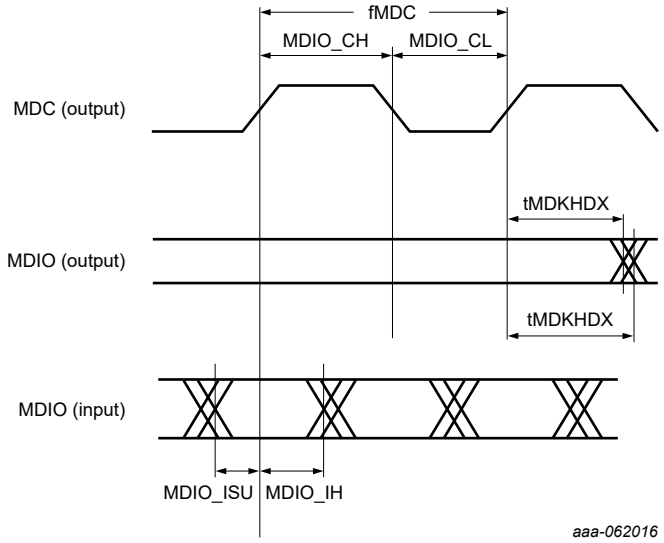


Figure 45. MDC / MDIO Timing

14.5.2 Ethernet MII

Table 52. Ethernet MII

Symbol	Description	Min	Typ	Max	Unit	Condition
tCYC_RX	RX_CLK period	—	40 / 400	—	ns	10/100 Mbps
ΔtCYC_RX	RX_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—
tS	Input setup time to RX_CLK [1]	5	—	—	ns	10/100 Mbps
tH	Input hold time to RX_CLK [1]	5	—	—	ns	10/100 Mbps
tCYC_TX	TX_CLK period [2]	—	40 / 400	—	ns	10/100 Mbps
ΔtCYC_TX	TX_CLK duty cycle (tPWH / tCYC) [2]	35	—	65	%	—
tD	Output delay from TX_CLK [2]	2	—	25	ns	10/100 Mbps

[1] Input timing assumes an input signal slew rate of 3ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

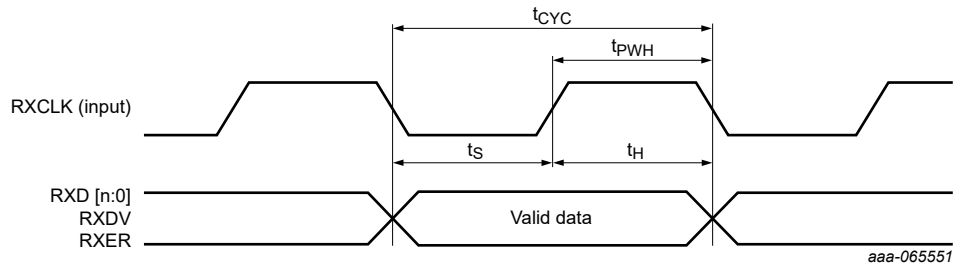


Figure 46. MII Receive Timing

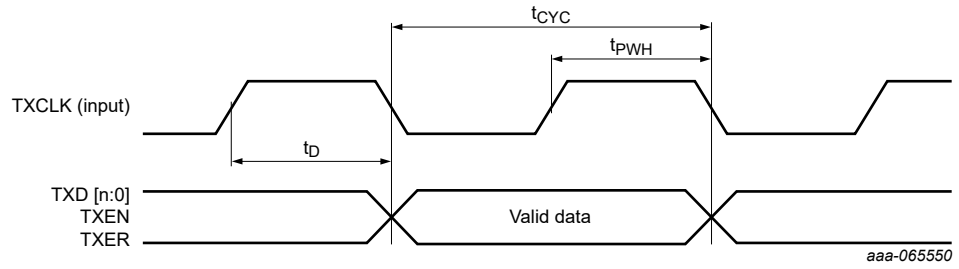


Figure 47. MII Transmit Timing

14.5.3 Ethernet RMII

Table 53. Ethernet RMII

Symbol	Description	Min	Typ	Max	Unit	Condition
fRMII_CLK	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	—
ΔtRMII_CLK	RMII_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—
tS	RXD[1:0], CRS_DV, RXER to RMII_CLK setup time [1]	4	—	—	ns	—
tH	RMII_CLK to RXD[1:0], CRS_DV, RXER hold time [1]	2	—	—	ns	—
tDATA_VALID	RMII_CLK to TXD[1:0], TXEN data valid [2]	—	—	14	ns	CLOAD = 25pF
tDATA_INVALID	RMII_CLK to TXD[1:0], TXEN data invalid [2]	2	—	—	ns	CLOAD = 25pF

[1] Input timing assumes an input signal slew rate of 3ns (20%/80%).
[2] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

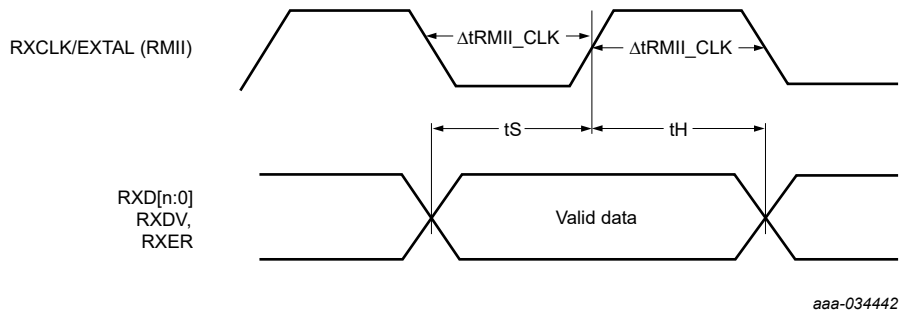


Figure 48. RMII Receive Timing

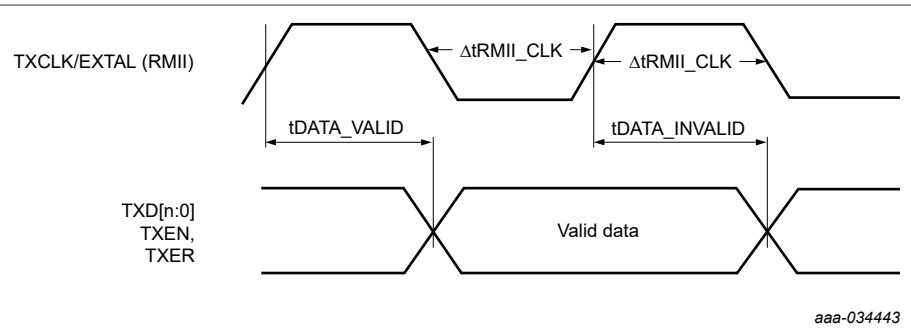


Figure 49. RMII Transmit Timing

14.5.4 Ethernet RGMII

Table 54. Ethernet RGMII

Symbol	Description	Min	Typ	Max	Unit	Condition
Tcyc	Clock cycle duration [1][2][3][4]	7.2	—	8.8	ns	—
TskewT	Data to clock output skew (at transmitter) [1][3][4][5]	-500	—	500	ps	—
TskewR	Data to clock input skew (at receiver) [1][3][4][5]	1	—	2.6	ns	—
Duty_G	Clock duty cycle for Gigabit [3][4][6]	45	—	55	%	—
Duty_T	Clock duty cycle for 10/100T [3][4][6]	40	—	60	%	—

[1] Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
[3] Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2
[4] RGMII timing specifications are valid for 1.8 V nominal I/O pad supply voltage.
[5] For all versions prior to RGMII v2.0 specifications; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.
[6] Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

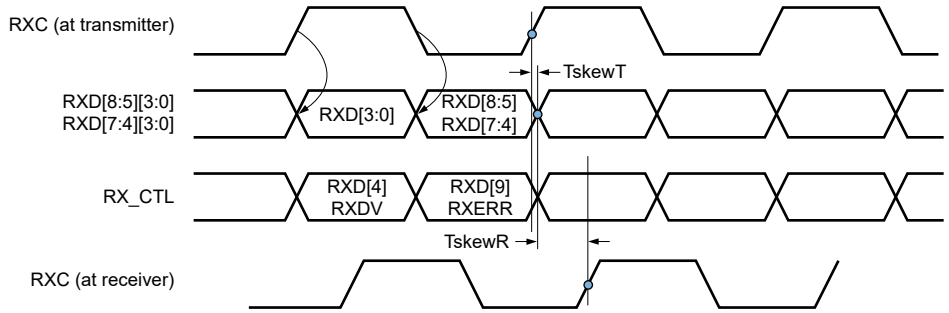


Figure 50. RGMII Receive Timing

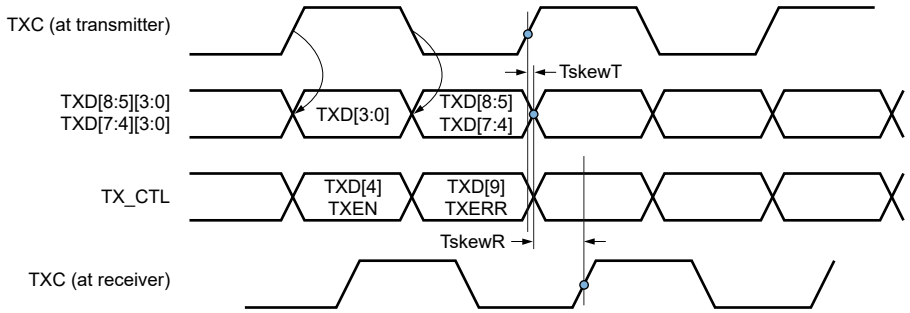


Figure 51. RGMII Transmit Timing

14.5.5 IEEE1588 interface

Table 55. IEEE1588 interface

Symbol	Description	Min	Typ	Max	Unit	Condition
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	—
tT1588CLKH/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	—
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	—
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	—
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	—
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	2 x t1588CLK	—	—	ns	—
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	—
tT1588OV	TMR_1588_CLK_OUT to TMR_1588_PULSE_OUT1/2,TMR_1588_ALARM_OUT1/2 valid	0.5	—	4.0	ns	—

Table continues on the next page...

Table 55. IEEE1588 interface...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tT1588TRIGH	TMR_1588_TRIG_IN1/2 pulse width	2 x t1588CLK	—	—	ns	—

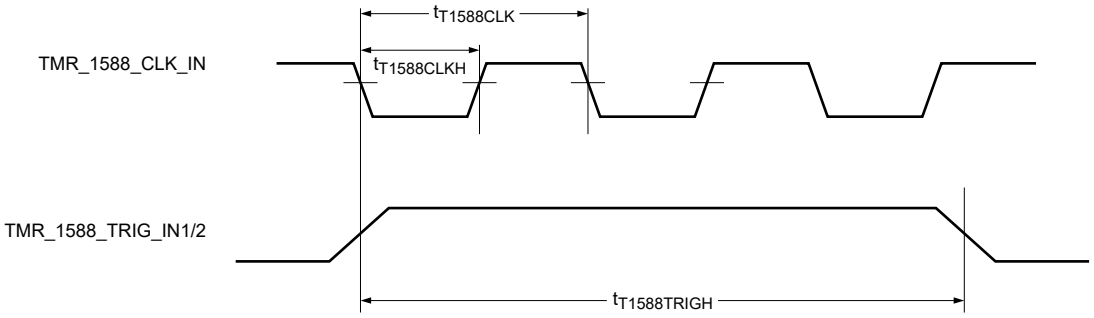
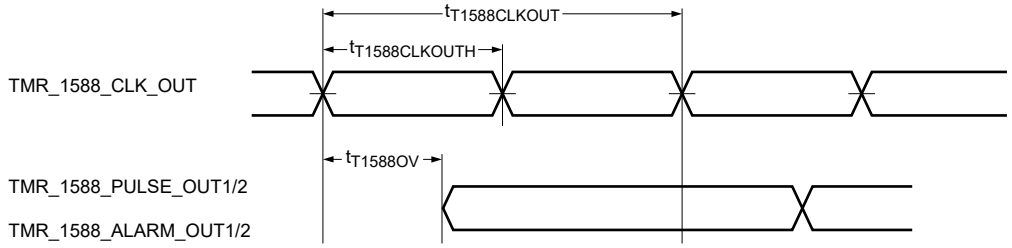


Figure 52. IEEE 1588 input AC timing



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 53. IEEE 1588 output AC timing

14.6 Memory interfaces

14.6.1 QuadSPI

An external resistor is needed to pull up a QuadSPI chip select signal.

14.6.1.1 QuadSPI Quad 1.8V DDR 66MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 56. QuadSPI Quad 1.8V DDR 66MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	SCK clock frequency [1][2]	—	—	66	MHz	DLL mode enabled
tCL_SCK	SCK clock low time [1][2]	6.818	—	—	ns	—
tCH_SCK	SCK clock high time [1][2]	6.818	—	—	ns	—

Table continues on the next page...

Table 56. QuadSPI Quad 1.8V DDR 66MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tOD_DATA	Data output delay (w.r.t. SCK) [2]	2.316	—	4.802	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [2] [3]	5.016 - n/fSCK	—	1.802 + m/fSCK	ns	—
tDVW	Input data valid window [1]	5.14	—	—	ns	—
tLSKEW	Skew target for Auto-learning mode [4]	1.89	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.
[4] Data valid window includes DLL Margin, and determines LEARNING skew targets which can be more pessimistic than tISU_SCK and tIH_SCK.

14.6.1.2 QuadSPI Quad 1.8V SDR 133MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 57. QuadSPI Quad 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	SCK clock frequency [1][2][3]	—	—	133	MHz	DLL mode enabled
tCL_SCK	SCK low time [1][3]	3.383	—	—	ns	—
tCH_SCK	SCK high time [1][3]	3.383	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [3]	-0.594	—	1.594	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [3] [4]	4.016 - n/fSCK	—	4.204 + m/fSCK	ns	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	0.580	—	—	ns	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	1.000	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).
[2] fSCK of 133.33MHz is also acceptable.
[3] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[4] Where m=TCSS and n=TCSH-1.

14.6.1.3 QuadSPI Octal 1.8V SDR 133MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 58. QuadSPI Octal 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	SCK clock frequency [1][2][3]	—	—	133	MHz	DLL mode enabled
tCL_SCK	SCK clock low time [1][3]	3.383	—	—	ns	—
tCH_SCK	SCK clock high time [1][3]	3.383	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [3]	-1.594	—	1.594	ns	—

Table continues on the next page...

Table 58. QuadSPI Octal 1.8V SDR 133MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tOD_CS	CS output delay (w.r.t. SCK) [3] [4]	3.016 - n/fSCK	—	2.704 + m/fSCK	ns	—
tDVW	Input data valid window [1]	4.609	—	—	ns	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	0.580	—	—	ns	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	0.9	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).
[2] fSCK of 133.33MHz is also acceptable.
[3] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[4] Where m=TCSS and n=TCSH-1.

14.6.1.4 QuadSPI Octal 1.8V DDR 100MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 59. QuadSPI Octal 1.8V DDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK_DQS	SCK / DQS frequency [1][2]	—	—	100	MHz	fSCK duty cycle distortion is in the range of 45%-55%.
tCL_SCK	SCK low time [1][2]	4.500	—	—	ns	—
tCH_SCK	SCK high time [1][2]	4.500	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	1.016	—	3.484	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [2] [3]	3.016 - n/fSCK	—	-0.016 + m/fSCK	ns	—
tDVW	Input data valid window [1]	3.284	—	—	ns	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.816	—	—	ns	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.684	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

14.6.1.5 QuadSPI Octal 1.8V DDR 133MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 60. QuadSPI Octal 1.8V DDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK_DQS	SCK / DQS frequency [1][2][3]	—	—	133	MHz	DLL mode enabled, fSCK duty cycle distortion is in the range of 45%-55%.

Table continues on the next page...

Table 60. QuadSPI Octal 1.8V DDR 133MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tCL_SCK	SCK low time [1][3]	3.383	—	—	ns	—
tCH_SCK	SCK high time [1][3]	3.383	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [3]	0.816	—	2.567	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [3] [4]	3.015 - n/fSCK	—	-1.33 + m/fSCK	ns	—
tDVW	Input data valid window [1]	2.314	—	—	ns	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	2.767	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] fSCK of 133.33MHz is also acceptable.
[3] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[4] Where m=TCSS and n=TCSH-1.

14.6.1.6 QuadSPI Octal 1.8V DDR 166MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 61. QuadSPI Octal 1.8V DDR 166MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK-DQS	SCK/DQS frequency [1][2]	—	—	166	MHz	fSCK duty cycle distortion is in the range of 45%-55%.
tCL_SCK	SCK low time [1][2]	2.711	—	—	ns	—
tCH_SCK	SCK high time [1][2]	2.711	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.616	—	2.095	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [2] [3]	3.016 - n/fSCK	—	-1.805 + m/fSCK	ns	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	2.105	—	—	ns	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

14.6.1.7 QuadSPI Octal 1.8V DDR 200MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 62. QuadSPI Octal 1.8V DDR 200MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK-DQS	SCK/DQS frequency [1][2]	—	—	200	MHz	fSCK duty cycle distortion is in the range of 45%-55%.
tCL_SCK	SCK low time [1][2]	2.25	—	—	ns	—
tCH_SCK	SCK high time [1][2]	2.25	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.616	—	1.634	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [2] [3]	3.016 - n/fSCK	—	-2.266 + m/fSCK	ns	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	1.644	—	—	ns	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.466	—	—	ns	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

14.6.1.8 QuadSPI Octal 1.8V SDR 100MHz

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 63. QuadSPI Octal 1.8V SDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	SCK clock frequency [1][2]	—	—	100	MHz	—
tCL_SCK	SCK clock low time [1][2]	4.5	—	—	ns	—
tCH_SCK	SCK clock high time [1][2]	4.5	—	—	ns	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	-2.822	—	2.822	ns	—
tOD_CS	CS output delay (w.r.t. SCK) [2] [3]	3.016 - n/fSCK	—	5.160 + m/fSCK	ns	—
tDVW	Input data valid window [1]	6.884	—	—	ns	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	3.036	—	—	ns	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	0.9	—	—	ns	—

[1] Input timing assumes an input signal transition of 1ns (20%/80%).
[2] Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] Where m=TCSS and n=TCSH-1.

14.6.1.9 QuadSPI configurations

Frequency (MHz)	200	133/100
DDR/SDR	DDR	SDR
External DQS alignment	Edge-aligned	Dummy pad loopback
Flash	Octal Flash (1.8 V)	Quad/Octal Flash (1.8 V)

Table continues on the next page...

Table continued from the previous page...

Frequency (MHz)	200	133/100
FLSHCR[TDH]	1	0
FLSHCR[TCHS]	2	2
FLSHCR[TCSS]	2	2
MCR[DLPEN]	0	1
DLLCR[DLLEN]	1	1
DLLCR[FREQEN]	1	0
DLLCR[DLL_REFCNTR]	2	2
DLLCR[DLLRES]	8	8
DLLCR[SLV_FINE_OFFSET]	0	0
DLLCR[SLV_DLY_OFFSET]	0	3
DLLCR[SLV_DLY_COARSE]	0	0
DLLCR[SLV_DLY_FINE]	0	0
DLLCR[SLAVE_AUTO_UPDT]	1	1
DLLCR[SLV_EN]	1	1
DLLCR[SLV_DLL_BYPASS]	0	0
DLLCR[SLV_UPD]	1	1
SMPR[DLLFSMPF*]	3	3
SMPR[FSDLY]	0	0
SMPR[FSPHS]	NA	1

14.6.1.10 QuadSPI interfaces

The QuadSPI module supports 2 interfaces; QSPI A & QSPI B. These interfaces are not independent & the QSPI chapter of the reference manual should be consulted for their usage. The table below summarizes which specifications are supported on each interface.

Table 64. QuadSPI interfaces

Specification / Interface	1.8V Quad	1.8V Octal	1.8V Hyperflash
QSPI A	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133/166/200 MHz	DDR 100/133/166/200 MHz
QSPI B	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133MHz	DDR 100/133/166/200 MHz

14.6.1.11 QuadSPI timing diagrams

The sections shows the QuadSPI timing diagrams for all modes supported by the device. All data is based on a negative edge data launch from the device.

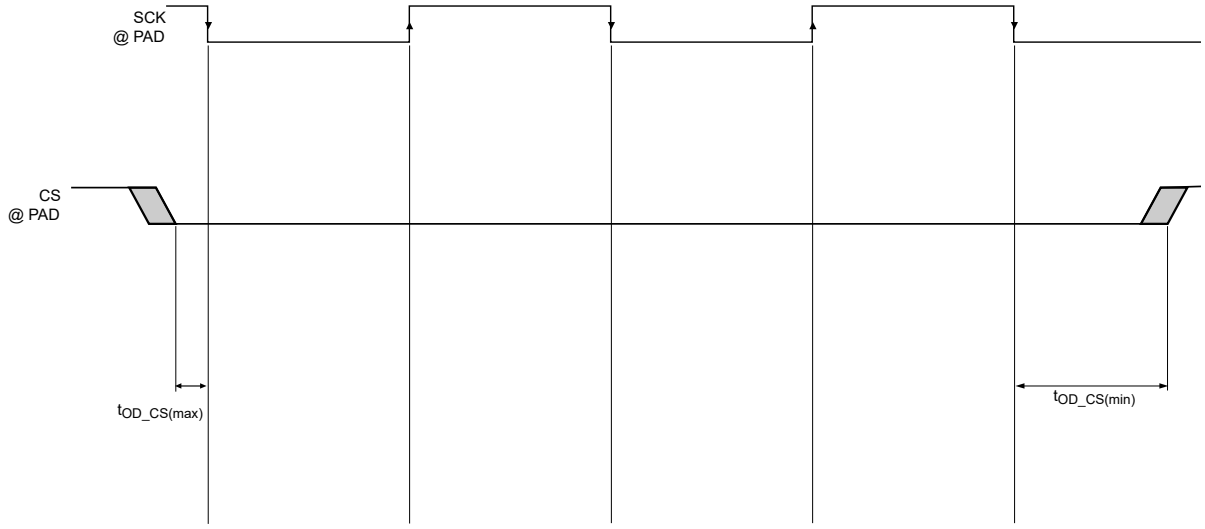


Figure 54. CS output timing

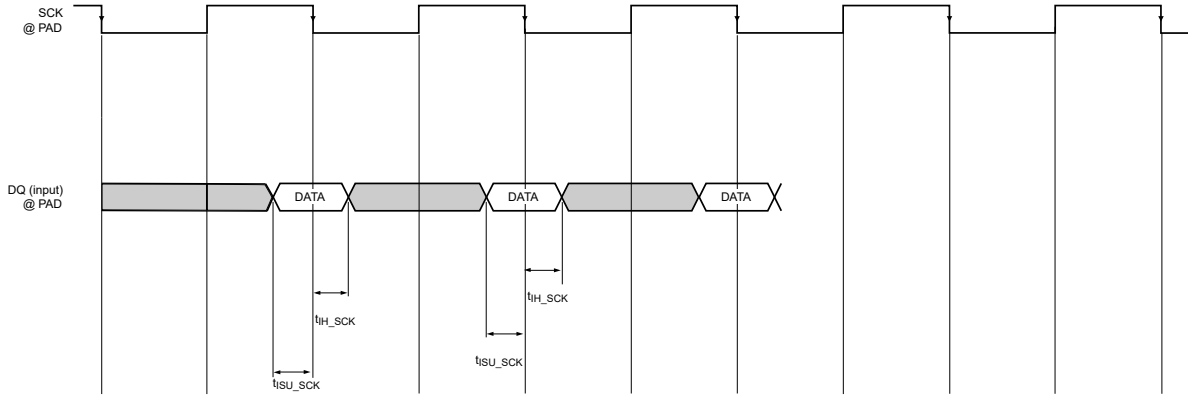


Figure 55. SDR input timing

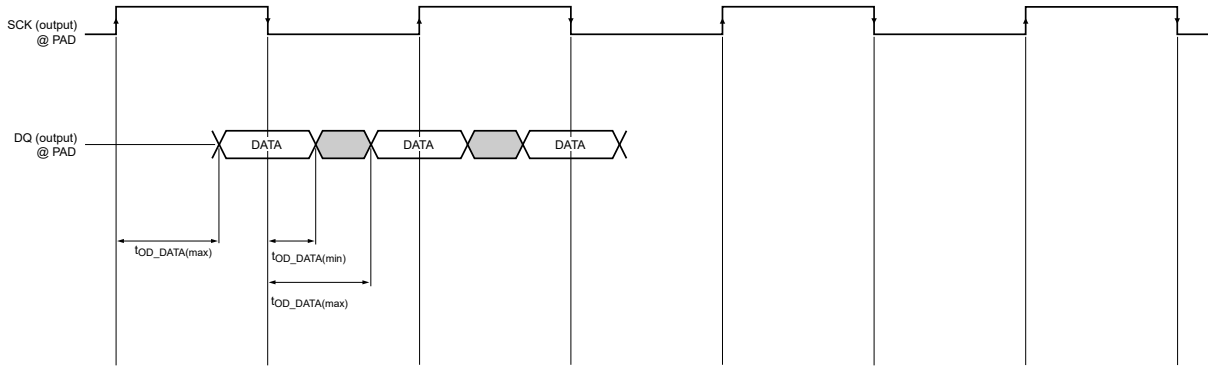


Figure 56. DDR output timing

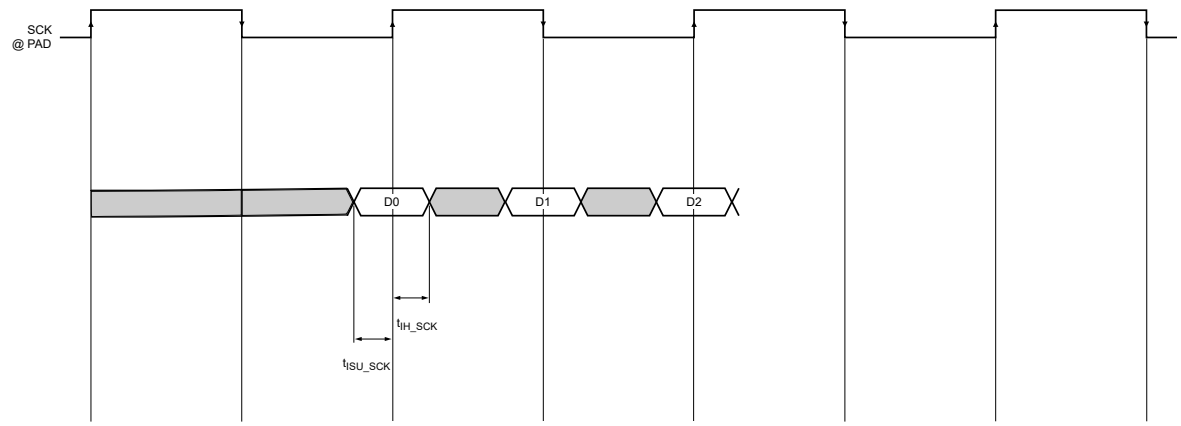


Figure 57. DDR with internal pad loopback input timing

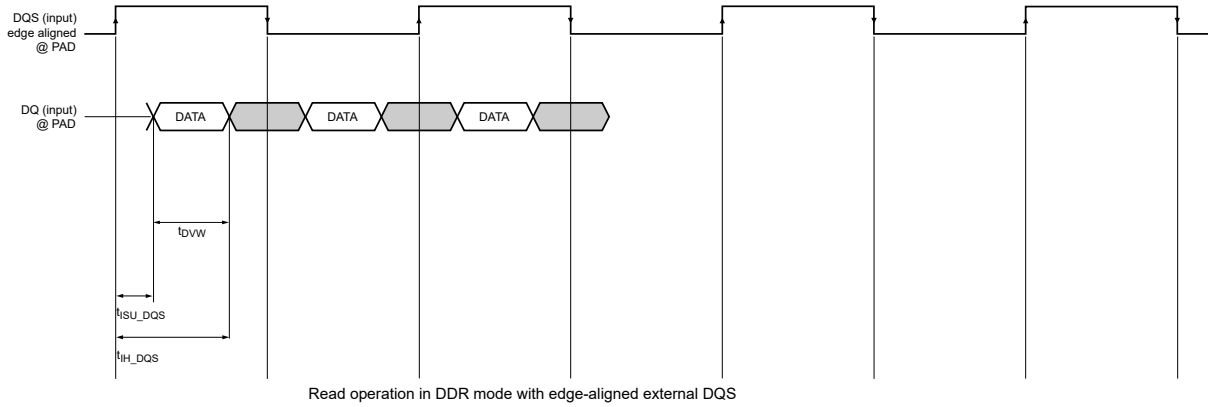


Figure 58. DDR edge-aligned DQS input timing

14.6.2 DDR

The chip supports the following memory types:

Table 65. DDR

Symbol	Description	Min	Typ	Max	Unit	Condition
LPDDR4X	LPDDR4X DRAM types speed class [1]	—	—	4267	MT/s	—
LPDDR5X	LPDDR5X DRAM types speed class [1]	—	—	7500	MT/s	—

[1] A table of valid values for this clock can be found in the Clocking Chapter in the Reference Manual. Values not listed in the said reference manual table are not supported.

14.6.2.1 DDR Common DC Input

The specifications given in the table below represent the common DC input conditions for all DDR interface modes. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins. Subsequent sections list input parameters for the specific memory interface standards.

Table 66. DDR Common DC Input

Symbol	Description	Min	Typ	Max	Unit	Condition
IIZ-BP	DDR data, mask, strobe pins input leakage current [1]	-100	—	100	uA	—
RTT	ON-die termination (ODT) programmable resistance [2][3][4]	—	open,120 ,60,40	—	Ohm	—
VREF	Internal reference voltage [5]	—	Variable	—	V	—
VIH_DC	Input high voltage [6]	VREF+ 0.04	—	—	V	—
VIL_DC	Input low voltage [6]	—	—	VREF-0. 04	V	—
VID-DC	Differential input voltage abs(DQS_t - DQS_c) [7]	0.1	—	—	V	—

[1] Leakage current is measured when the pin is configured to a high-impedance state with all on-die termination disabled. Leakage is valid for listed inputs over the range:0 <= VIN <= VDDQ. All pins not under test = VSS or VDDQ.
[2] All values are after ZQ Calibration
[3] For LPDDR4X and 5X ODT is a pull-down to VSS
[4] Refer to IBIS model for the complete IV curve characteristics
[5] Because termination at the DRAMs is configurable, there is no fixed setting. VREF is set automatically during interface training. The trained Vref value is dependent on DRAM driver impedence Ron and system effective ODT impedance Rtt.
[6] The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined.
[7] The differential voltage VID is the difference between the true and complement signals. Absolute value taken so that minimum spec applies to both high and low differential inputs.

14.6.2.2 DDR Common DC Output

Table 67. DDR Common DC Output

Symbol	Description	Min	Typ	Max	Unit	Condition
ROnPu	Output driver pull-up impedance: DQ, DQS, Address, Command, CLK outputs [1][2][3]	—	120, 60,40	—	Ohm	—
ROnPd	Output driver pull-down impedance: DQ, DQS, Address, Command, CLK outputs [1][2][3]	—	120, 60,40	—	Ohm	—
ROnPu_cs	Output driver pull-up impedance: chip select outputs [1][2][3]	—	400,100, 66,50	—	Ohm	—
ROnPd_cs	Output driver pull-down impedance: chip select outputs [2][3]	—	400,100, 66,50	—	Ohm	—
ROnPu_mr	Output driver pull-up impedance: MEMRESET_n [2][3]	50	75	100	Ohm	—
ROnPd_mr	Output driver pull-down impedance: MEMRESET_n	50	75	100	Ohm	—

[1] All values are after ZQ Calibration.
[2] MEMRESET_n driver is uncalibrated and minimum/maximum impedance value is process, voltage, and temperature dependent.
[3] Refer to IBIS model for the complete IV curve characteristics

14.6.2.3 LPDDR4X Output timing

Table 68. LPDDR4X Output timing

Symbol	Description	Min	Typ	Max	Unit	Condition
tCK(avg)	Average clock period [1]	—	468	—	ps	—
tDOeye	output data eye [1][2][3]	0.65	—	—	UI	—
tCAOeye	CA output data eye [1][4]	0.7	—	—	UI	—

[1] Measurements were done with signals terminated thru a 50ohm resistor to VSS, Phy output is calibrated to a drive strength of 40ohms.
[2] tDOeye is trained to be shifted 120 ps from DQS edge (tDQS2DQ learning)
[3] Tx DQS to MCLK edges are trained to be aligned
[4] Addr/Cmd is centered aligned by training.

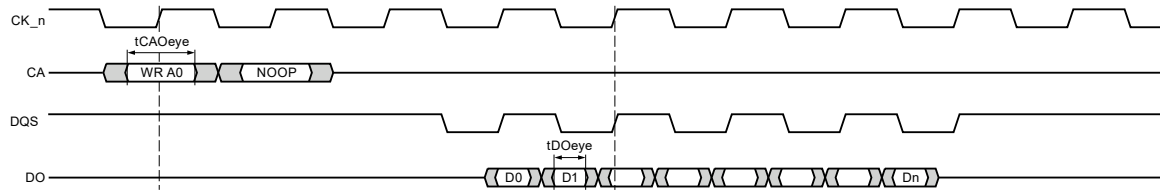


Figure 59. LPDDR4X output timing

14.6.2.4 LPDDR5X Output timing

Table 69. LPDDR5X Output timing

Symbol	Description	Min	Typ	Max	Unit	Condition
tCK(avg)	Average clock period [1]	—	1066.7	—	ps	—
tWCK(avg)	Average clock period [1]	—	266.7	—	ps	—
tDOeye	output data eye [1][2][3][4]	0.42	—	—	UI	—
tCAOeye	CA output data eye [1][5]	0.7	—	—	UI	—
tDOVW1	Output data eye width at midband voltage	0.48	—	—	UI	—
tDOVW2	Output data eye width at midband voltage +/- (vDIVW/2)	0.32	—	—	UI	—

[1] Measurements were done with signals terminated thru a 50ohm resistor to VSS, Phy output is calibrated to a drive strength of 40ohms.
[2] Measurements are done without any DFE enablement in measurement equipment.
[3] tDOeye is trained to be shifted 300-800 ps from DQS edge (tWCK2DQ learning)
[4] Tx tWCK to MCLK edges are trained to be aligned
[5] Addr/Cmd is centered aligned by training

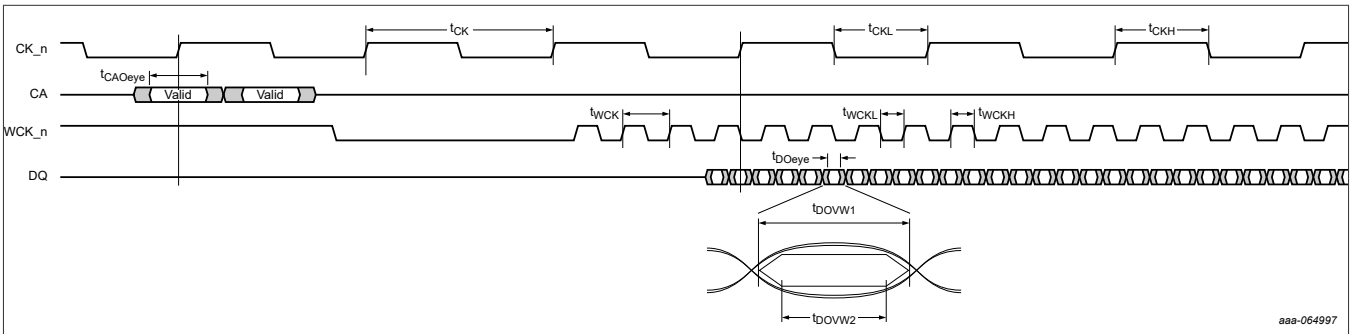


Figure 60. LPDDR5X output timing

14.6.3 uSDHC

14.6.3.1 uSDHC SD3.0/SDIO3.0/eMMC5.1 DDR - 50MHz

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 70. uSDHC SD3.0/SDIO3.0/eMMC5.1 DDR - 50MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fpp	Clock frequency (eMMC5.1 DDR) [1]	—	—	50	MHz	—
fpp	Clock frequency (SD3.0 DDR) [1]	—	—	50	MHz	—
tWL	Clock low time	8.8	—	—	ns	—
tWH	Clock high time	8.8	—	—	ns	—
tTLH	Clock rise time [1][2]	—	—	0.8	ns	—
tTHL	Clock fall time [2]	—	—	0.8	ns	—
tOD	SDHC output delay (output valid)	2.7	—	5.6	ns	SDHC_CLK to SDHC_DAT
tOD	SDHC output delay (output valid)	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD, See SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing figure
tISU	SDHC Input setup time [3]	1.6	—	—	ns	SDHC_DAT to SDHC_CLK
tISU	SDHC Input setup time [3]	4.8	—	—	ns	SDHC_CMD to SDHC_CLK, See SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing figure
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_DAT

Table continues on the next page...

Table 70. uSDHC SD3.0/SDIO3.0/eMMC5.1 DDR - 50MHz*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD, See SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing figure

[1] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
[3] Input signal timing assumes an input signal slew rate of 3ns (20%/80%).

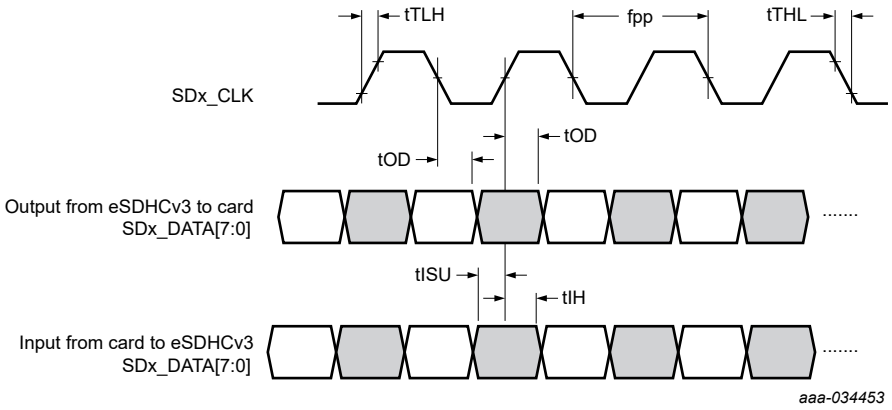


Figure 61. SD3.0/SDIO3.0/eMMC5.1 DDR Mode Interface Timing

14.6.3.2 uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR - 50 MHz

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 71. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR - 50 MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
fpp	Clock frequency (low speed) [1] [2]	—	—	400	kHz	—
fpp	Clock frequency (SD/SDIO full speed /high speed) [2][3]	—	—	25/50	MHz	—
fpp	Clock frequency (eMMC full speed/high speed) [2][4]	—	—	25/50	MHz	—
fOD	Clock frequency (identification mode) [2]	100	—	400	kHz	—
tWL	Clock low time	8.8	—	—	ns	—
tWH	Clock high time	8.8	—	—	ns	—
tTLH	Clock rise time [2][5]	—	—	0.8	ns	—
tTHL	Clock fall time [2][5]	—	—	0.8	ns	—

Table continues on the next page...

Table 71. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR - 50 MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tOD	SDHC output delay (output valid) [2]	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT
tISU	SDHC Input setup time [6]	4.8	—	—	ns	SDHC_CMD / SDHC_DAT to SDHC_CLK
tIH	SDHC Input hold time [6]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT

[1] In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V.
[2] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[3] In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[4] In normal (full) speed mode for MMC card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[5] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
[6] Input signal timing assumes an input signal slew rate of 3ns (20%/80%).

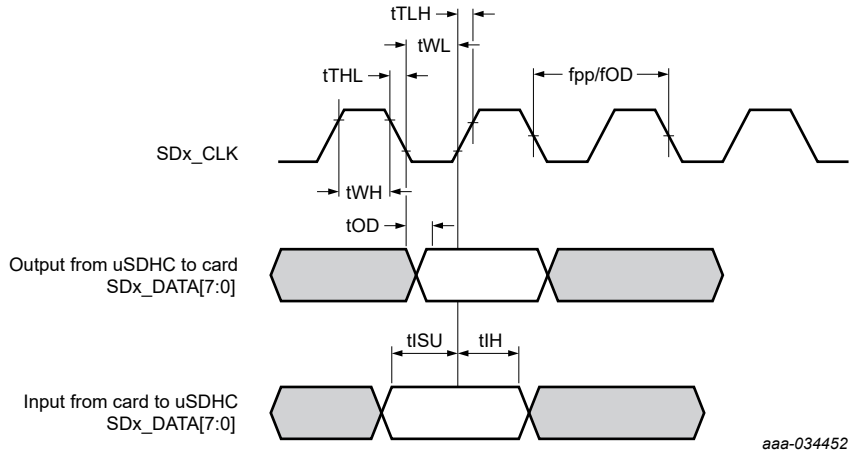


Figure 62. SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing

14.6.3.3 uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR-100MHz

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 72. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR-100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition
tCLK	Clock frequency [1]	—	—	100	MHz	—
tCL	Clock low time	4.5	—	—	ns	—
tCH	Clock high time	4.5	—	—	ns	—
tTLH	Clock rise time [1][2]	—	—	0.8	ns	—
tTHL	Clock fall time [1][2]	—	—	0.8	ns	—
tOD	uSDHC output delay [1]	-3.5	—	1.3	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT

Table continues on the next page...

Table 72. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR-100MHz*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tISU	uSDHC input setup time [3]	1.6	—	—	ns	SDHC_CMD / SDHC_DAT to SDHC_CLK
tIH	uSDHC input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT

[1] Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
[3] Input signal timing assumes an input signal slew rate of 1ns (20%/80%).

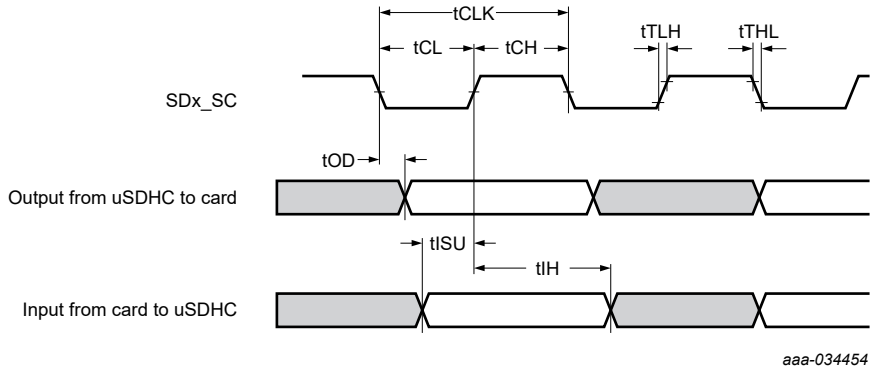


Figure 63. SDR-100 Mode Interface Timing

14.6.3.4 uSDHC eMMC5.1 SDR-HS200

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 73. uSDHC eMMC5.1 SDR-HS200

Symbol	Description	Min	Typ	Max	Unit	Condition
tCLK	Clock frequency [1]	—	—	200	MHz	—
tCL	Clock low time	2.2	—	—	ns	—
tCH	Clock high time	2.2	—	—	ns	—
tTLH	Clock rise time [1][2]	—	—	0.8	ns	—
tTHL	Clock fall time [1][2]	—	—	0.8	ns	—
tOD	uSDHC output delay [1]	-1.2	—	0.6	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT
tODW	Input data window [3]	2.6	—	—	ns	SDHC_DAT / SDHC_CMD

[1] Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
[3] Input signal timing assumes an input signal slew rate of 1ns (20%/80%).

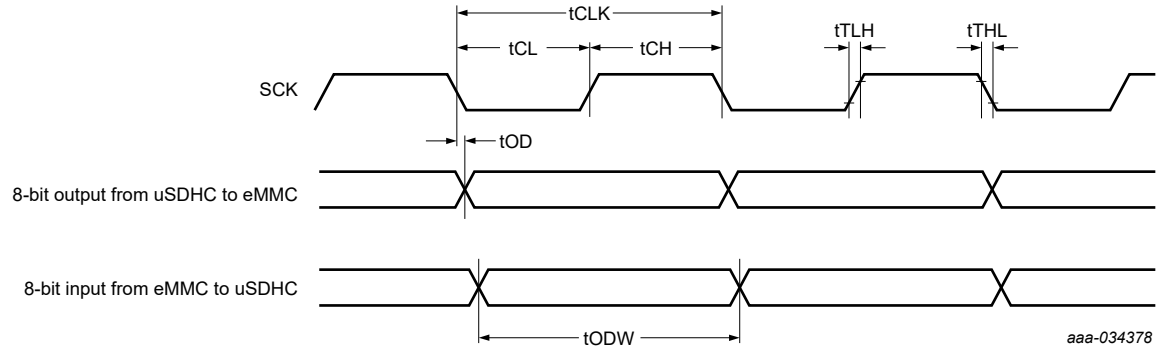


Figure 64. HS200 Mode Interface Timing

14.6.3.5 uSDHC eMMC5.1 DDR-HS400

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 74. uSDHC eMMC5.1 DDR-HS400

Symbol	Description	Min	Typ	Max	Unit	Condition
fPP	Clock frequency [1]	133	—	200	MHz	—
tCL	Clock low time	2.2	—	—	ns	—
tCH	Clock high time	2.2	—	—	ns	—
tTLH	Clock rise time [1][2]	—	—	0.8	ns	—
tTHL	Clock fall time [1][2]	—	—	0.8	ns	—
tOD1	Output skew from Edge of Data to SCK [1][3]	0.45	—	—	ns	—
tOD2	Output skew from Edge of SCK to Data [1][3]	0.45	—	—	ns	—
tRQD	Input skew (data) [4]	—	—	0.45	ns	—
tRQC	Input skew (CMD) [4][5]	—	—	0.45	ns	—
tRQHD	Hold skew (data) [4]	—	—	0.45	ns	—
tRQHC	Hold skew (CMD) [4][5]	—	—	0.45	ns	—
tOD	uSDHC Output delay [1]	-1.2	—	0.6	ns	SDHC_CLK to SDHC_CMD

[1] Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
[3] Board skew margin between CLK and DATA/CMD is considered as +/-50 ps in calculations
[4] Input signal timing assumes an input signal slew rate of 1ns (20%/80%).
[5] Spec numbers SD6 and SD7 are also applicable for the CMD input timing for HS400 mode in enhanced strobe mode. For HS400 mode without enhanced strobe, CMD input timing is the same as for HS200 mode.

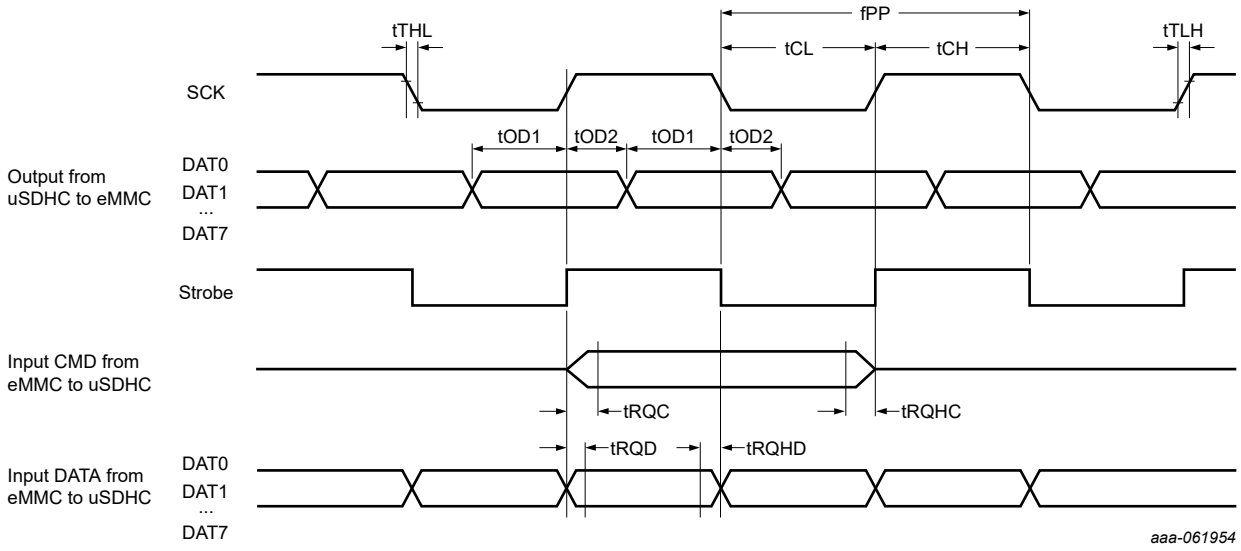


Figure 65. HS400 Mode Interface Timing

14.7 Debug modules

14.7.1 JTAG Boundary Scan

The following table gives the JTAG specifications in boundary scan mode.

Table 75. JTAG Boundary Scan

Symbol	Description	Min	Typ	Max	Unit	Condition
tJCYC	TCK cycle time [1][2][3]	100	—	—	ns	—
tJDC	TCK clock pulse width [1][3]	45	—	55	%	—
tTCKRISE	TCK rise/fall time [1][4]	—	—	3	ns	—
tTMSS, tTDIS	TMS, TDI data setup time [1][5]	5	—	—	ns	—
tTMSH, tTDIH	TMS, TDI data hold time [1][5]	5	—	—	ns	—
tTDOV	TCK low to TDO data valid [1][6][7]	—	—	17.5	ns	—
tTDOI	TCK low to TDO data invalid [1][7]	0	—	—	ns	—
tTDOHZ	TCK low to TDO high impedance [1][7]	—	—	17.5	ns	—
tJCMPPW	JCOMP assertion time [1]	100	—	—	ns	—
tJCMPS	JCOMP setup time to TCK high [1]	40	—	—	ns	—
tBSDV	TCK falling edge to output valid [1][7][8]	—	—	600	ns	—
tBSDVZ	TCK falling edge to output valid out of high impedance [1][7]	—	—	600	ns	—

Table continues on the next page...

Table 75. JTAG Boundary Scan...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tBSDVHZ	TCK falling edge to output high impedance [1][7]	—	—	600	ns	—
tBSDST	Boundary scan input valid to TCK rising edge [1]	15	—	—	ns	—
tBSDHT	TCK rising edge to boundary scan input invalid [1]	15	—	—	ns	—

[1] These specifications apply to JTAG boundary scan mode only.
[2] JTAG port interface speed only. Does not apply to boundary scan timing.
[3] TCK pin must have an external pull down.
[4] The TCK rise/fall time specification applies to the input clock transition required in order to meet the TDO output specifications that are relative to TCK.
[5] Input timing assumes an input signal slew rate of 3ns (20%/80%).
[6] Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
[7] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[8] Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

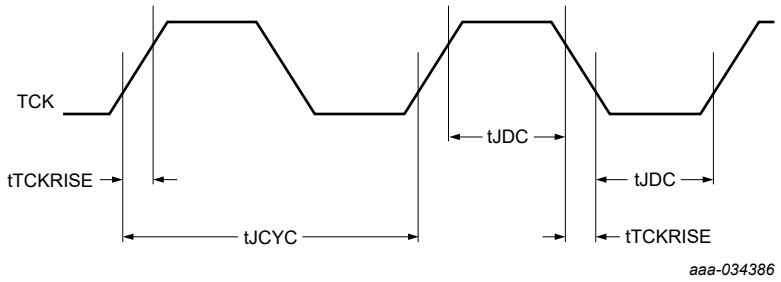


Figure 66. JTAG TCK Input Timing

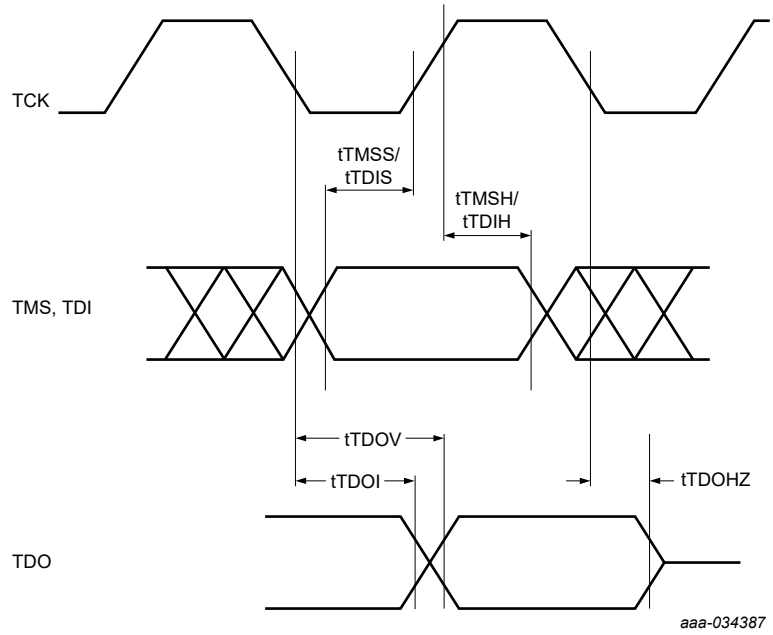


Figure 67. JTAG Test Access Port Timing

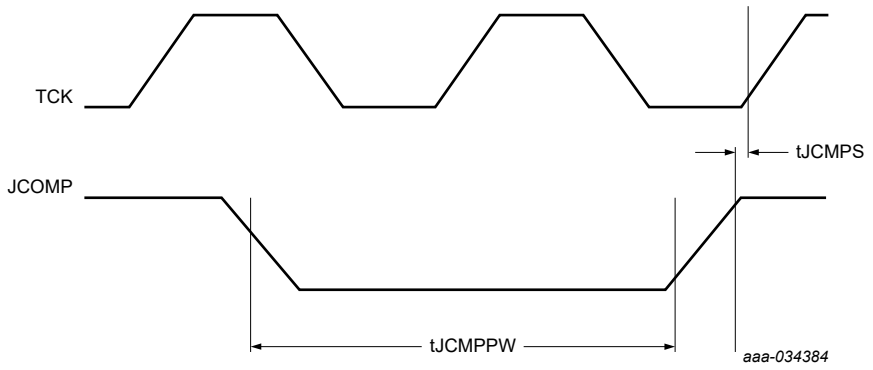


Figure 68. JCOMP Timing

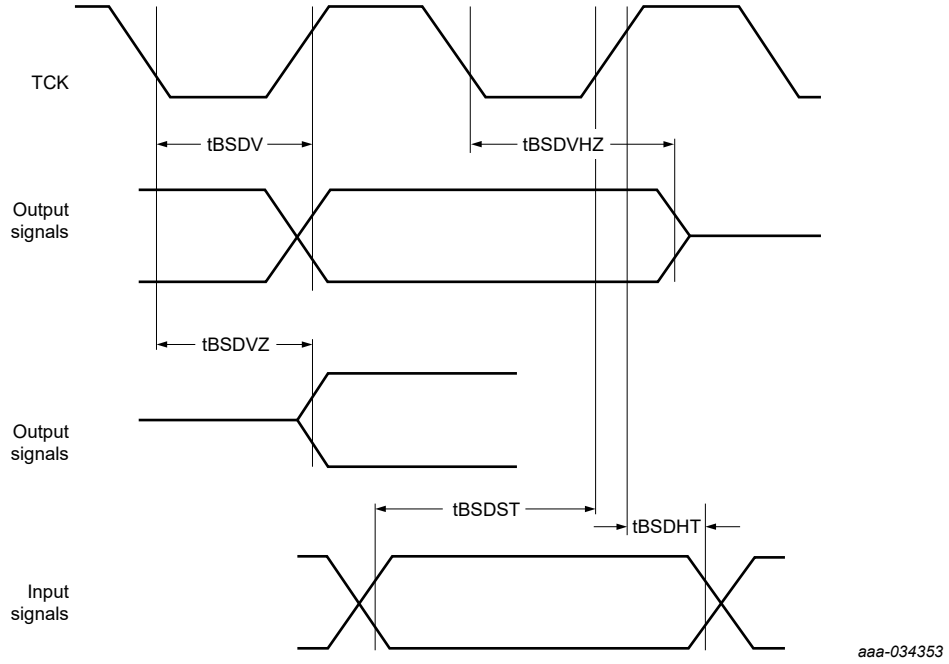


Figure 69. Boundary Scan Timing

14.7.2 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 76. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
tTCYC	Absolute minimum TCK cycle time (TDO sampled on posedge of TCK) [1][2]	50	—	—	ns	—
tTCYC	Absolute minimum TCK cycle time (TDO sampled on negedge of TCK) [1][2]	25	—	—	ns	—
tJDC	TCK clock pulse width	45	—	55	%	—

Table continues on the next page...

Table 76. JTAG Debug Interface Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tNTDIS	TDI data setup time [3]	5	—	—	ns	—
tNTDIH	TDI data hold time [3]	5	—	—	ns	—
tNTMSS	TMS data setup time	5	—	—	ns	—
tNTMSH	TMS data hold time	5	—	—	ns	—
tNTDOD	TDO propagation delay from falling edge of TCK [4][5]	—	—	17.5	ns	—
tNTDOH	TDO hold time with respect to falling edge of TCK [5]	1	—	—	ns	—
tTDOHZ	TCK low to TDO high impedance [5]	—	—	17.5	ns	—

[1] Maximum frequency for TCK is limited to 6MHz during BOOTROM startup of the device, when the system clock is the trimmed 300 MHz FIOSC.
[2] TCK pin must have external pull down.
[3] Input timing assumes an input signal slew rate of 3ns (20%/80%).
[4] Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
[5] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

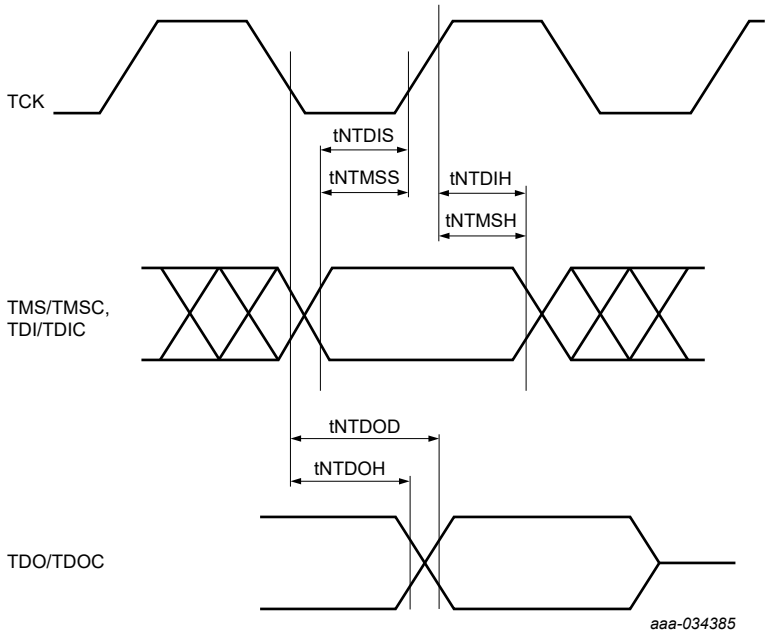


Figure 70. JTAG debug Interface Timing

14.7.3 Debug trace timing specifications

The following table describes the Debug trace electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns.

Table 77. Debug trace timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fTRACE	Trace clock frequency (trace on Fast pads)	—	—	200	MHz	—
tDVW	Data output valid window	1.2	—	—	ns	—
tDIV	Data output invalid	-0.3	—	—	ns	—

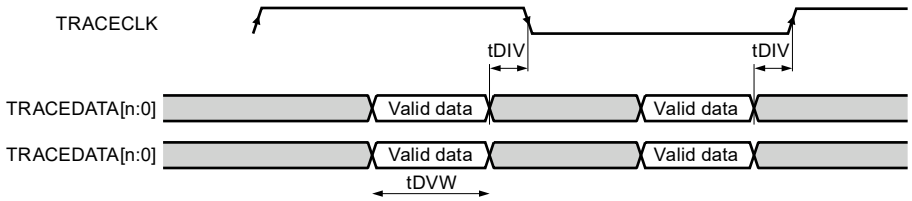


Figure 71. Trace CLKOUT specifications

15 Pinouts

For package pinouts and signal descriptions, see the Reference Manual.

16 Packaging

This device is offered in following package types.

Package Type	Document Number
19 mm x 19 mm 798-ball FCBGA	98ASA01985D

Note: *Contact NXP sales representative for package drawing.*

17 Revision history

The following table lists the changes in this document.

Document ID	Release date	Description
S32N55 v.4.0	27 April 2026	Product data sheet - Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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