MPF5032BMMA5ES – NXP Standard

Configuration report for QM OTP program ID: A5 rev C

Rev. 1.0 - 08/03/2023 **Report**

1 General description

The PF5030 is a power management integrated circuit (PMIC) designed for S32Z2/E2 processors. Its input voltage up to 5.25 V maximum for automotive drive train market allows to be ideally attached to NXP front system supply families (FS86, FS6x) or any other front supply.

Built-in one-time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after startup, offering flexibility for different system states.

Note: Electrical characteristics for the PF5030 are maintained in the datasheet.

2 Features and benefits

Voltage Range

• 5 V DC maximum input voltage

• Support operating voltage range down to 3.3 V

• Low Power OFF mode with low sleep current (15 uA typ.)

Power Supplies

• BUCK1/2: Low voltage integrated synchronous BUCK converter

  ■ Configurable output voltage from 0.7 V to 1.5 V and current capability up to 3.5 A DC

  ■ Capable of multiphase operation for up to 7.0 A DC

• BUCK3: Low voltage integrated synchronous BUCK converter

  ■ Configurable output voltage from 1.0 V to 4.1 V and current capability up to 2.5 A DC

• LDO1/2: Low voltage LDO regulator for MCU I/O and system peripheral

  ■ Configurable Output voltage from 1.1 V to 4.1 V and current capability up to 400 mA DC

System support

• 1x input pins for power-ON detection, 1.8 V / 3.3 V / 5.0 V compatible

• Analog Multiplexer with full System Voltages monitoring

• Enhanced master/slave power up sequencing management thru XFAILB pin

• 10 ms optional RSTB release delay during power up for certain MCU compliancy

• Device control via 32 bits I2C 1 MHz interface with 8-bit CRC

Compliancy

• EMC optimization techniques on switching regulators including spread spectrum

• EMI robustness supporting various automotive EMI Test standards

• Conducted Emission: IEC 61967-4

• Conducted Immunity: IEC 62132-4

Functional Safety

• ASILD capability on UV/OV for all S32Z2/E2 power rails (0.8 V, 1.1 V, 1.8 V and 3.3 V)

• Independent voltage Monitoring Circuitry

• Up to 6 voltage monitoring inputs for PF5030 and external voltage rails with 1 % target accuracy

• Logical and Analog Built-in Self-Test

• Safety Outputs with latent fault detection mechanism (PGOOD, RSTB, FS0B)

Configuration and Enablement

• QFN 40 pins with exposed pad for optimized thermal management

• OTP programming for device customization

3 Applications

• EV propulsion and Power train domain controller

• Chassis integrated systems

• S32Z2/E2 companion chip

4 Ordering information

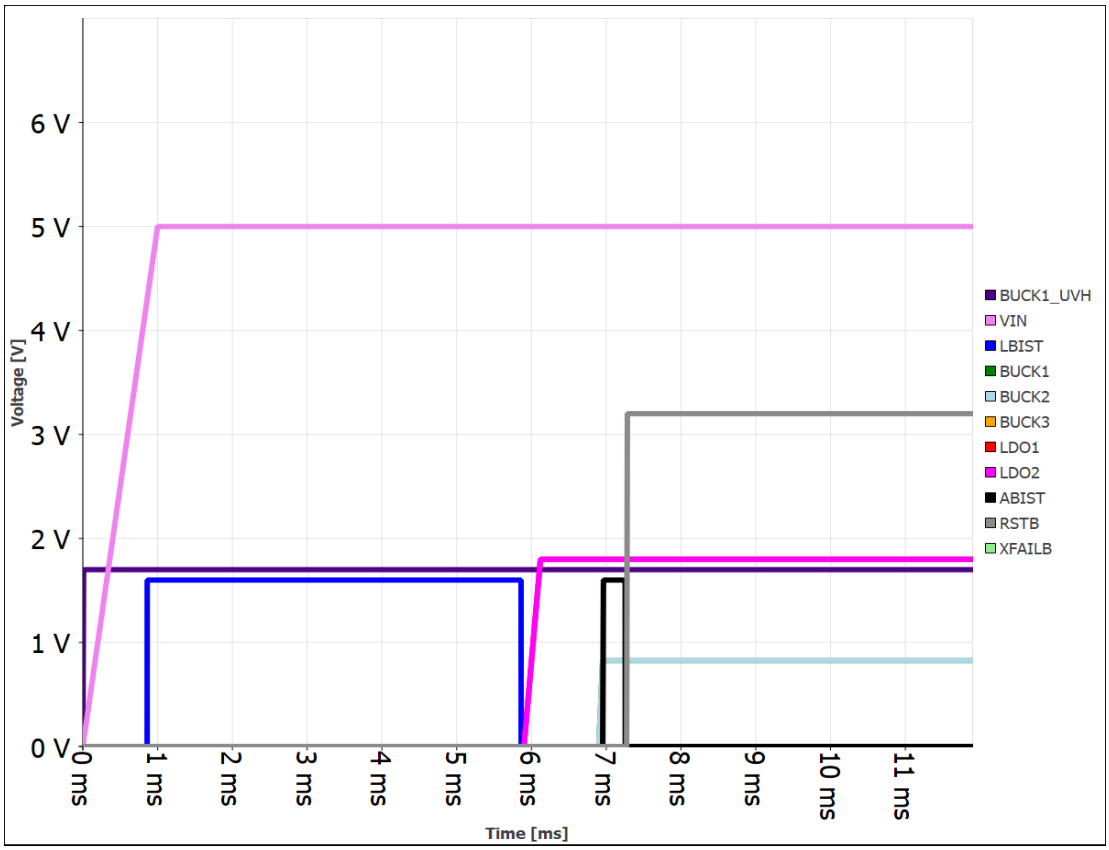
Table 1. Ordering information

Type number[1][2]	Package		
	Name	Description	Version
MPF5032BMMA5ES	QFN40eP	QFN40ep, plastic, thermally enhanced, wettable flanks, 6 x 6 x 0.85mm, 0.5 mm pitch, 40 pins	SOT618-18(D)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

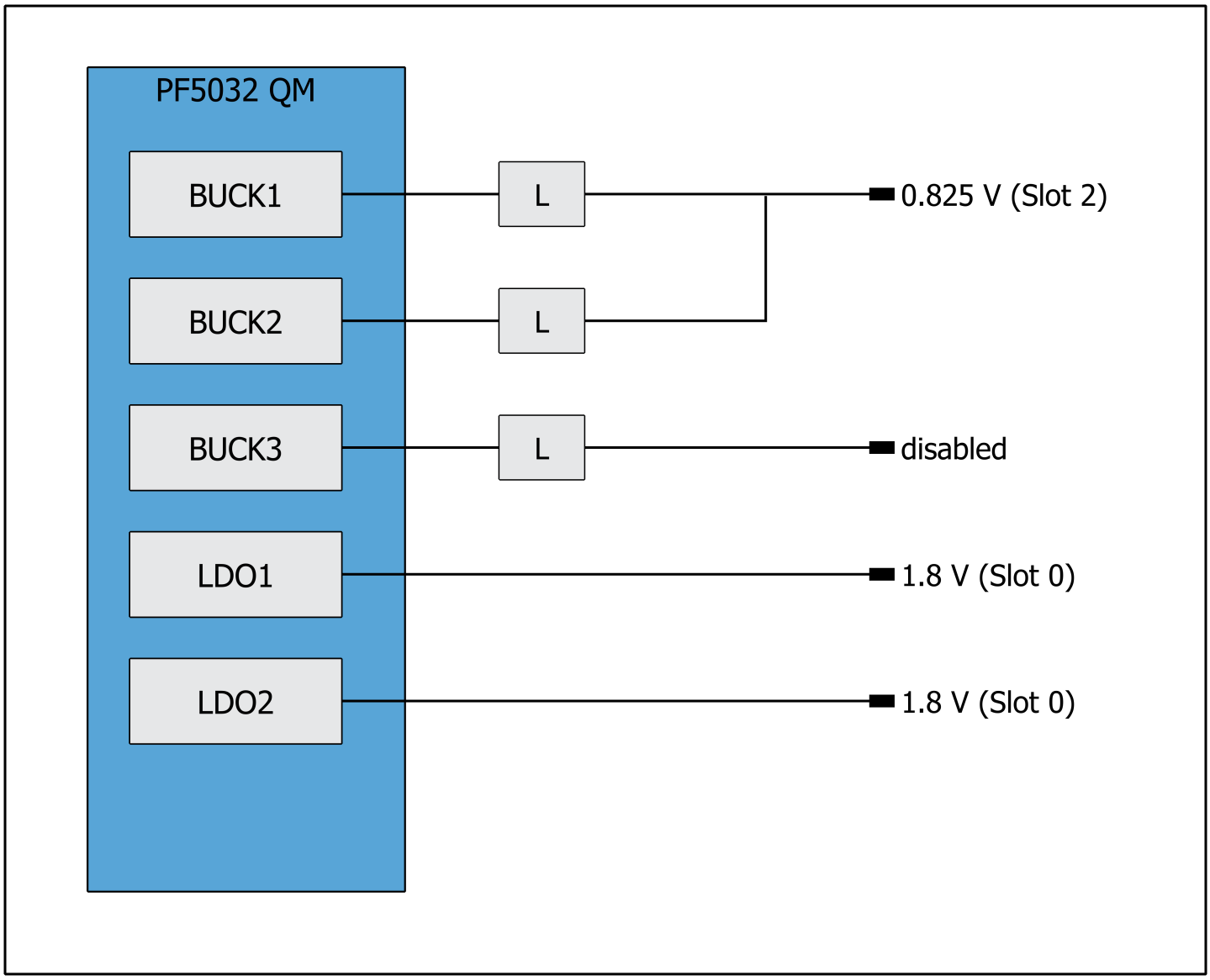
[2] For production part number use prefix S instead of P

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See PF5030 datasheet for parametric details. The OTP configuration summary for A5 sequence ID is provided in Tables below.

Table 2. Main Configuration

Functional block	Feature	OTP selection
System configuration	Main Device I2C Address	0x22
	FailSafe Device I2C Address	0x23
	Device ID	1
	VIN Undervoltage Threshold	5.0 V (UV at 4.3 V)
	Power Down Sequence In Case Of DFS	Power down sequence
	Autoretry Enable Configuration	Enabled
	Autoretry Number Configuration	Endless
	Deglitcher Time SCL Signal	15 ns
	Delay Between Main State Machine	2 ms
	Program ID Low	5
	Program ID High	A
	VMON4 External Regulator Assign	LDO1
	VMON5 External Regulator Assign	LDO2
Clock and Synchronisation	Enable Clock Modulation	Clock modulation enabled
	Clock Modulation Configuration	Triangular modulation
	XFAILB Configuration	Synchronization enabled
	XFAILB Release Slot	Slot 0
	XFAILB Assertion Impact	Power down when XFAILB is asserted low

Table 3. Power-up sequence

Functional block	Feature	OTP selection
Power-up sequence	BUCK1 Power-up Slot	Slot 2
	BUCK2 Power-up Slot	Slot 2
	BUCK3 Power-up Slot	Slot 1
	LDO1 Power-up Slot	Slot 0
	LDO2 Power-up Slot	Slot 0
	Power-up/down Slot Timing	0.5 ms
	Power-up Last Slot	Power up ends in slot 3
	Power-down First Slot	Power down starts in slot 3

Table 4. Switching and LDOs regulators

Functional block	Feature	OTP selection
BUCK1/2 multiphase operation	BUCK1 And BUCK2 Multiphase Operation	Enabled
	DVS Ramp Of BUCK1/2	15.62 mV/us
BUCK1 configuration	BUCK1 Inductor Selection	0.47 uH
	BUCK1 Output Voltage	0.825 V
	BUCK1 Transconductance	2.91
	BUCK1 Current Limitation	5 A
	BUCK1 Phase Delay	No delay
	BUCK1 TSD Behavior	BUCK1 shutdown
BUCK2 configuration	BUCK2 Enable	Enabled
	BUCK2 Inductor Selection	0.47 uH
	BUCK2 Output Voltage	0.825 V
	BUCK2 Transconductance	2.91

	BUCK2 Current Limitation	5 A
	BUCK2 Phase Delay	Delay 4
	BUCK2 TSD Behavior	BUCK2 shutdown
BUCK3 configuration	BUCK3 Enable	Disabled
	BUCK3 Inductor Selection	1 uH
	BUCK3 Output Voltage	1.1 V
	BUCK3 Current Limitation	2.1 A
	BUCK3 Phase Delay	Delay 3
	BUCK3 TSD Behavior	BUCK3 shutdown
	BUCK3 Soft Start Ramp	10.41 mV/us
LDO1 configuration	LDO1 Load Switch Mode Enable	Disabled
	LDO1 Output Voltage	1.8 V
	LDO1 TSD Behavior	LDO1 shutdown
LDO2 configuration	LDO2 Load Switch Mode Enable	Disabled
	LDO2 Output Voltage	1.8 V
	LDO2 TSD Behavior	LDO2 shutdown

Table 5. System safety configuration

Functional block	Feature	OTP selection
System safety configuration	Watchdog Infinite Window	Infinite open window
	Watchdog Mode Selection	Simple watchdog
	RSTb 8s Timer Disable	Counter enabled
	RSTB Delay	No delay

	RSTB Pgood	Fault asserting RSTb will assert PGOOD
	Revert Backup Safety Path	Enabled
	SVS Max Value Allowed	No SVS

Table 6. Voltage monitoring

Functional block	Feature	OTP selection
VMON0 configuration	VMON0 Enable	Enabled
	VMON0 Undervoltage Threshold	96.0 %
	VMON0 Overvoltage Threshold	104.0 %
	VMON0 Undervoltage Deglitcher	100us/400 us
	VMON0 Overvoltage Deglitcher	100 us/400 us
	VMON0 Assignement To PGOOD	Not assigned
	VMON0 Assignment To ABIST1	Assigned
VMON1 configuration	VMON1 Enable	Enabled
	VMON1 Voltage Configuration	0.825 V
	VMON1 Undervoltage Threshold	96.0 %
	VMON1 Overvoltage Threshold	104.0 %
	VMON1 Undervoltage Deglitcher	100 us/400 us
	VMON1 Overvoltage Deglitcher	100 us/400 us
	VMON1 Assignement To PGOOD	Not assigned
	VMON1 Assignment To ABIST1	Assigned
VMON2 configuration	VMON2 Enable	Enabled
	VMON2 Voltage Configuration	0.875 V
	VMON2 Undervoltage Threshold	90.0 %
	VMON2 Overvoltage Threshold	110.0 %

	VMON2 Undervoltage Deglitcher	100 us/400 us
	VMON2 Overvoltage Deglitcher	100 us/400 us
	VMON2 Assignement To PGOOD	Not assigned
	VMON2 Assignment To ABIST1	Assigned
VMON3 configuration	VMON3 Enable	Disabled
	VMON3 Voltage Configuration	1.1 V
	VMON3 Undervoltage Threshold	97.5 %
	VMON3 Overvoltage Threshold	104.0 %
	VMON3 Undervoltage Deglitcher	100 us/400 us
	VMON3 Overvoltage Deglitcher	100 us/400 us
	VMON3 Assignement To PGOOD	Not assigned
	VMON3 Assignment To ABIST1	Not assigned
VMON4 configuration	VMON4 Enable	Enabled
	VMON4 Voltage Configuration	1.8 V
	VMON4 Undervoltage Threshold	95.5 %
	VMON4 Overvoltage Threshold	104.5 %
	VMON4 Undervoltage Deglitcher	100 us/400 us
	VMON4 Overvoltage Deglitcher	100 us/400 us
	VMON4 Assignement To PGOOD	Not assigned
	VMON4 Assignment To ABIST1	Assigned
VMON5 configuration	VMON5 Enable	Enabled
	VMON5 Voltage Configuration	1.8 V
	VMON5 Undervoltage Threshold	95.5 %
	VMON5 Overvoltage Threshold	104.5 %

	VMON5 Undervoltage Deglitcher	100 us/400 us
	VMON5 Overvoltage Deglitcher	100 us/400 us
	VMON5 Assignement To PGOOD	Not assigned
	VMON5 Assignment To ABIST1	Assigned

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