

PN76AC

NFC controller with ultra-low-power card detection and NCI interface

Rev. 1.4 — 22 October 2026

Objective data sheet

1 General description

This document describes the functionality and electrical specification of the PN76AC high power NFC controller with NCI interface.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, PN76AC is a robust solution for access control which can generate a strong RF field in difficult environments.

PN76AC communicates with a connected host through a physical interface using the NCI 2.2 protocol.

PN76AC supports highly innovative and unique features, which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveshape control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the PN76AC are mentioned in [Section 18](#). For information about the CLIF/PCRM register and EEPROM configuration, refer to [ref.\[1\]](#).



2 Features and benefits

2.1 RF functionality

As a highly integrated high performance full NFC Forum-compliant NFC controller for contactless communication at 13.56 MHz, this NFC controller IC utilizes an outstanding modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.

PN76AC supports the following RF operating modes:

2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

2.1.2 ISO/IEC 14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

2.1.4 Card emulation

- ISO/IEC 14443-A card mode from 106 kbit/s up to 848 kbit/s (PICC) with active load modulation for increased communication range.

2.2 Transmitter

- Transmitter with high RF output power of 2.0 W
- Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
- Adaptive waveshape control (AWC)

2.3 Receiver

- Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

2.4 Integrated polling loop

- RF polling loop according to NFC Forum

2.5 RF debugging support

- RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on predefined trigger conditions.
- One digital and one analog debug signal is provided by the chip for connection of an oscilloscope

2.6 Host interface

PN76AC supports host connection based on SPI target interface with data rates up to 15 Mbit/s.

PN76AC supports host connection based on I²C target interface with data rates up to 3.4 Mbit/s.

3 Applications

- Aliro-based Physical Access Control

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	battery supply voltage on pin VBAT	$V_{BAT} \geq V_{DDIO}$	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO	1.8 V supply	1.62	-	1.98	V
		3.3 V supply	2.4	-	3.6	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	supply with VDDPA from internal VDDPA LDO	1.5	-	5.7	V
I_{pd}	power down current	$V_{DD(VDDPA)} = V_{DD(VDDIO)} = V_{DD(VDD)} = 3.0\text{ V}$; hard power down state; pin VEN set LOW, $T_{amb} = 25\text{ }^{\circ}\text{C}$, External supply by VDDIO	-	40	105	μA
I_{stb}	standby current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	45	110	μA
I_{ULPCD}	average ultra low-power card detection current	$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{DD(VDDPA)} = V_{DD(VDDIO)} = V_{DD(VDD)} = 3.0\text{ V}$, 330 ms Polling interval, 50 R antenna matching	-	22	-	μA
$I_{DD(VDDPA)}$	supply current on pin VDDPA	supplied via VUP_TX (TX_LDO active)	-	-	350	mA
$P_{(PA)}$	Transmitter output power	supplied via VUP_TX (TX_LDO active)	-	-	2.0	W
T_{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB TX current _{max} = 350 mA @ VDDPA _{max} = 5.7V	-40	-	+85	$^{\circ}\text{C}$
		in still air with exposed pins soldered on a 4 layer JEDEC PCB TX current _{max} = 120 mA @ VDDPA _{max} = 3.6 V	-40	-	+105	$^{\circ}\text{C}$
T_{stg}	storage temperature	no supply voltage applied	-55	-	+150	$^{\circ}\text{C}$
T_{j_max}	maximum junction temperature	-	-	-	+125	$^{\circ}\text{C}$

5 Firmware versions

The product allows firmware updates. For the description of the firmware versions and the related content, refer to the related firmware release notes.

6 Ordering information

Table 2. Ordering information

Type number	Package			Packing	12NC
	Name	Description	Version		
PN76ACEV/C100Y	VFBGA64	Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm. MSL = 3. This version has the firmware v03.01.01 installed.	SOT1307-2	Tape and Reel packing. Minimum order quantity = 4000 pcs	9354 659 05518

7 Block diagram

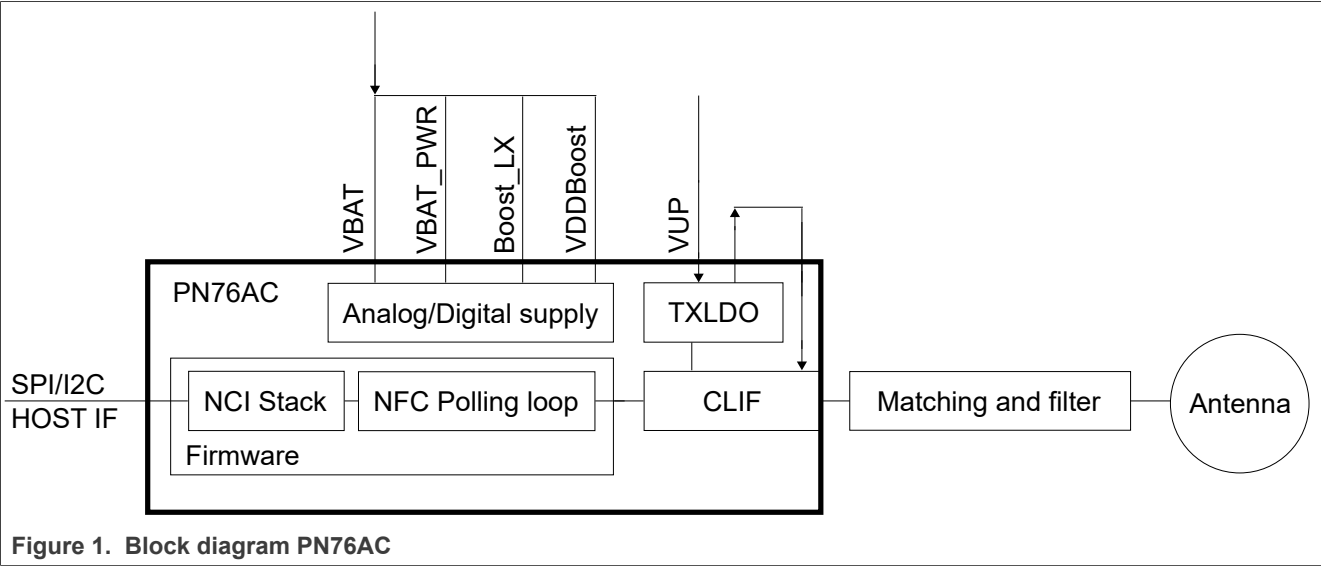


Figure 1. Block diagram PN76AC

8 Pinning information

8.1 Pin description VFBGA64

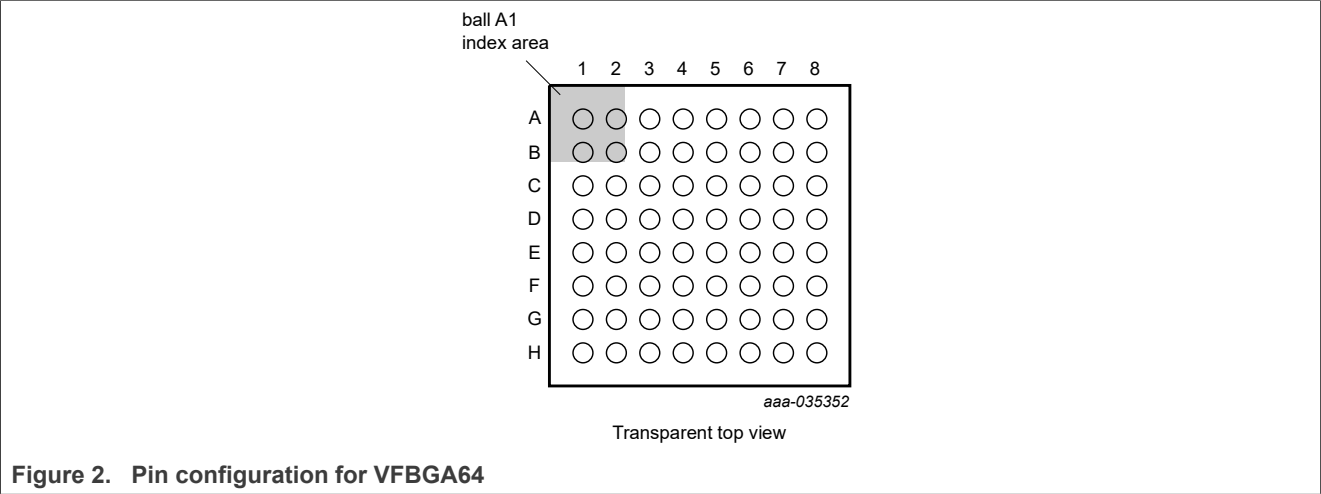


Figure 2. Pin configuration for VFBGA64

Table 3. Pin description VFBGA64

Pin number	Symbol	Type	Description PN76AC
Host interface			
E6	ATX_A	I/O	HSUART RX, I ³ C SDA, SPI MISO, I ² C SDA
E5	ATX_B	I/O	HSUART CTS, I ³ C SCL, SPI SCK, I ² C SCL
D6	ATX_C	I/O	HSUART RTS, I ³ C address bit 0, SPI NSS, I ² C address bit 0
D5	ATX_D	I/O	HSUART TX, I ³ C address bit 1, SPI MOSI, I ² C address bit 1
B7	IRQ	Output	Host communication / event interrupt signal
XTAL connection			
F8	XTAL1	Input	Crystal / system clock input
G8	XTAL2	Output	Clock output (amplifier-inverted signal output) for crystal
Hardware reset			
B3	VEN	Input	Hardware reset, low active (independent from V _{VDDIO}) Avoid a floating or unexpected toggling of the pin.
Supply pins			
H2	VSS_PA	Supply GND	Transmitter ground
G3	VSS_PLL	Supply GND	PLL ground (low noise)
A2	VSS_PWR	Supply GND	DC-DC disabled but boost ground must be connected
D3	VSS_REF	Supply GND	PMU ground
B2, E3	VSS_SUB	Supply GND	Substrate ground
C3	VSS_PMU	Supply GND	PMU ground
F4	VSS_DIG	Supply GND	Digital ground

NFC controller with ultra-low-power card detection and NCI interface

Table 3. Pin description VFBGA64...continued

Pin number	Symbol	Type	Description PN76AC
F3	VSS_NFC	Supply GND	NFC ground
E1	VBAT	Supply	System supply, used to supply the analog and digital blocks, memory and internal voltage references
A8	VDDIO	Supply	I/O pads power supply
G1	VDDPA	Supply	Transmitter supply
F1	VUP_TX	Supply	Input supply voltage for transmitter LDO
B1	VDDBOOST	Supply	DC-DC boost supply - DC-DC disabled but supply must be connected
A1	BOOST_LX	Output	DC-DC disabled but output must be connected
A3	VBATPWR	Supply	To be connected to BOOST_LX and transmitter power supply
Outputs for stabilizing cap			
A4	VDDNV	Output	Nonvolatile memory power supply, to be connected to ground via a 220 nF blocking cap
D2	VREF	Output	High quiescent reference voltage, to be connected to ground via a 100 nF blocking cap
C1	VDDC	Output	Power supply for Digital Core, to be connected to ground via a 220 nF blocking cap
G2	TXVCM	Output	Transmitter voltage common mode, to be connected to ground via a 220 nF blocking cap
F2	TXVCASC	Output	TX decoupling cap, to be connected to VDDPA
H6	VMID	Output	Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap
RF debug signals			
G7	AUX1	I/O	Test bus 1 / Digital I/O
F7	AUX2	I/O	Test bus 2 / Digital I/O
H8	AUX3	Output	Test bus 3 / GPIO 8
Antenna connections			
H5	RXP	Input	Receiver input "Positive"
H4	RXN	Input	Receiver input "Negative"
H1	TX1	Output	Antenna driver output 1
H3	TX2	Output	Antenna driver output 2
Wake-up / Digital debug signals			
E8	GPIO0/ Digital TestBus0	Input/Output	GPIO0 / Digital test bus 0
D8	GPIO1/Digital TestBus1	Input/Output	GPIO1 / Digital test bus 1
E7	GPIO2/ Digital TestBus2	Input/Output	GPIO2 / Digital test bus 2

Table 3. Pin description VFBGA64...continued

Pin number	Symbol	Type	Description PN76AC
D7	WKUP_REQ / GPIO3 / Digital TestBus3	Input	Wake-up request when in Standby and ULPCD; GPIO3 / Digital test bus 3
C5	GPIO4	Input/Output	GPIO4
B5	GPIO5	Input/Output	GPIO5
Host interface selection			
C6	HOST_IF_SEL1	Input	Shall always be on GND on PN76AC
C7	HOST_IF_SEL0	Input	Host interface select 0 - selection of SPI or I ² C Level L: I ² C host interface Level H: SPI host interface
Pins not to be connected			
B4	RFU	N/A	Do not connect or connect to GND
G4	RFU	N/A	Do not connect or connect to GND
H7	RFU	N/A	Do not connect
A6	RFU	N/A	Do not connect
B6	RFU	N/A	Do not connect
C2	RFU	N/A	Internal test pin. To be connected to GND.
A7	RFU	N/A	Do not connect
B8	RFU	N/A	Do not connect
C4	RFU	N/A	Do not connect
C8	RFU	N/A	Do not connect
D1	RFU	N/A	Do not connect
D4	RFU	N/A	Do not connect
E2	RFU	Output	Do not connect
E4	RFU	N/A	Do not connect
F5	RFU	N/A	Do not connect
F6	RFU	N/A	Do not connect
G5	RFU	N/A	Do not connect
G6	RFU	N/A	Do not connect
A5	RFU	Output	Do not connect

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

9 Functional description

9.1 Functional overview

PN76AC is a NFC controller with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuit and the functionality to realize a reader for smart access solution.

Connection to host controller

PN76AC can be connected to a host through I²C or SPI physical interface.

For NFC data exchange a high-level NCI 2.2 protocol implementation extended by proprietary commands is available.

Integrated NFC polling loop

All supported RF technologies in [Section "RF functionality"](#) can be independently enabled within this PCD polling loop. The sequence of RF technologies within the PCD polling loop cannot be modified.

Clock supply

PN76AC uses an external 27.12 MHz crystal as the clock source for generating the RF field and its internal digital logic.

Transmitter LDO (VDDPA LDO)

The transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the VDDPA LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

Ultra Low-power card detection

The ultra low-power card detection (ULPCD) enables saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the ultra low-power card detection provides a functionality, which allows to power down the NFC controller for a certain amount of time to save energy. After some time, the NFC controller sends a RF ping to detect a card in the RF field. If no card is detected, the device can go back to the power-down state.

Dynamic power control 2.0

The next-generation dynamic power control (DPC2.0) with true transmitter current measurement works autonomously without application FW interaction. Avoiding additional processing at application FW is important for time-critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matching.

Adaptive waveshape control

The adaptive waveshape control (AWC) helps to keep the wave shapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna-matching procedure and does not require any matching compromises to be taken.

Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true baseband amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and nonstandard compliant cards and mobile phones. An Integrated Chip scope allows for

performing a nonintrusive debugging of receiver signals without the need to connect additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred through configured host interface to a host microcontroller and visualized on a PC by the NFC Cockpit development tool.

A virtual COM interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller.

Analog debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system.

Automatic EMD error handling

Automatic EMD error handling according to ISO/IEC14443 is supported. In addition, the EMD error handling is widely configurable, which allows adaptations in case of future possible specification changes.

Firmware update

PN76AC supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN76AC will be in download mode.

For the secure firmware update, the following interfaces can be used: I²C and SPI.

EEPROM configuration

Non-volatile EEPROM memory of PN76AC is used to store configuration data that must be preserved in case PN76AC is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory as well as other configuration data which must be preserved during power supply disconnect is stored in this EEPROM memory. Examples for these are settings for receiver sensitivity, DPC, waveshaping, ULPCD, and power supply configurations

RF configuration

PN76AC allows an automatic RF protocol selection based on the actual polling loop state. Pre-defined user configuration data is stored in non-volatile memory (EEPROM) and is automatically loaded for the modulation scheme currently activated by the polling loop.

The loading of the RF configuration to the non-volatile memory is typically done only once during production.

Note: Frequent automatic reloading of the RF configuration in the application is not recommended, since the number of possible configuration updates (EEPROM programming cycles) is technically limited. The device allows to store data which requires a frequent update in the application in registers / RAM.

9.2 NCI interface

The functionality of the NCI interface is described in the user manual and the NCI 2.2 Interface standard.

9.3 Endianness

The endianness describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234
Address x: 12
Address x+1: 34

The location of word-sized data (16 bit) is as follows:

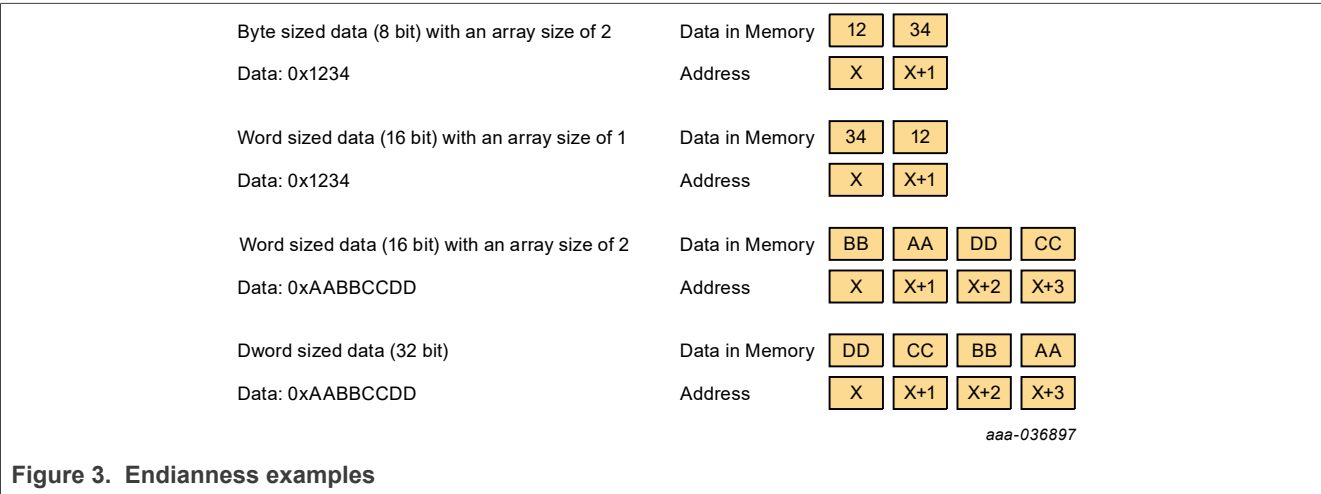
Value hex: 0x1234
Address x: 34
Address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is big-endian. The placement of nibbles of the variable is little-endian.
Value hex: 0xAABBCCDD
Address x: BB
Address x+1: AA
Address x+2: DD
Address x+3: CC

The location of double word-sized data (32 bit) is as follows:

Value hex: 0xAABBCCDD
Address x: DD
Address x+1: CC
Address x+2: BB
Address x+3: AA



The PN76AC is a little-endian system. This means that the byte at the lower address is read first.

9.4 Initial calibration

The PN76AC requires a calibration before the RF field is switched on for the first time with unloaded condition. "Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

- Write EEPROM CfgNovCal – 0x00
- Write REGISTER TX_NOV_CALIBRATE_AND_STORE_VAL - 0x01
- Write EEPROM CfgNovCal – 0x02

9.5 System power states

The PN76AC can operate in different power states. The functionality and current consumption depends on the actual system power state.

Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT.

In addition, state changes are triggered from the user application of the device.

Disconnecting and connecting the power supply on VBAT restarts the PN76AC always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN76AC always in Active State.

The following power states are supported:

Table 4. System power states

Power state	Description
Power OFF state	The PN76AC device (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO)
PMU OFF state	The PN76AC device is disabled via a low signal on pin VEN. No internal clocks of the PN76AC are active. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, RX ULPCD detect, ULP abort signal on WKUP_REQ.
ULPCD state	The ULPCD (ultra low-power card detection) offers the highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, abort signal on WKUP_REQ or a reset (VEN) of the PN76AC. Only the wake-up timer is active during ULPCD Standby state. The ULPCD comprises 2 phases: 1. Calibration phase: In this phase, an RF field is established and the field strength (RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register. 2. Measurement phase: In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.
Standby state	The user application can set the PN76AC into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-

Table 4. System power states...continued

Power state	Description
	power state. A wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, ULPDET, LPDET, wake-up counter, power loss on VDDIO, GPIO, RXPROT, No High Temp on TX and so on.
Active state	The PN76AC is able to process internal or external events or data. All external power supply sources and the external clock need to be available, and all internal clocks are active.

9.6 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations needs to be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance. In this configuration the DPC, current measurement and overcurrent protection is not available.

9.6.1 System power supply overview

The PN76AC is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIOs (VDDIO)
2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)
3. Supply of the RF drivers (VDDPA) and TX_LDO (VUP)

The functionality of the GPIOs, Host Interface and internal analog and digital blocks is independent from the supply of the RF driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

Note: The voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in power-off mode.

Note: This product implements DC-DC in hardware however it is disabled in final product. DC-DC functionality can not be used however some supply connections are still necessary.

9.6.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors need to be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

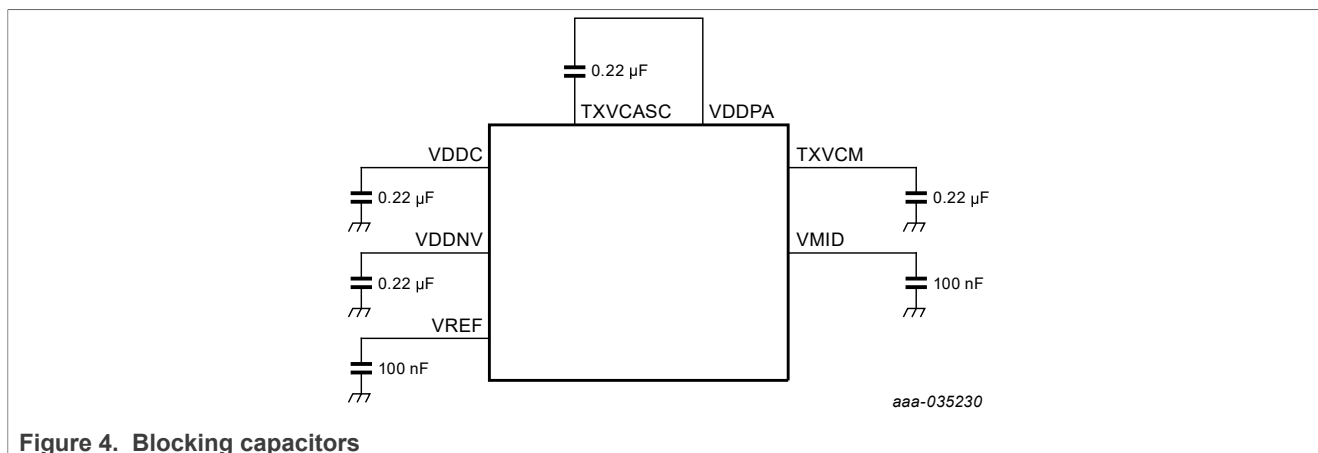


Figure 4. Blocking capacitors

9.6.3 Transmitter power supply

PN76AC is configured by EEPROM for the different power supply options.

The following EEPROM configurations are used to configure the power supply of the transmitter:

TXLDO_CONFIG (address 0x0002) - Enables/disables and configures the TX_LDO.

TXLDO_VDDPA_HIGH (0x0006) - initial out voltage when DPC is used.

TXLDO_VDDPA_LOW (0x0007) - lowest VDDPA when DPC is used.

TXLDO_VDDPA_MAX_RDR (0x0008) - maximum voltage to be set in reader mode used by DPC.

TXLDO_VDDPA_MAX_CARD (0x0009) - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

9.6.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

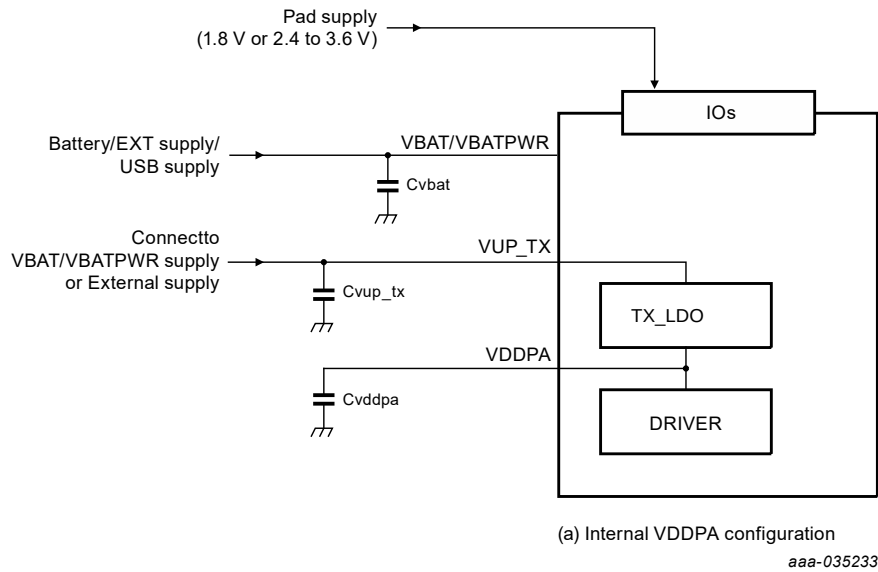


Figure 5. Transmitter supply

9.6.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBAPWR.

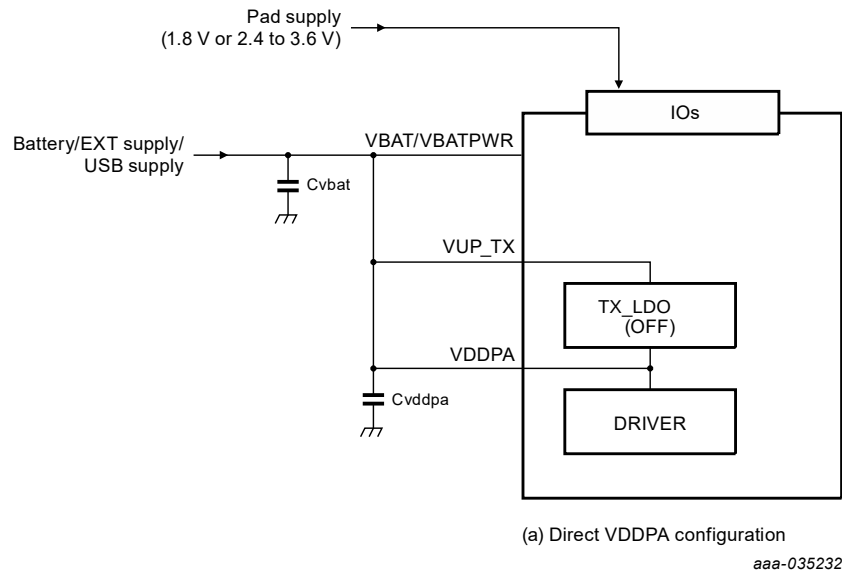


Figure 6. Direct transmitter supply

Note: With a direct transmitter supply, 0.3 V voltage drop from EXT battery supply is being avoided. This may be beneficial in battery operated devices. A clean power supply with low noise needs to be provided for optimum RF performance.

9.6.3.3 Configuration example 1: TX_LDO transmitter supply connected to VBAT

VBat is connected to VBAPWR and must be the same voltage level

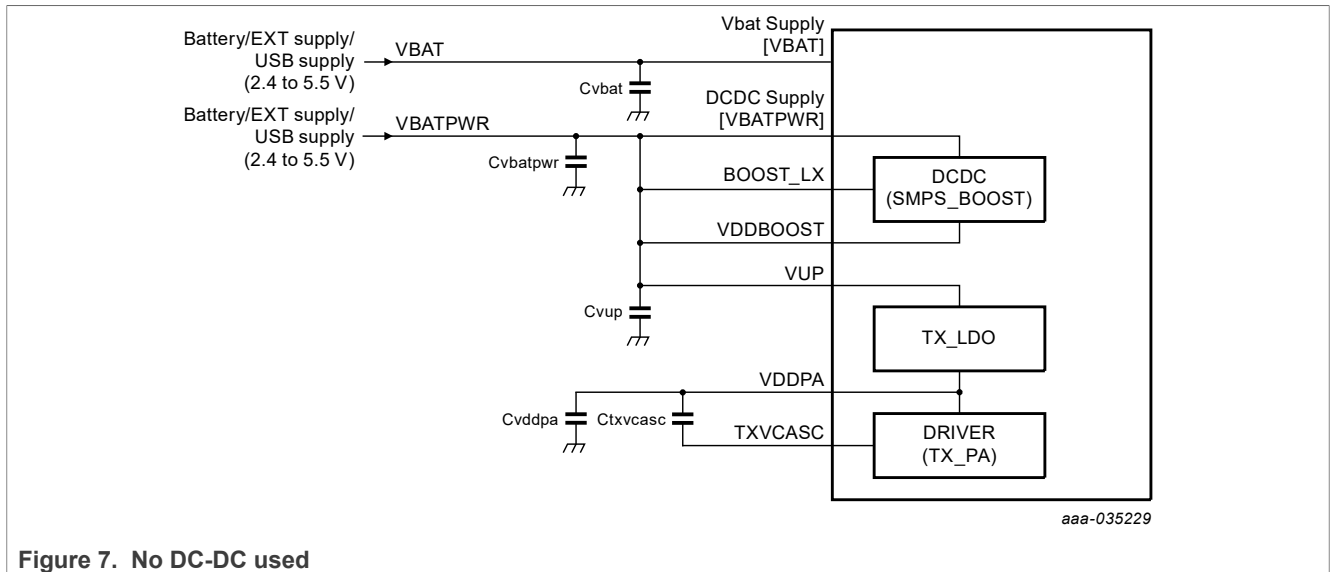


Figure 7. No DC-DC used

Note: DCDC (SMPS_BOOST) is disabled for PN76AC.

Note: Note: VBAT and VBAT_PWR should be routed as separate supply lines with separated block capacitors but connected to the same source.

9.6.3.4 Configuration example 2: TX_LDO supplied independent from VBAT

VBat is connected to VBATPWR and must be the same voltage level

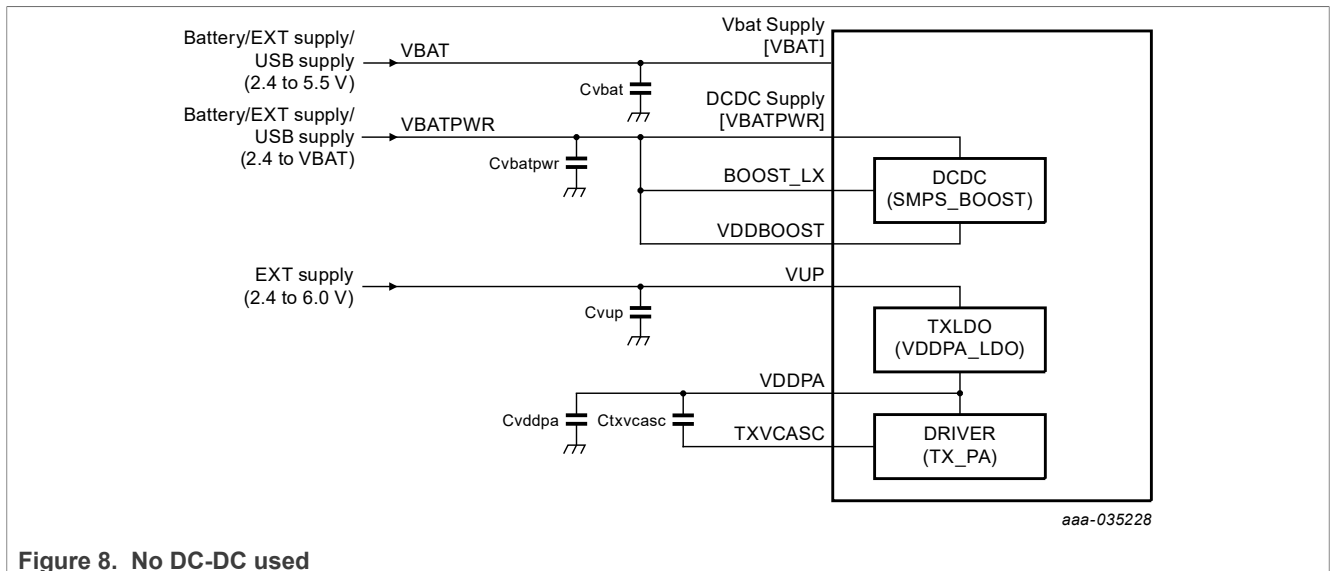


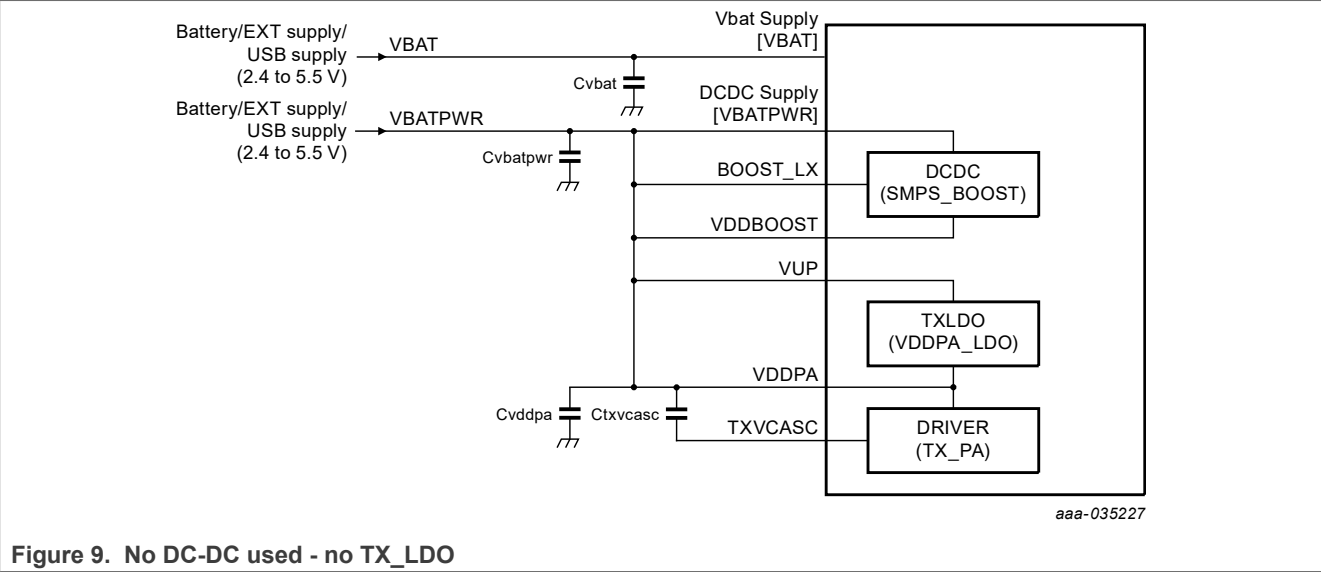
Figure 8. No DC-DC used

Note: DCDC (SMPS_BOOST) is disabled for PN76AC.

Note: Note: VBAT and VBAT_PWR should be routed as separate supply lines with separated block capacitors but connected to the same source.

9.6.3.5 Configuration example 3: TX_LDO not used

VBat is connected to VBATPWR and must be the same voltage level



Note: DCDC (SMPS_BOOST) is disabled for PN76AC.

9.6.3.6 Supply voltage range for transmitter supply configuration examples

Table 5. Supply voltage range configuration

Supply	Config1: TX_LDO transmitter supply connected to VBAT	Config2: TX_LDO supplied independent from VBAT	Config3: TX_LDO not used
EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (0x0076)			
TXLDO_VDDPA_ HIGH (0x0006)	0x0 (1.5 V)	0x0 (1.5 V)	NA
TXLDO_VDDPA_ MAX_RDR (0x0008)	0x2A (5.7 V)	0x2A (5.7 V)	NA
EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (0x0076)			
TXLDO_VDDPA_ HIGH (0x0006)	0x0 (1.5 V)	0x0 (1.5 V)	0x0 (1.5 V)
TXLDO_VDDPA_ MAX_RDR (0x0008)	NA	NA	NA

Table 6. Supply voltage range

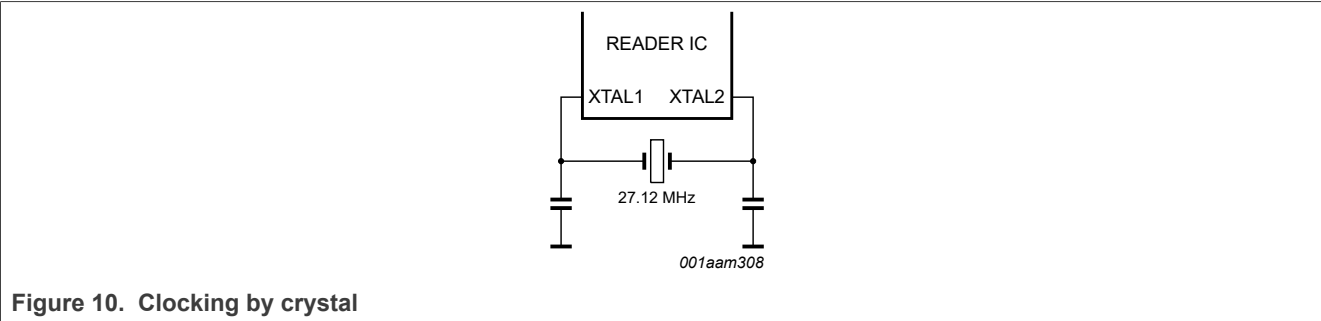
Supply	Config1: TX_LDO transmitter supply connected to VBAT	Config2: TX_LDO supplied independent from VBAT	Config3: TX_LDO not used
VBAT	2.4 V ... 5.5 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V
VBATPWR	2.4 V ... 5.5 V	2.4 V ... 5.5 V	2.4 V ... 5.5 V

Table 6. Supply voltage range...continued

Supply	Config1: TX_LDO transmitter supply connected to VBAT	Config2: TX_LDO supplied independent from VBAT	Config3: TX_LDO not used
VUP	2.4 V ... 5.5 V	2.4 V ... 6.0 V	2.4 V ... 5.5 V
VDDPA	VUP-0.3V drop of TX_LDO	VUP-0.3V drop of TX_LDO	2.4 V ... 5.5 V

9.7 Clock generation

The device supports the operation with crystal.
A high quality crystal with fast startup times will support a low current consumption during ULPCD mode.



9.8 External interfaces

PN76AC requires the connection of a power supply, a clock source like a crystal or external clock and a host microcontroller connected to NCI host interface for operation.
Additional connections of the package require the connection of stabilizing capacitors and ground.
The RF interface connects transmitter and receiver to the EMC filter of a connected antenna-matching network.

9.9 Transmitter overcurrent and temperature protection

The PN76AC implements different mechanisms to protect the chip against damages.
On the one hand, an overcurrent protection exists which shuts down the transmitter driver if there is a current exceeding the specification. This can be enabled in EEPROM "TXLDO_CONFIG (0x0002)", bit 11: overcurrent enable (0: disable, 1: enable).
An NCI notification is used to indicate the shut-down of the transmitter driver to a connected host.
On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM "TEMP_WARNING (0x0648)". Three temperatures can be configured: 114 °C, 125 °C, 130 °C.
An NCI notification is used to indicate this temperature warning to a connected host.
The actual measured temperature is available in the register "TEMP_SENSOR (0x005B)". The chip will go into standby immediately.
This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

9.10 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong near to the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (for example, NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to the detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC configuration data is stored in EEPROM, so that it is used after startup. This avoids the host to configure the chip after each reset or power off.

The following EEPROM configurations are most relevant for the DPC configuration:

DPC_Config: Enables/Disables the DPC (enable: 0x39, disable: 0x00)

DPC_TargetCurrent: Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC_TARGET_CURRENT is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.

DPC_Hysteresis: Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

DPC_Lookup_Table: configures the current reduction

The DPC_LOOKUP_TABLE allows, in addition to the limitation of the current, to configure:

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10 % and ASK100 % modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function than the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM_RSSI

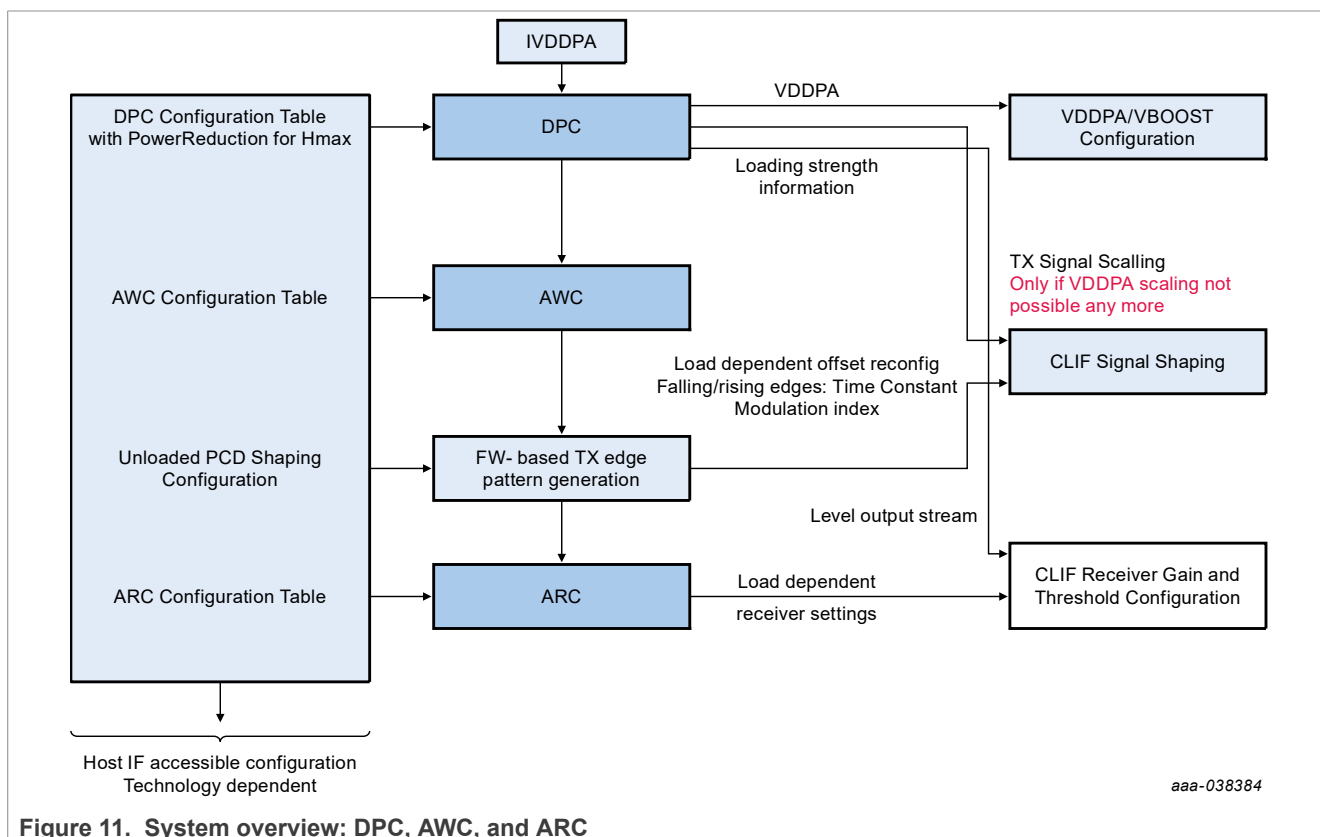
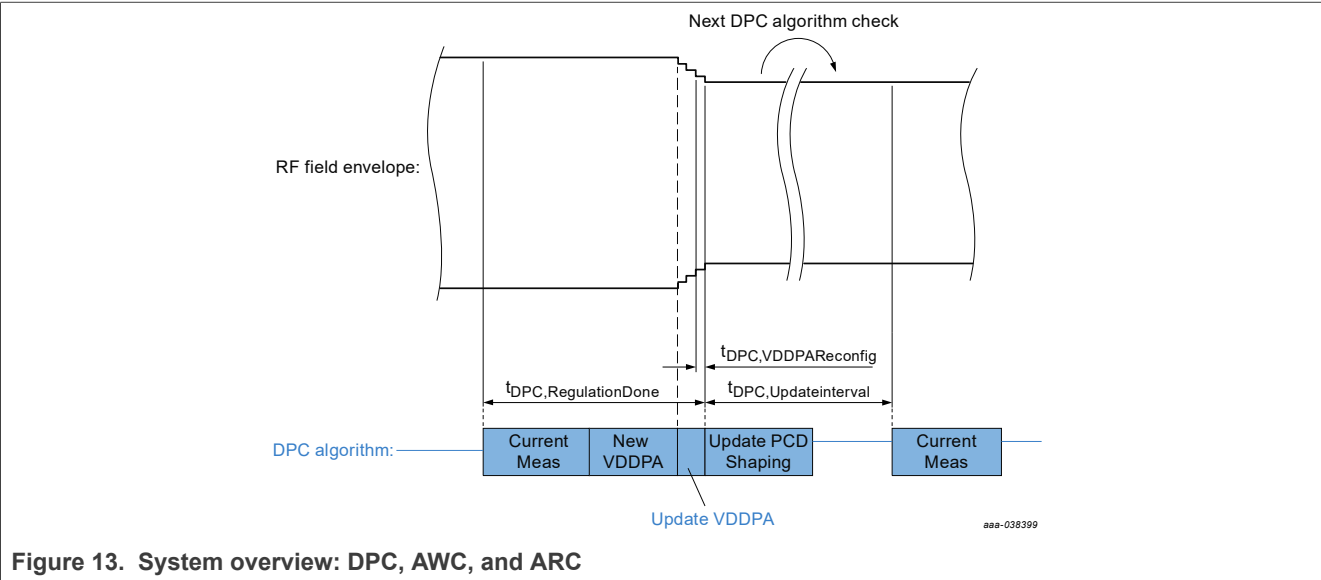
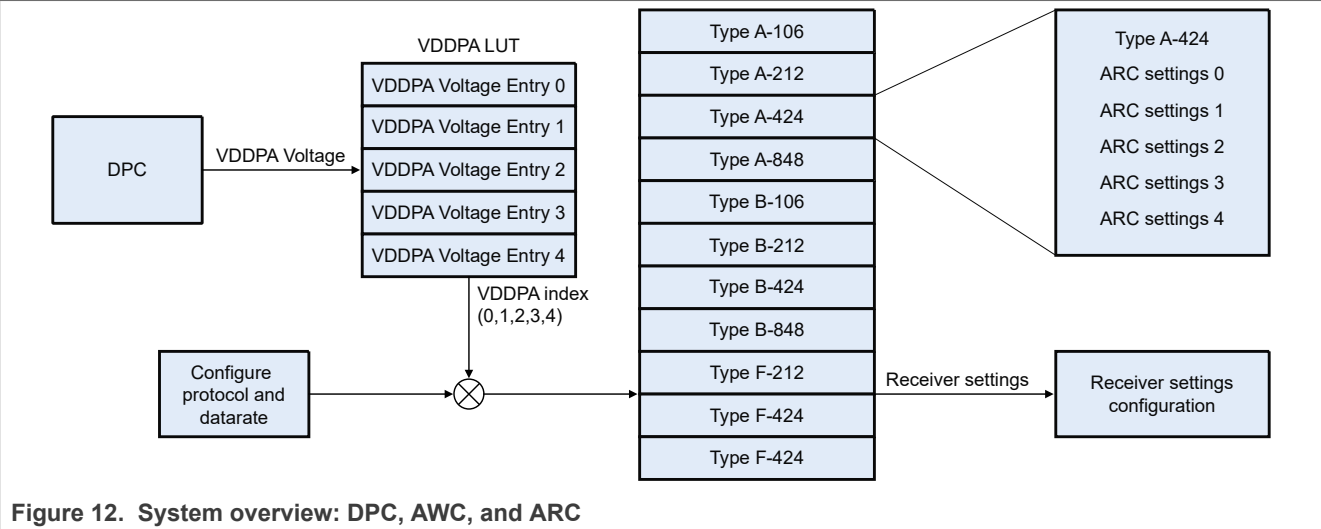


Figure 11. System overview: DPC, AWC, and ARC



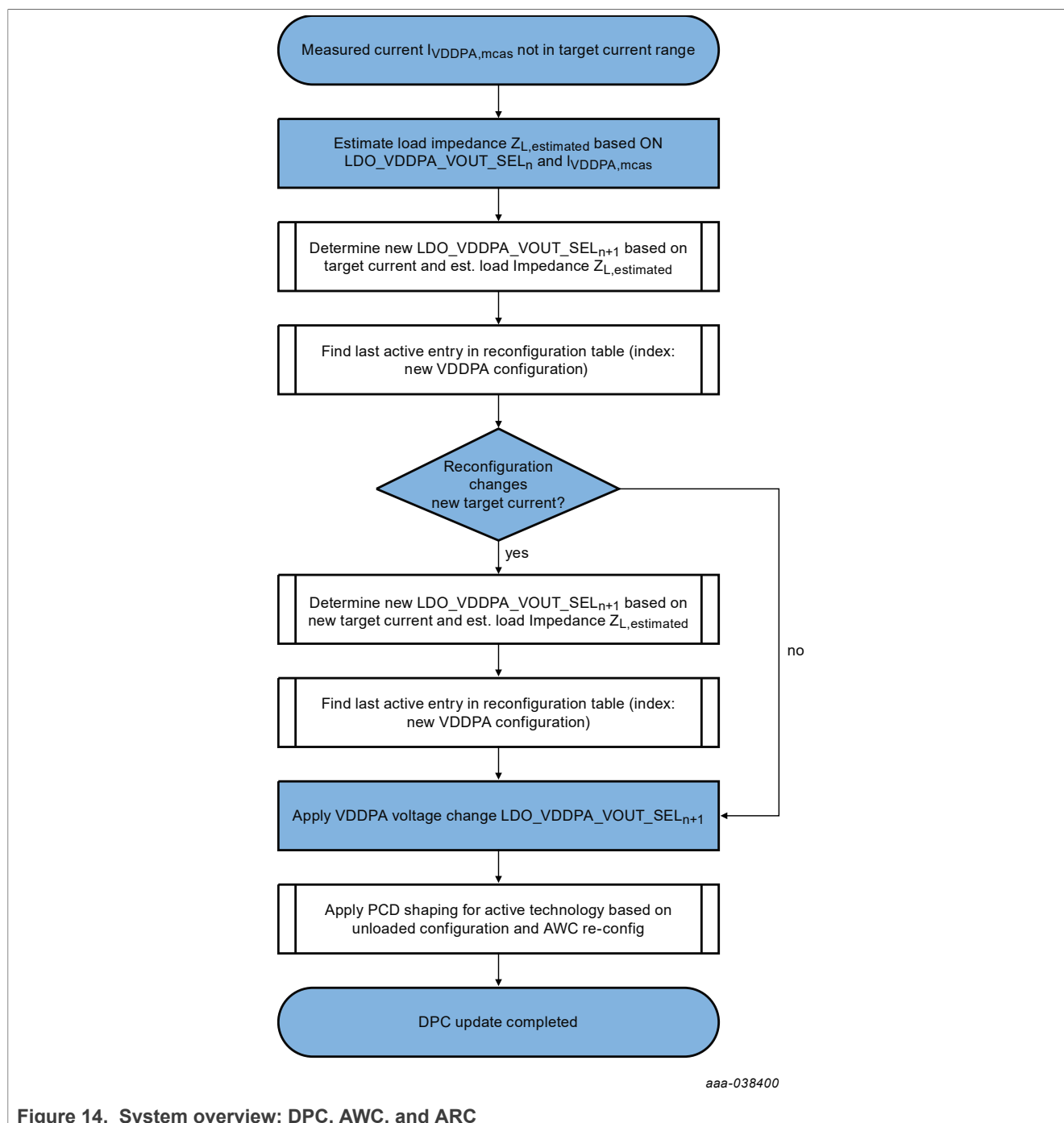


Figure 14. System overview: DPC, AWC, and ARC

9.10.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current

$$\text{VDDPA New (for target current of } I_{\text{target}}) = \text{VDDPA Voltage} / \text{VDDPA current} * I_{\text{target}}$$
3. Update VDDPA: Perform output power update

4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for a short duration

The reconfiguration table includes relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration after Field ON:

VDDPA max set to 42 (5.7 V) · Target current set to 280 mA

Technology B106: amp_mod = 200

Falling edge time constant = rising edge time constant = 3

Table 7. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage

Function	Bit	Description
ENTRY 0	31:0	This is the entry for 1.5 V.
Target current reduction	31:23	ENTRY 0 -LSB - byte 0 Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7 Bits[7:0] = Target current reduction in mA (unsigned)
AWC amp mod change	23:16	ENTRY 0 - byte 1 Bits[7:0] = Relative change of modulated amplitude level (signed)
AWC edge time constant for ASK100	15:8	ENTRY 0 - byte 2 Bits[3:0] = ASK100, Relative change of falling edge time constant (signed) Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)
AWC falling edge time constant for ASK10	7:0	ENTRY 0 -MSB - byte 4 Bits[3:0] = ASK10, Relative change of falling edge time constant (signed) Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

9.11 Adaptive waveshape control (AWC)

Depending on the level of detected detuning of the antenna, waveshaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. firmware-based shaping (1,2,3)
2. lookup-table-based shaping (4,5,6)

The firmware-based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup-table-based shaping allows maximum flexibility and enables to configure almost any possible correction.

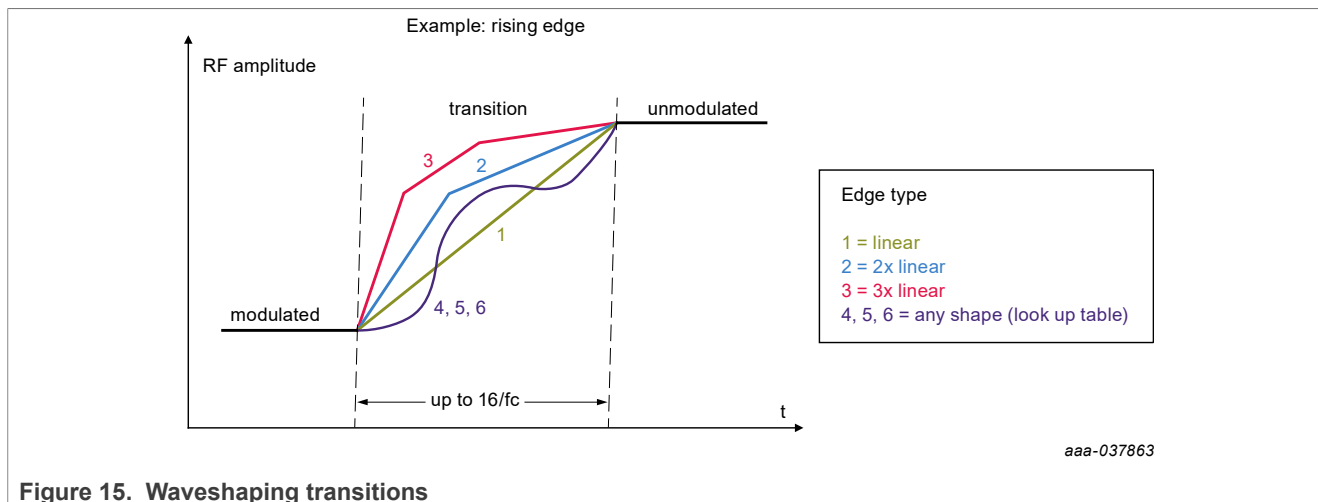


Figure 15. Waveshaping transitions

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated waveshaping configuration for the corresponding detuning condition but it also allows to configure the waveshaping individually dependent on the actual active protocol.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to the detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability

The device supports the design of compliant antennas by allowing to actively shape the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels
2. Two linear transitions between amplitude levels and
3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers `EDGE_TYPE_(protocol)`. It can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers `EDGE_STYLE_(protocol)` define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers `EDGE_LENGTH_(protocol)` define the total length of the edge pattern.

[Figure 16](#) to [Figure 18](#) illustrate the edge type for the falling edge.

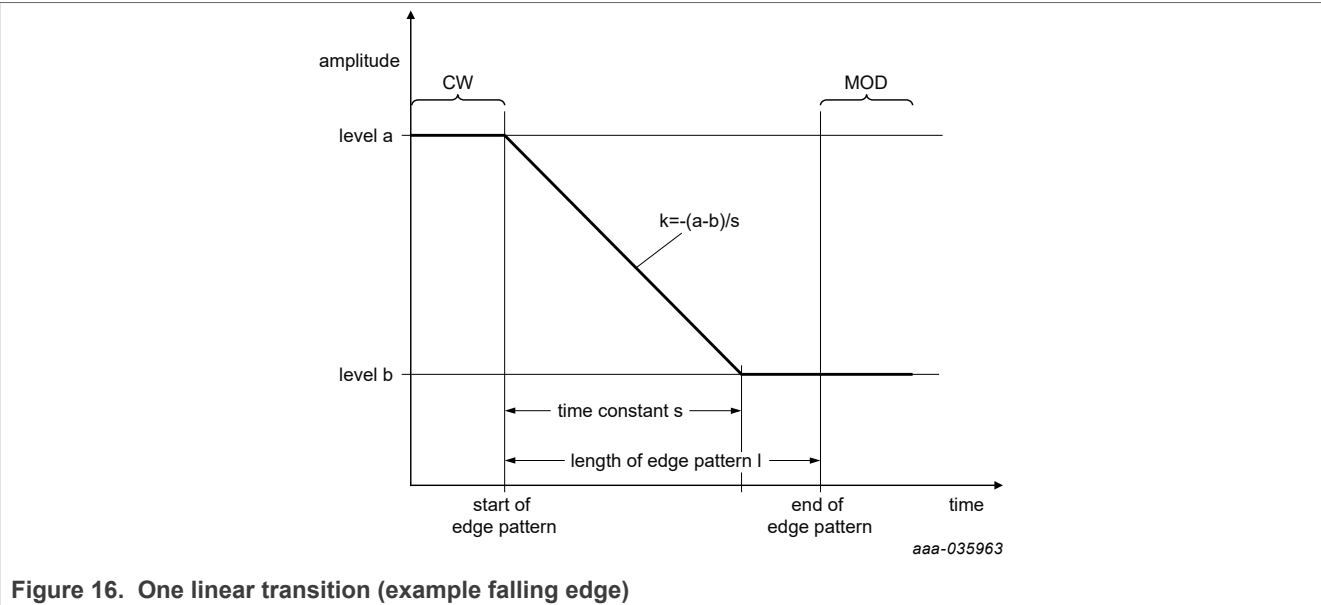


Figure 16. One linear transition (example falling edge)

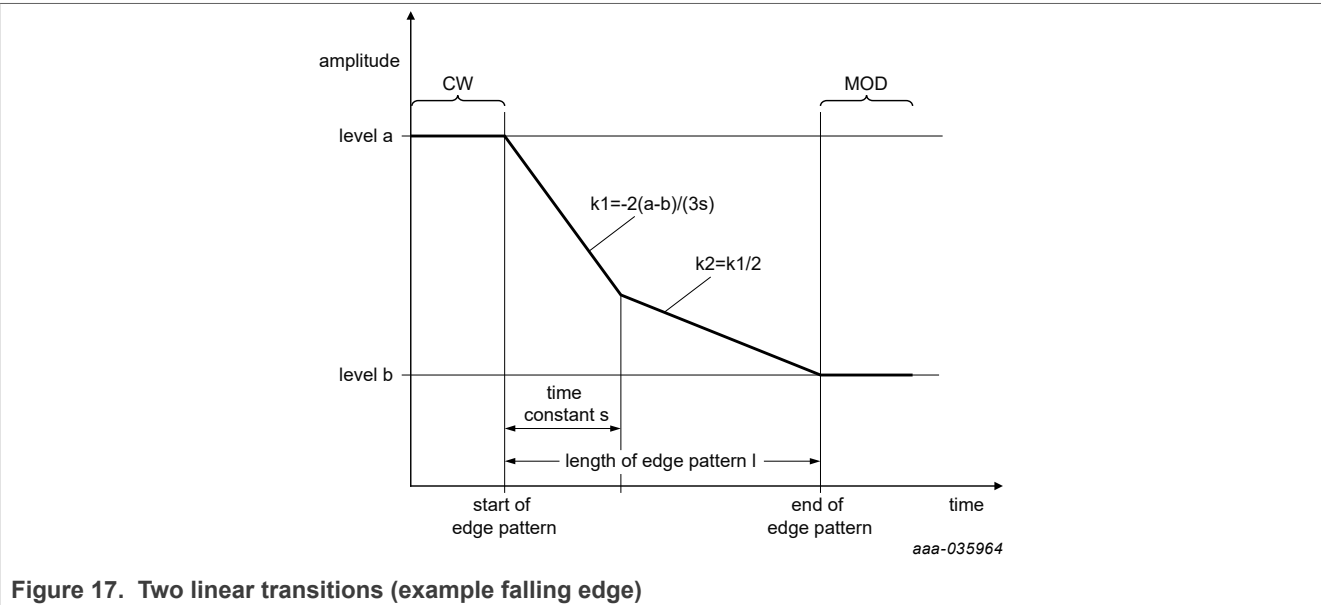
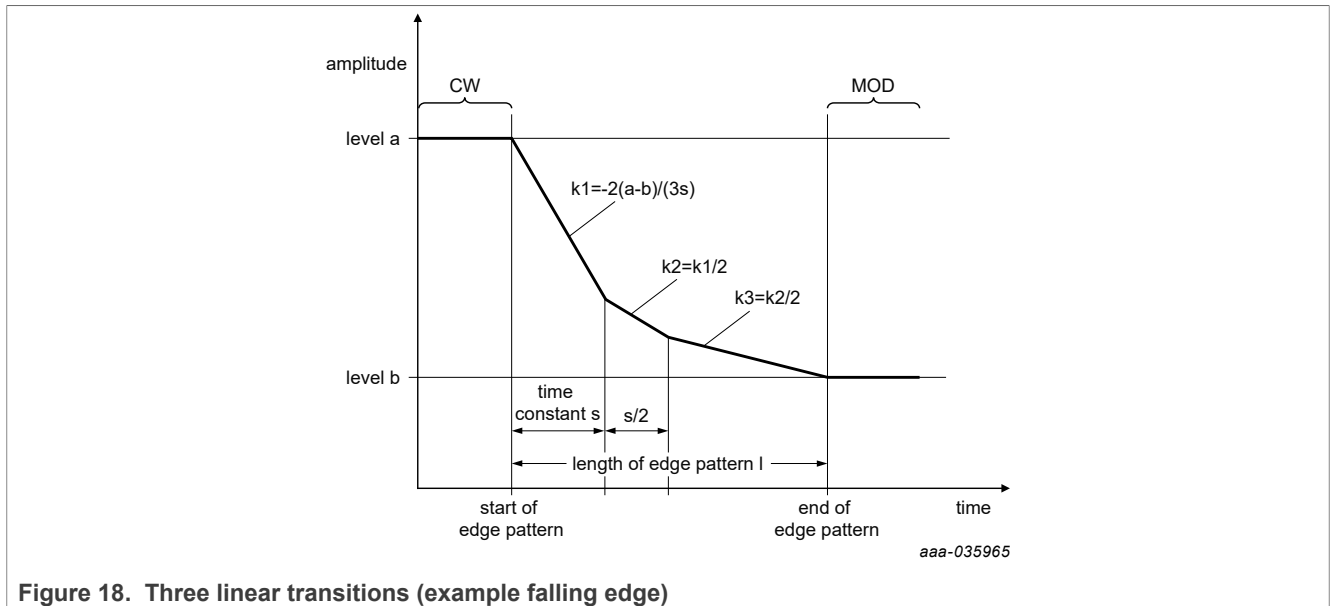


Figure 17. Two linear transitions (example falling edge)



The transition patterns are used as implicit predistortion to compensate effects of TX loading circuitry (for example, resonant circuitry parameters) to the emitted RF envelope.

9.12 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG (0x30) → DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG (0x22) → RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION (0x0D).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

VDDPA lookup table:

VDDPA lookup table defines a maximum of five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

Table 8. ARC_VDDPA EEPROM configuration bit description

Function	Bit	Description
ARC VDDPA Setting	7:0	Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4
	7:0	Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3
	7:0	Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2
	7:0	Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1

Table 8. ARC_VDDPA EEPROM configuration bit description...continued

Function	Bit	Description
	7:0	Byte[0] = ARC_VDDPA_0: $1.5 > VDDPA < ARC_VDDPA_0$

ARC lookup table:

VDDPA index and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. The ARC algorithm selects one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Following table shows ARC settings for Type A-106.

Table 9. ARC_RM_A106 EEPROM configuration bit description

Function	Bit	Description
RM_RX_ARC_4	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = <i>MF_GAIN</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled) Bits[6:0] = <i>DPC_SIGNAL_DETECT_TH_OVR_VAL</i> (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_3	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = <i>MF_GAIN</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled) Bits[6:0] = <i>DPC_SIGNAL_DETECT_TH_OVR_VAL</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled)
RM_RX_ARC_2	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = <i>MF_GAIN</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled) Bits[6:0] = <i>DPC_SIGNAL_DETECT_TH_OVR_VAL</i> (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)
RM_RX_ARC_1	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT, Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = <i>MF_GAIN</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled) Bits[6:0] = <i>DPC_SIGNAL_DETECT_TH_OVR_VAL</i> (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Table 9. ARC_RM_A106 EEPROM configuration bit description...continued

Function	Bit	Description
RM_RX_ARC_0	15:0	Bit[15] 0: ARC settings always apply 1: ARC settings applicable during FDT and DPC change Bits[14:10] = RFU Bit [9] = Enable the IIR filter. Bits[8:7] = <i>MF_GAIN</i> (this value will be applied to the SIGPR_RM_Tech register, applies as soon as the ARC is enabled) Bits[6:0] = <i>DPC_SIGNAL_DETECT_TH_OVR_VAL</i> (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)

Note: For ISO14443-A: In case ARC is disabled, it requires *DPC_SIGNAL_DETECT_TH_OVR_VAL* larger than 0x50 (with *MF_GAIN* = 2 (default))

Note: For ISO14443-A: In case Bit[15] is configured to 0, it requires *DPC_SIGNAL_DETECT_TH_OVR_VAL* larger than 0x50 (with *MF_GAIN* = 2 (default)) if the ARC is enabled.

9.13 Automatic EMD error handling

The PN76AC supports a configurable EMD handling according to the ISO14443 standard. To support further extensions or changes of these standards, the EMD block is configurable.

After being configured, the PN76AC restarts both the receiver and a timeout timer automatically without host interaction in case of a detected EMD event.

Features of the Automatic EMD Error Handling:

- No real-time constraints
- Less processing load on the host processor
- Configurable, anticipating future specification changes

9.14 Energy-saving card detection

Ultra low-power card detection (ULPCD) is an energy-saving card detection mode of PN76AC. A host microcontroller must set this power-saving mode on PN76AC.

A wake-up timer (ULFO) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse. The short pulse allows for the detection of a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode.

Trimming for the Ultra Low Frequency Timer is not required.

9.14.1 Ultra low-power card detection (ULPCD)

The ULPCD (ultra low-power card detection) offers the highest current saving. In this mode, the only wake-up sources are either a detected antenna detuning, a signal on **WKUP_REQ**, or a reset (VEN) of the PN76AC.

During ULPCD standby state, only the wake-up timer (ULFO) is active. It implies that the WKUP_REQ assertion is checked after the wake-up timer is elapsed.

The ULPCD comprises 2 phases:

1. Calibration phase

In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored as a reference value in a low-power persistent register.

2. Measurement phase

In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. The RSSI value is measured and compared against the reference value. When an object is in the proximity of the reader, the measured RSSI is compared against the reference RSSI and if this difference is more than a configured threshold, the object is detected.

9.15 RF level detection

PN76AC implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

RF Level Detector:

During ultra low-power card detection (ULPCD), a specific ultra low-power RF level detector is used as RF level detector(RFLD). This can be enabled as a wake-up source.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN76AC from power-saving mode.

NFC Level Detector:

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

9.16 Antenna connection

The PN76AC allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.

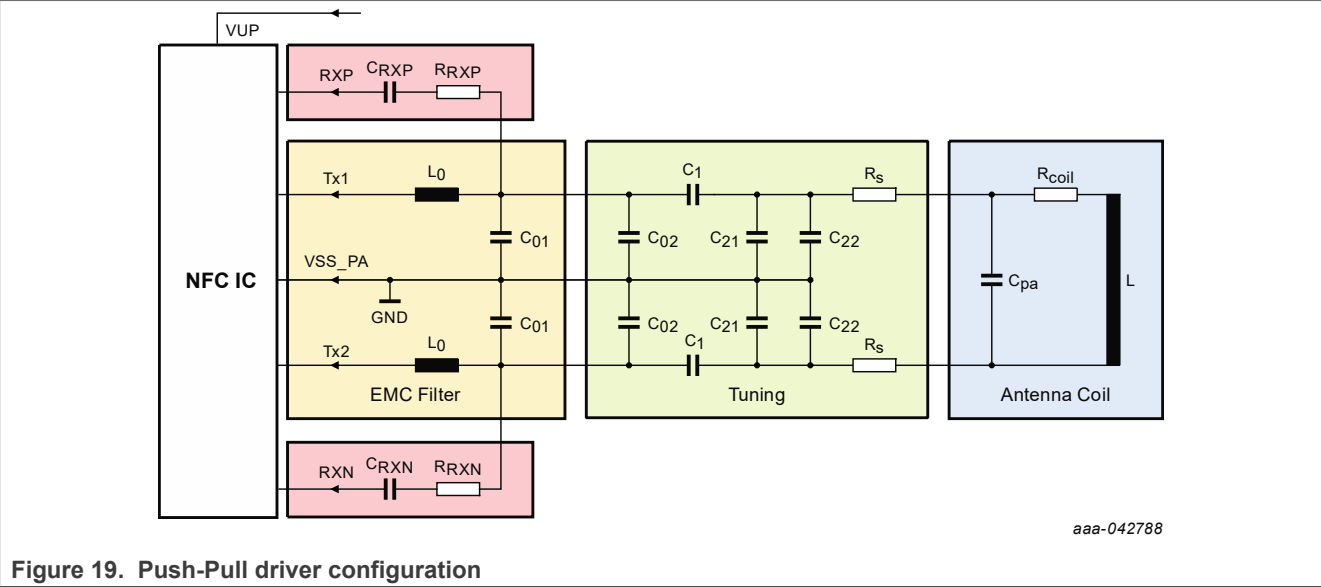


Figure 19. Push-Pull driver configuration

The PN76AC allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

Note: The RSSI target for SE must be calculated as follows and differs from the differential antenna:

$$RSSI\ target = Target\ RX\ Peak\ Voltage * 1024 / (1.8 * 2)$$

Example: For a 1.2 V target: $DGRM_RSSI_TARGET = 1.2 * 1024 / (1.8 * 2) = 341d = 0x155$

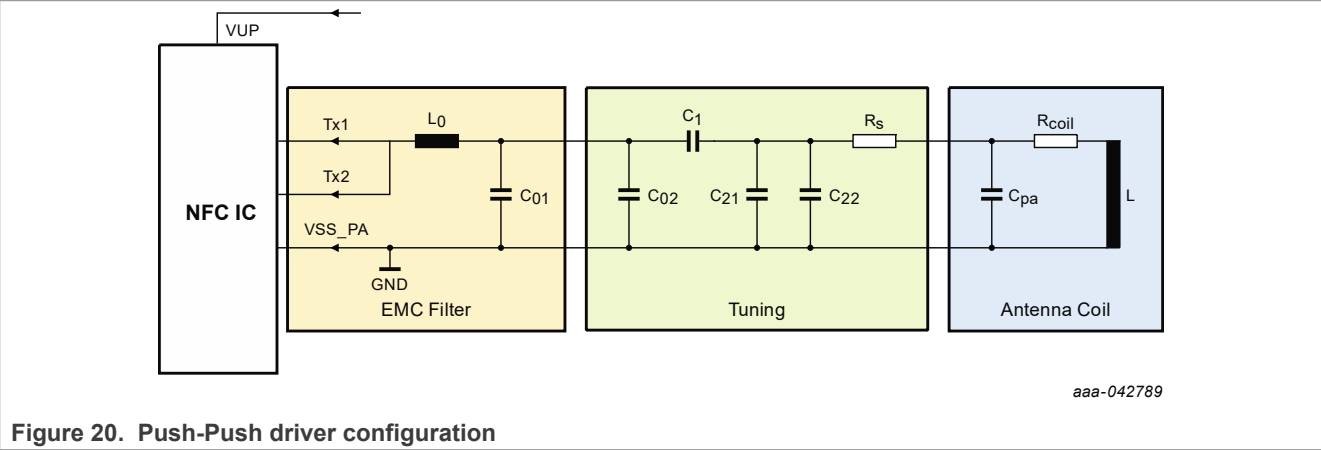


Figure 20. Push-Push driver configuration

Table 10. Antenna register configuration

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
SS_TX_CFG (0x15)	TX2_USE_TX1_CONF	1b	1b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_TRANS_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_MOD_RM	111b	111b
SS_TX1_RMCFG (0x16)	TX1_CLK_MODE_CW_RM	111b	111b

Table 10. Antenna register configuration...continued

Register (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_TRANS_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_MOD_RM	do not care	do not care
SS_TX2_RMCFG (0x17)	TX2_CLK_MODE_CW_RM	do not care	do not care
DGRM_RSSI (0x30)	DGRM_RSSI_TARGET	direct entry	as per calculation for SE (RSSI target = Target RX Peak Voltage*1024/ (1.8*2))
ANA_RX_CTRL (0x43)	RX_MIXER_SE_MODE_EN	0	1
ANACTRL_TX_CONFIG (0x44)	TX_INVP_RM	10b	00b
ANACTRL_TX_CONFIG (0x44)	TX_PWM_MODE_RM	0b	0b

Table 11. Antenna EEPROM configuration

EEPROM (Address)	Bit	Differential Antenna Push-Pull driver TX1, TX2	Single-Ended Push-Push driver TX1, TX2
TX_SHAPING_CONFIG (0x17)	0	0	0

Note: Recommendation is to use all the settings configured in EEPROM. For CLIF_SS_TX_CFG_REG, the value has to be configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.

9.17 RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by calling a respective system service API provided by PN76AC.

The system service APIs provide configuring the either digital or analog output to configure the dedicated signal on an output pin.

If used, **ADC-Q needs to be routed always to AUX1, ADC-I needs to be routed always to AUX2.**

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):

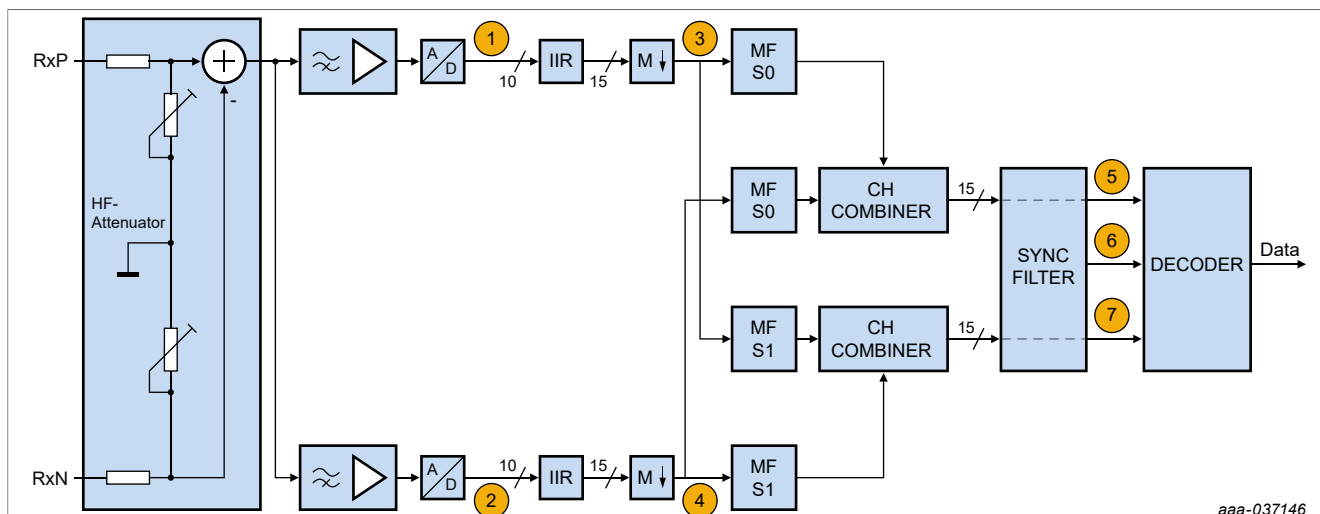


Figure 21. Receiver block diagram

Table 12. Debug signals

Signal	REGISTER	SIGNAL NAME	BITS	Description
ADC Data I Channel (1)	obs_clif_tbcontrol_patchbox0	adc_data_i_i	9:2	Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox1		9; 6:0	Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)
ADC Data Q Channel (2)	obs_clif_tbcontrol_patchbox2	adc_data_q_i	9:2	Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
	obs_clif_tbcontrol_patchbox3		9; 6:0	Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)
Preprocessor Out I Channel (3)	obs_clif_sigpro_rm0	rm_cor_adc_i_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm1		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling
Preprocessor Out Q Channel (4)	obs_clif_sigpro_rm2	rm_cor_adc_q_o	14:8	Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU
	obs_clif_sigpro_rm3		7:0	Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling
Output MF S0 (5)	obs_clif_sigpro_rm4	mf_pt_s0_d	14:8	Delayed matched filter S0 output, after CH combiner

Table 12. Debug signals...continued

Signal	REGISTER	SIGNAL NAME	BITS	Description
				upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm5		7:0	Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner
Output MF S1 (6)	obs_clif_sigpro_rm6	mf_pt_s1_d	14:8	Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106
	obs_clif_sigpro_rm7		7:0	Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106
Output Synchronization Filter (7)	obs_clif_sigpro_rm8	sync_filt_out	14:8	Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)
	obs_clif_sigpro_rm9		7:0	Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output
clif_status	transceive_state		7:5	
	rx_cl_error		4	
	tx_envelope		3	
	rx_enevelope		2	
	svalid		1	
	sdata		0	
clif_transceive	rx_start_receive		7	
	rx_over_ok		6	
	rx_over_term		5	
	rx_resume		4	
	sgp_msg_busy		3	
	fig_reset_sigpro		2	
	fig_reset_rxdec		1	
	cfg_sw_reset_sigpro		0	

Table 13. Trigger signals

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
TX Active	obs_clif_txenc1	tx_active_o	1	high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission.

Table 13. Trigger signals...continued

TRIGGER	REGISTER	SIGNAL NAME	BITS	Description
RX Enable	obs_clif_sigpro_rm15	rx_enable_o	1	high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception
RX collision detected	obs_clif_sigpro_rm14	rm_scoll_o	1	high-level pulse indicates that the collision is detected during reception

9.18 Polling loop

The polling loop and related configuration are described in the user manual.

10 Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}(VUP_TX)$	supply voltage on pin VUP_TX	-	-0.3	6.3	V
$V_{DD}(VBAT)$	supply voltage on pin VBAT	-	-0.3	5.8	V
$V_{DD}(VDDIO)$	supply voltage on pin VDDIO	on pin VDDIO, power supply for host interface and GPIOs	-0.3	3.8	V
$V_{DD}(GPIO_x)$	input voltage on pin used as GPIO	-	-0.3	3.8	V
$V_{DD}(VDDPA)$	supply voltage on pin VDDPA	maximum limiting values for $I_{DD}(VDDPA)$ and $T_{j(max)}$ not violated	-	6.0	V
$V_{i(RXP)}$	input voltage on pin RXP	-	-0.3	+ 2.0	V
$V_{i(RXN)}$	input voltage on pin RXN	-	-0.3	+ 2.0	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM) ^[1]	-2000	2000	V
		charge device model (CDM) ^[2]	-500	+500	V
$T_{j(max)}$	junction temperature	-	-	125	°C
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C

[1] According to ANSI/ESDA/JEDEC JS-001

[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime. The product might not behave according to specification.

11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

11.1 Static characteristics

Table 15. Supply voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT_PWR)}$	supply voltage on pin VBAT_PWR	DC-DC disabled	2.4	-	5.5	V
$V_{DD(VUP_TX)}$	supply voltage on pin VUP_TX (TX_LDO input pin)	-	2.4	-	6.0	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA (input of the transmitter power amplifier)	-	1.5	-	5.7	V
$V_{DD(VDDPA)}$	supply voltage on pin VDDPA		2.4	-	4.7	V
$V_{DD(VBAT)}$	supply voltage on pin VBAT (analog and digital supply)	$VBAT \geq VDDIO$	2.4	-	5.5	V
$V_{DD(VDDIO)}$	supply voltage on pin VDDIO (supply for host interface and GPIOs)	typical 1.8 V interface supply voltage	1.62	-	1.98	V
		typical 3.3 V interface supply voltage	2.4	-	3.6	V
$V_{I(RXP)}$	input voltage on pin RXP	-	-0.5	-	1.8	V
$V_{I(RXN)}$	input voltage on pin RXN	-	-0.5	-	1.8	V

Note: The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.

Note: $V_{DD(VBAT_PWR)}$ needs to be connected to $V_{DD(VBAT)}$

Table 16. Current consumption in active mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(VBAT)}$	system supply		-	-	20	mA
$I_{DD(VDDIO)}$		This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)} \text{ max}$	-	-	30	mA
$I_{DD(VUP_TX)}$	input supply for transmitter LDO	-	-	-	350	mA
$I_{DD(VDDPA)}$	RF power amplifier (transmitter) current	supplied via VUP_TX (TX_LDO active)	-	-	350	mA

Table 17. Current consumption during power-saving modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{\text{OFF Plus Mode (VDDIO+VBAT)}}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode	25 °C ambient operating temperature	-	5	-	μA
$I_{\text{OFF Plus ULFO Mode (VDDIO+VBAT)}}$	sum of supply current on pin VDDIO and VBAT in OFF Plus mode, ULFO active (ULPCD during RF-OFF)	25 °C ambient operating temperature	-	5	-	μA
$I_{\text{hard power down (VDDIO+VBAT)}}$	sum of supply current on pin VDDIO and VBAT in hard Power-down mode	25 °C ambient operating temperature	-	40	105	μA
$I_{\text{standby (VDDIO+VBAT)}}$	sum of supply current on pin VDDIO and VBAT in Standby mode	25 °C ambient operating temperature	-	45	110	μA
$I_{\text{suspend (VBAT)}}$	supply current on pin VBAT in suspend mode	25 °C ambient operating temperature	-	2.5	-	mA
$I_{\text{ULPCD (VDDIO+VBAT)}}$	sum of supply current on pin VDDIO and VBAT in ULPCD (Ultra Low-Power Card Detection) mode	25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second	-	22	-	μA

Table 18. Overcurrent detection function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{\text{DD(VUP_TX)}}$	current of overcurrent detection becoming active	-	450	550	650	mA

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 19. VEN pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{\text{DD(VDDIO)}} \leq V_{\text{DD(VBAT)}}$	0.7 * $V_{\text{DD(VDDIO)}}$	-	$V_{\text{DD(VDDIO)}}$	V
V_{IL}	LOW-level input voltage		0	-	0.3 * $V_{\text{DD(VDDIO)}}$	V
I_{IH}	HIGH-level input current	$V_{\text{I}} = V_{\text{DD(VBAT)}}$	-	-	1	μA
I_{IL}	LOW-level input current	$V_{\text{I}} = 0 \text{ V}$	-1	-	-	μA
C_{i}	input capacitance		-	5	-	pF
$t_{\text{(ULPCD_abort)}}$	VEN time required to abort ULPCD		5	-	-	ms

Table 20. CLK1, CLK2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{I(p-p)}$	peak-to-peak input voltage	-	0.4	-	1.65	V
I_{IH}	HIGH-level input current	$V_I = 1.65$ V, no power saving, active mode	-	-	5	μ A
I_{IL}	LOW-level input current	$V_I = 0$ V, no power saving, active mode	-	-	1	μ A
δ	duty cycle	-	35	-	65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	$V_{DD} = 1.8$ V, $V_{DC} = 0.65$ V, $V_{AC} = 0.9$ V (p-p)	-	1	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	$V_{DD} = 1.8$ V, $V_{DC} = 0.65$ V, $V_{AC} = 0.9$ V (p-p)	-	1	-	pF

Table 21. IRQ pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$I_{OH} < 3$ mA	$V_{DD(VDDIO)} - 0.4$	-	$V_{DD(VDDIO)}$	V
V_{OL}	LOW-level output voltage	$I_{OL} < 3$ mA	0	-	0.4	V
I_{OH}	HIGH-level output current		-	-	3	mA
I_{OL}	LOW-level output current		-	-	3	mA
C_L	load capacitance		-	-	10	pF
t_f	fall time	$C_L = 12$ pF max	1	-	3	ns
t_r	rise time	$C_L = 12$ pF max	1	-	3	ns
R_{pd}	pull-down resistance		40	-	62	k Ω

Table 22. SPI SCK / I2C1_SCL, SPI NSS / I2C address bit 0, SPI COTI / I2C address bit 1 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65 \times V_{DD(VDDIO)}$	-	$V_{DD(VDDIO)}$	V
V_{IL}	LOW-level input voltage		- 0.5	-	$0.35 \times V_{DD(VDDIO)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{VDDIO}$	-	-	1	μ A
I_{IL}	LOW-level input current	$V_I = 0$ V	-	-	1	μ A
C_i	input capacitance		-	5	-	pF

Table 23. I2C1_ SDA pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	I _{OH} < 3 mA	V _{DD(VDDIO)} - 0.4	-	V _{DD(VDDIO)}	V
V _{OL}	LOW-level output voltage	I _{OL} < 3 mA	0	-	0.4	V
I _{OH}	HIGH-level output current		-	-	3	mA
I _{OL}	LOW-level output current		-	-	3	mA
C _L	load capacitance		-	-	10	pF
t _f	fall time	C _L = 12 pF max	1	-	3	ns
t _r	rise time	C _L = 12 pF max	1	-	3	ns

Table 24. Mode selection, HOST_IF_SEL0, HOST_IF_SEL1, WAKEUP pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	HIGH-level input voltage	V _{DD(VDDIO)} ≤ V _{DD(VBAT)} ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6	0.65 × VDDIO	-	VDDIO + 0.5 V	V
V _{IL}	LOW-level input voltage	V _{DD(VDDIO)} ≤ V _{DD(VBAT)} ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6	- 0.5	-	0.35 × VDDIO	V
V _{OH}	HIGH-level output voltage	V _{DD(VDDIO)} = 3.3 V	VDDIO - 0.4	-	VDDIO	V
V _{OL}	LOW-level output voltage	V _{DD(VDDIO)} = 3.3 V	0	-	0.4	V
I _{OH}	HIGH-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{OL}	LOW-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{IH}	HIGH-level input current	V _{DD(VDDIO)} = 3.3 V	-	-	1	μA
I _{IL}	LOW-level input current	V _{DD(VDDIO)} = 3.3 V	-	-	1	μA
R _{PU}	Weak pullup resistor	-	40	50	62	kΩ
R _{PD}	Weak pulldown resistor	-	40	50	62	kΩ

Table 25. RXp, RXn pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{i(dyn)}	dynamic input voltage		-	-	1.8	V
C _i	input capacitance		-	1	-	pF
Z _i	input impedance from RXN, RXP pins to VMID	Reader, card, and P2P modes	-	-	15	kΩ

Table 26. TX1, TX2 pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _{DD(VDDPA)} =5.0 V; with internal VDDPA LDO	-	V _{DD(VDDPA)} -150 mV	V _{DD(VDDPA)}	V
V _{OL}	LOW-level output voltage	V _{DD(VDDPA)} =5.0 V; with internal VDDPA LDO	0	200	-	mV

Table 27. AUX1, AUX2 pins (Debug output)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{AUX_OH}	HIGH-level output voltage	pin used as debug signal output	VDDIO - 0.4	-	VDDIO	V
V _{AUX_OL}	LOW-level output voltage	pin used as debug signal output	0	-	0.4	V
I _{AUX_OH}	HIGH-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
I _{AUX_OL}	LOW-level output current	V _{DD(VDDIO)} = 3.3 V	-	-	3	mA
C _{O_LOAD}	output capacitance load of pin		-	5	10	pF

11.2 Timing characteristics

Table 28. Power supply connection timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{rise_vbat}	VBAT supply ramp	VEN = Low	2.5	-	5000	μs
t _{vbat_vddio}	time between ramping up VBAT and ramping VDDIO	VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	0	500	1000	ms
t _{boot}	start-up time ^[1]	VBAT > 2.4 V, VDDIO supply (External), hpd_off_sel = x	-	-	dependent on configuration of XTAL_CHECK_DELAY in EEPROM (see "XTAL_CHECK_DELAY (0x0012)" in UM12399 – PN76AC user manual). This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during ULPCD.	ms
t _{vddio_ven}	Startup sequence A: t _{vddio_ven} >= 25ms		25	-	-	ms

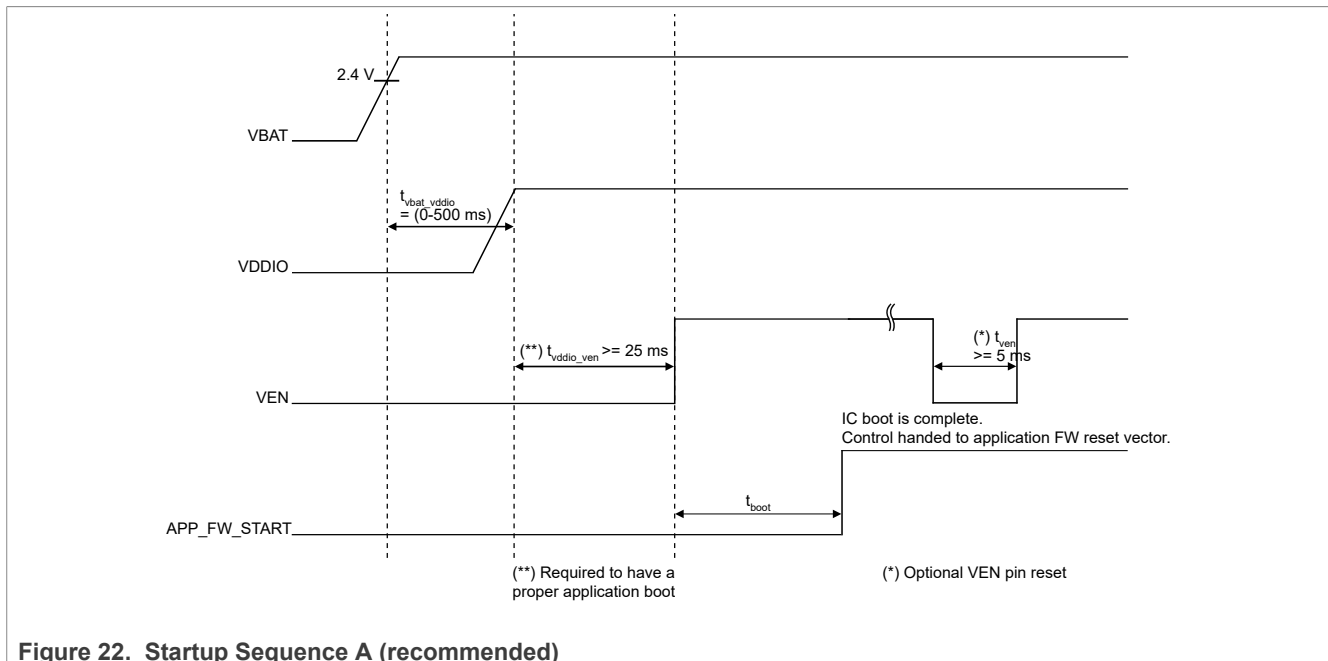
Table 28. Power supply connection timing ...continued

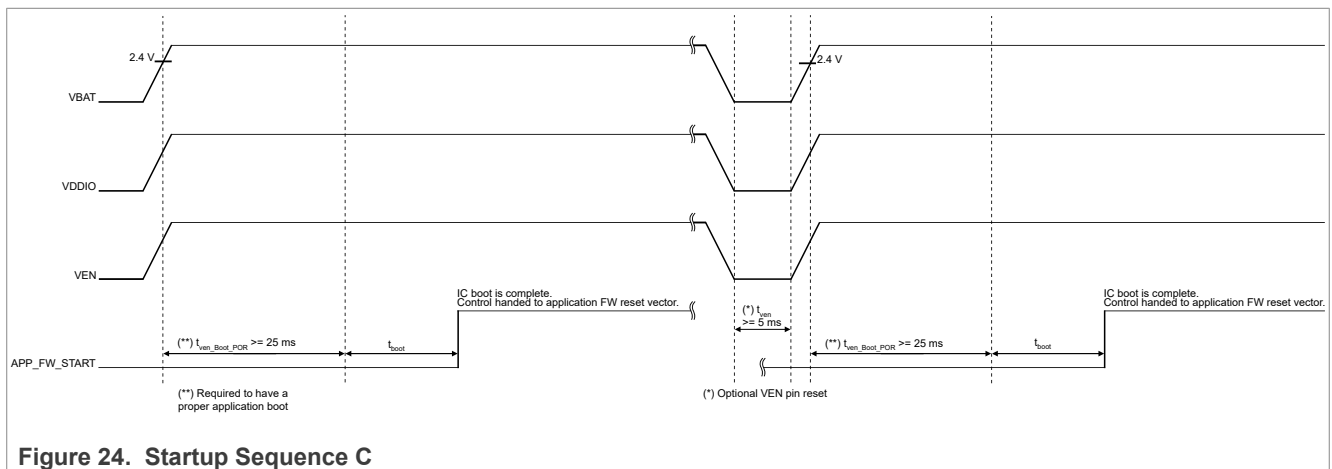
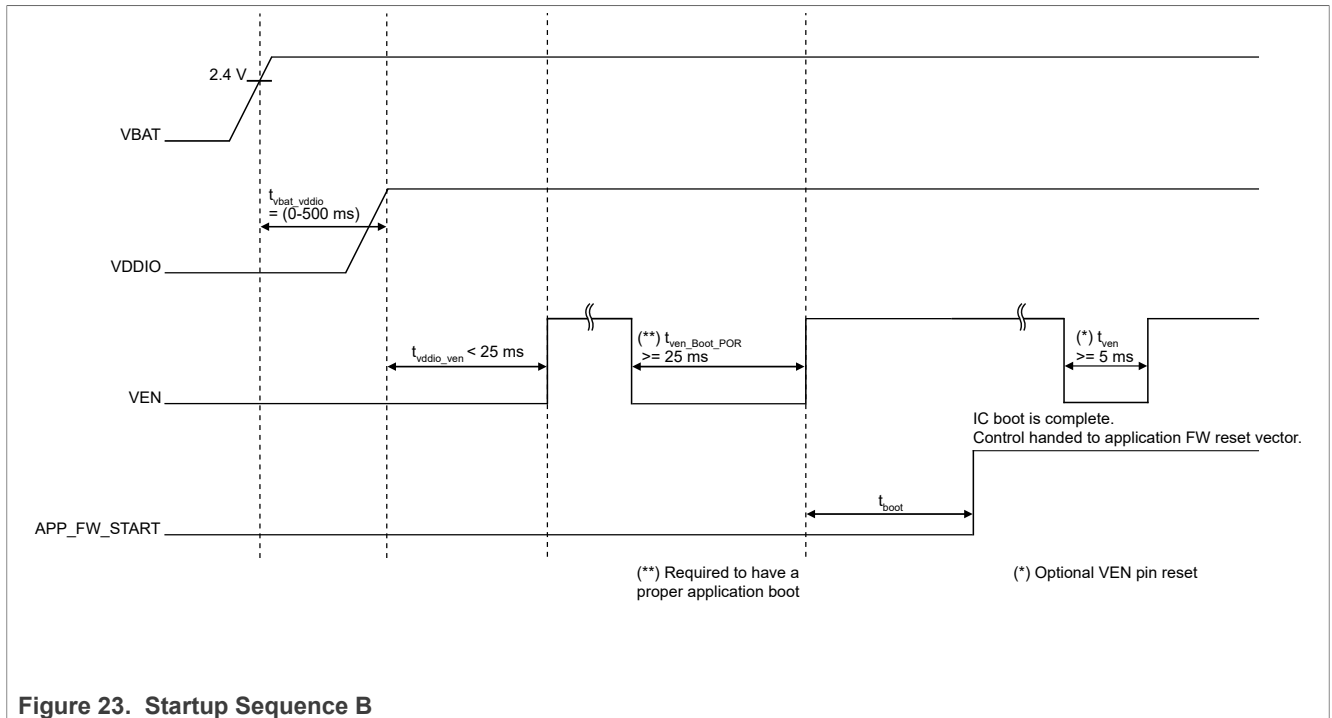
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	time from VDDIO HIGH TO VEN high					
	Startup sequence B: $t_{\text{vddio_ven}} < 25\text{ms}$ time from VDDIO HIGH TO VEN high		-	-	25	ms
	Startup sequence C: VBAT = VDDIO = VEN	A VBAT power cycle is required to reset the IC.	0	-	0	ms
$t_{\text{ven_Boot_POR}}$	if $t_{\text{vddio_ven}} < 25\text{ms}$ then VEN low pulse width for getting BOOT_POR	-	25	-	-	ms
t_{ven}	VEN pin low pulse width to reset	$t_{\text{vddio_ven}} \geq 5.5\text{ms}$	5	-	-	ms

[1] (PN76AC ready to receive commands on the host interface). For ULPCD, the PN76AC indicates the ability to receive commands from a host after raising an IDLE IRQ.

Note: Switching OFF VBAT during TX ON, might damage the IC - ensure to switch RF OFF before the power supply VBAT is disconnected

Note: For details on BOOT_POR refer to the User Manual.





Note: If VBAT = VDDIO = VEN (all connected together), then a VBAT power cycle is required to reset the IC.

Table 29. SPI interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	33.3	-	-	ns
t_{SCKH}	SCK HIGH time	33.3	-	-	ns
$t_h(SCKH-D)$	SCK HIGH to data input hold time	16.65	-	-	ns
$t_{su}(D-SCKH)$	data input to SCK HIGH set-up time	16.65	-	-	ns
$t_h(SCKL-Q)$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NTS HIGH time	0	-	-	ns
t_{NSSH}	NTS HIGH time	33.3	-	-	ns

Table 30. I²C timing specification: Standard, Fast Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	Load capacitance < 400 pF	0	-	0.4	MHz
t _{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t _{HD} START	hold time of a (repeated) START condition	Load capacitance < 400 pF	600	-	-	ns
t _{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 400 pF	1.3	-	-	μs
t _{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 400 pF	600	-	-	ns
t _{SU} DATA	DATA set-up time	Load capacitance < 400 pF	100	-	-	ns
t _{HD} DATA	DATA hold-up time	Load capacitance < 400 pF	0	-	900	ns
t _{rDA}	Rise time of SDA	Load capacitance < 400 pF	30	-	250	ns
t _{fDA}	Fall time of SDA	Load capacitance < 400 pF	30	-	250	ns

Table 31. I²C timing specification: High-Speed Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	3.4	MHz
t _{SU} START	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t _{HD} START	hold time of a (repeated) START condition	Load capacitance < 100 pF	160	-	-	ns
t _{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	160	-	-	ns

Table 31. I²C timing specification: High-Speed Mode...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	60	-	-	ns
t _{SU DATA}	DATA set-up time	Load capacitance < 100 pF	10	-	-	ns
t _{HD DATA}	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr _{DA}	Rise time of SDA	Load capacitance < 100 pF	10	-	80	ns
tf _{DA}	Fall time of SDA	Load capacitance < 100 pF	10	-	80	ns

Table 32. I²C timing specification: Fast + High-Speed-Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	Load capacitance < 100 pF	0	-	1	MHz
t _{SU START}	Set-up time for a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t _{HD START}	hold time of a (repeated) START condition	Load capacitance < 100 pF	260	-	-	ns
t _{LOW}	Timing of the LOW period of the SCL clock	Load capacitance < 100 pF	500	-	-	ns
t _{HIGH}	Timing of the HIGH period of the SCL clock	Load capacitance < 100 pF	260	-	-	ns
t _{SU DATA}	DATA set-up time	Load capacitance < 100 pF	50	-	-	ns
t _{HD DATA}	DATA hold-up time	Load capacitance < 100 pF	0	-	-	ns
tr _{DA}	Rise time of SDA	Load capacitance < 100 pF	-	-	120	ns

Table 32. I²C timing specification: Fast + High-Speed-Mode...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{fDA}	Fall time of SDA	Load capacitance < 100 pF	-	-	120	ns

11.3 Timing characteristics of host interface commands

TIMING OF VEN TRIGGERED BOOT

Table 33. Timing of VEN and command processing (HIF I2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{BOOT}	Boot time, chip initialization	VEN transition from L to H starts the chip initialization. During this time I2C commands/packets are not accepted and processed.	-	-	2.0	ms
t _{FW_DOWNLOAD_CMD}	Time after VEN transition from L to H, at which firmware download commands or a CoreReset command can be processed. A CoreResetCmd will abort the FW download mode immediately and switch to NCI command mode	After boot System waits for incoming packets for secure firmware update, FW download commands are accepted. The only standard NCI command accepted during this time is te CoreReset	2.0	-	4950	ms
t _{CMD_MODE_SWITCH}	Transition from FW download mode to NCI handling mode ,no NCI commands can be processed during this time	Time after VEN transition from L to H > 5000 ms and command is not received for FW download or Core Reset . Incase of FW download or Core Reset command received during t NCI_CMD, then tCMD_MODE_SWITCH is not available	3.0	-	5.0	ms
t _{NCI_CMD}	Time after tBoot, at which FW download or Core Reset command processed	After tBoot, Time window to process FW download command or Core Reset command	5105.0	-	-	ms

Table 34. Timing of VEN and command processing (HIF SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BOOT}	Boot time, chip initialization	VEN transition from L to H starts the chip initialization. During this time SPI commands/packets are not accepted and processed	-	-	2.0	ms
$t_{FW_DOWNLOAD_CMD}$	Time after VEN transition from L to H, at which firmware download commands can be processed	After boot System waits for incoming packets for secure firmware update, FW download commands are accepted	2.0	-	4950.0	ms
$t_{CMD_MODE_SWITCH}$	Duration to switch from secure firmware download command mode to NCI handling command mode	commands are not accepted	3.0	-	103.0	ms
t_{NCI_CMD}	Time after VEN transition L to H at which NCI commands can be processed	NCI commands are accepted	5105.0	-	-	ms

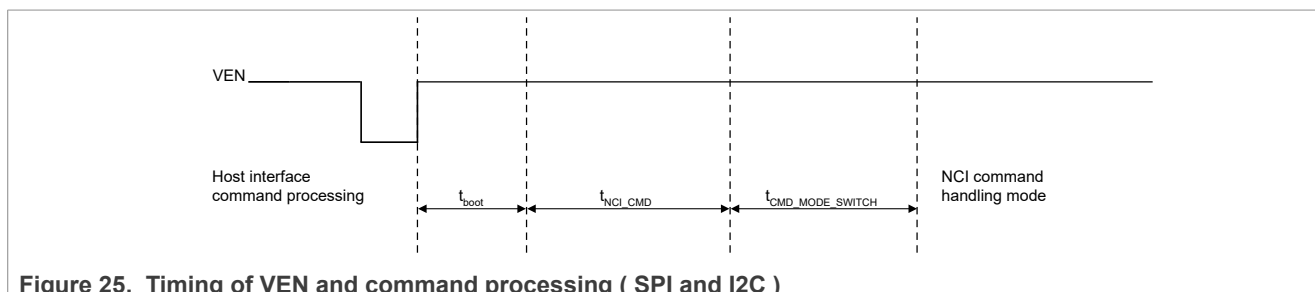


Figure 25. Timing of VEN and command processing (SPI and I2C)

t_{NCI_CMD} : the time during which a Firmware download command or core reset command is processed

- Any Firmware download command switches the host interface state to firmware download mode
- The core reset command switches the host interface state to NCI command handling mode

TIMING OF CORE RESET COMMAND TRIGGERED BY COLD BOOT

The core reset command can be used to shorten the time before the NCI commands are accepted.

Table 35. Timing of CORE RESET command after COLD RESET command (HIF I2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{NCI_CORE_RESET_IRQ_H}$	duration from NCI core reset in firmware download mode until NCI command processing is entered. Indicated by IRQ transition to H	NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and	-	-	6.4	ms

Table 36. Timing of CORE RESET command after COLD RESET command (HIF SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{NCI_CORE_RESET_IRQ_H}}$	duration from NCI core reset in firmware download mode until NCI command processing is entered, indicated by IRQ transition to H	NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and	-	-	6.4	ms

TIMING OF NCI CORE RESET COMMAND TRIGGERED BY WARM BOOT

Table 37. Timing of NCI CORE RESET command to NCI command mode (HIF I2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{NCI_CORE_RESET_IRQ_H}}$	duration from NCI core reset in NCI mode until NCI command processing is entered	NCI core reset command sent in NCI command mode	-	-	4.1	ms

Table 38. Timing of NCI CORE RESET to NCI command mode (HIF SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{NCI_CORE_RESET_IRQ_H}}$	duration from NCI core reset in NCI mode until NCI command processing is entered	NCI core reset command sent in NCI command mode on HIF1	-	-	4.1	ms

TIMING OF VEN TRIGGERED BOOT TO SECURE FIRMWARE DOWNLOAD MODE

Table 39. Timing of VEN triggered boot to secure firmware download mode (HIF I2C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{DWL_COMMAND_PROCESSING}}$	duration from DWL GET SESSION command until download command processing is entered		-	0.7	1.0	ms

Table 40. Timing of VEN triggered boot to secure firmware download mode (HIF SPI)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{DWL_COMMAND_PROCESSING}}$	duration from DWL GET SESSION command until download command processing is entered		-	0.7	1.0	ms

11.4 Clock input

Table 41. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC compliancy	-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	for full RF operating range	-40	-	+40	ppm
ESR	equivalent series resistance	-	10	30	100	Ω
C_L	load capacitance	-	6	8	10	pF
t_{startup}	crystal startup time	-	-	-	1	ms
P_{xtal}	crystal power dissipation	-	-	-	100	μW

Table 42. Recommended additional crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_m	Motion Capacitance	-	0.8	1	1.5	fF
C_{shunt}	Shunt Capacitance	Standard Operation	0.1	0.6	1	pF

Note: Please refer to [AN14518 Crystal Oscillator Design Guide](#) for further consideration to design and tuning crystal oscillator for NFC design.

Table 43. Frequency requirements for a direct clock input (no crystal)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC compliancy	-	24	-	MHz
			-	32	-	
			-	48	-	
Δf_{clk}	clock frequency accuracy	for full RF operating range	-40	-	+40	ppm
Φ_n	phase noise	input phase noise floor at 100 kHz offset	-	- 150	-145	dBc/Hz
Φ_n	phase noise	input phase noise floor at 1 MHz offset	-	- 152	-149	dBc/Hz
V_i	Input voltage boundary	sinus signal	0	-	1.8	V
$V_{i(p-p)}$	peak-to-peak Input voltage	sinus signal	0.4	-	1.8	V
$V_{i(\text{clk})}$	clock input voltage	square signal	0	-	1.8 +/-10%	V

11.5 DPC characteristics

Table 44. Dynamic power control characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (0x0079)	depends on application target current	ApplicationTargetCurrent × 0.0609 + 2 mA	-	-	mA
	Max target current configured in EEPROM DPC_TARGET_CURRENT (0x0077)	hysteresis as configured in DPC_HYSTERESIS (0x0079)		-	350 - Hysteresis	mA

11.6 EEPROM characteristics

Table 45. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _{endu(W)}	write endurance	at ambient temperature T _a = +25 °C	100	-	-	K cycles
t _{ret}	retention time	at ambient temperature T _a = +25 °C	25	-	-	years

11.7 Thermal characteristics

Table 46. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb}	ambient operating temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA	-40	+25	+85	°C
		in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V	-40	+25	+105	°C

Table 47. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64	53	K/W
R _{th(j-c)}	thermal resistance from junction to case	-	22	K/W

Table 48. Junction temperature

Symbol	Parameter	Conditions	Min	Max	Unit
T _{j_max}	maximum junction temperature	-	-	+125	°C

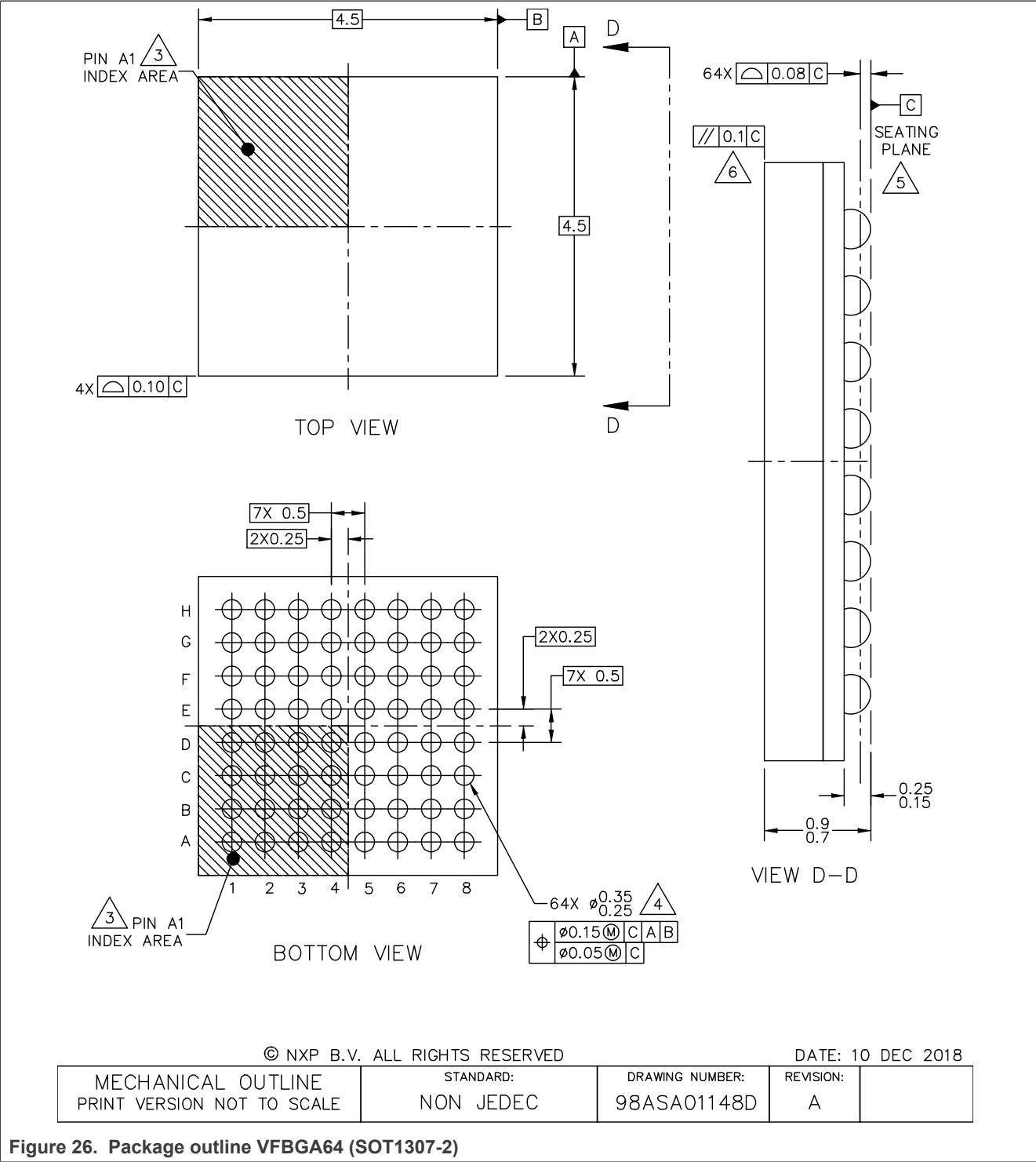
Table 49. Thermal shutdown temperature

Symbol	Parameter	Conditions	Typ	Unit
T _{shutdown}	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

12 Package outline

12.1 VFBGA64 package

Table 50. Package outline VFBGA64 (SOT1307-2)



NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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Figure 27. Package outline note VFBGA64 (SOT1307-2)

13 Package marking

13.1 Package marking drawing VFBGA64

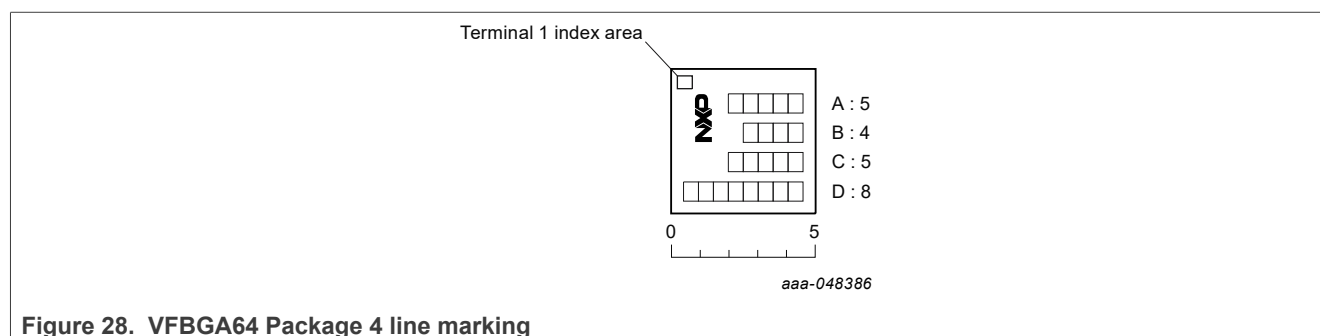


Figure 28. VFBGA64 Package 4 line marking

Line A: 5 characters; 76AC followed by a blank " "

Line B: Firmware version programmed during production

Line C: 5 characters; contains the diffusion batch identifier (DB ID), a blank " " and the assembly sequence identifier (AS ID)

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level ("X" = engineering samples, " " = released product)

14 Reflow soldering footprint VFBGA64

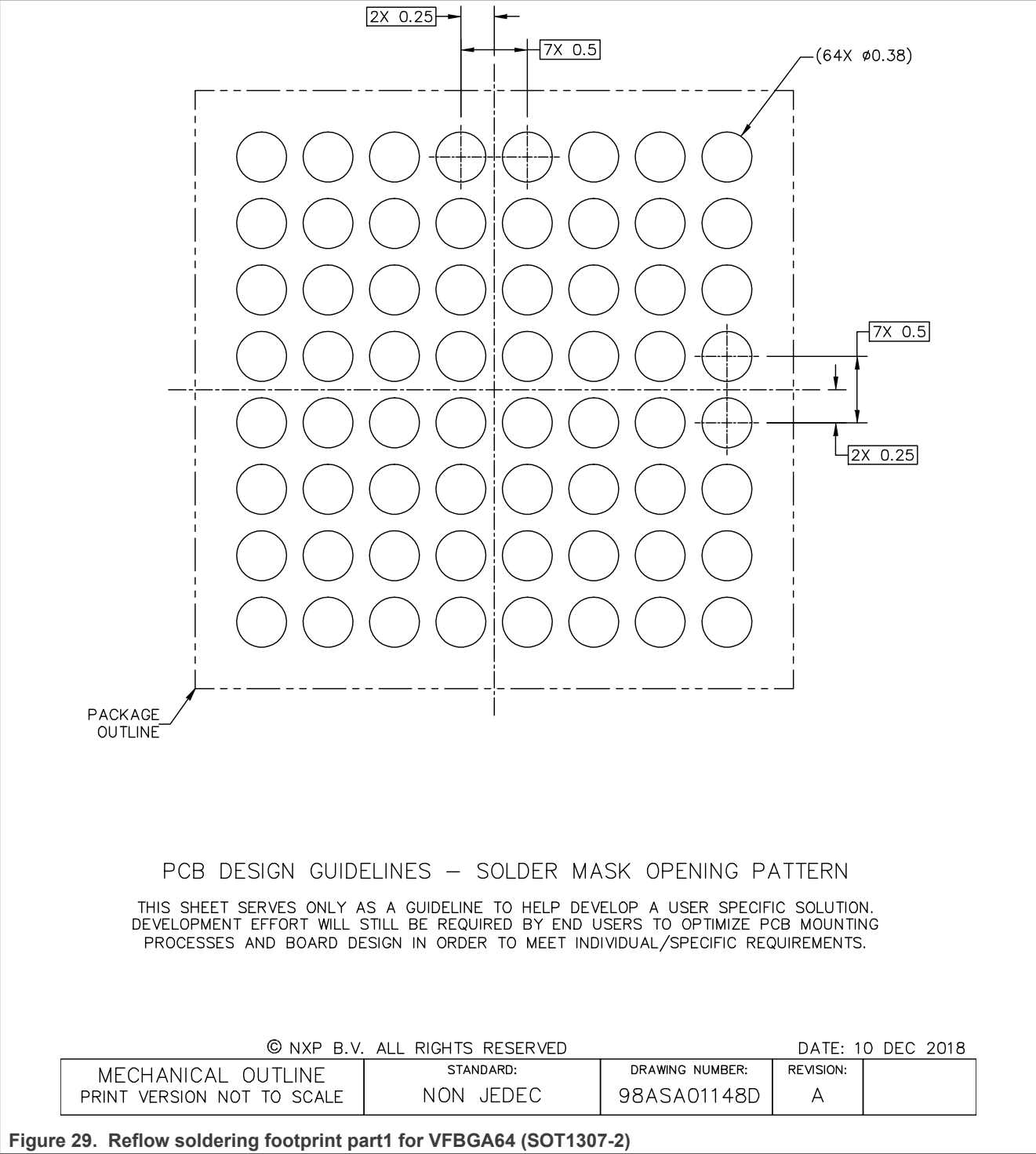
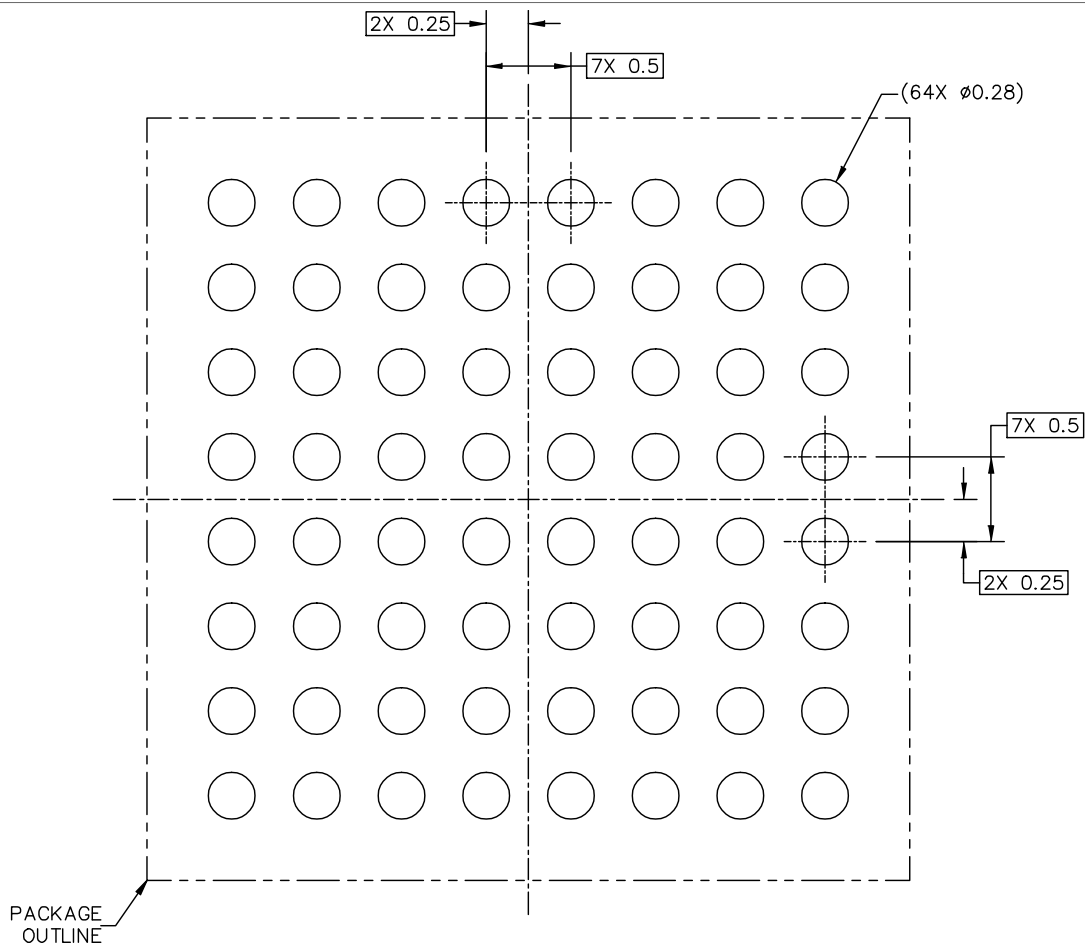


Figure 29. Reflow soldering footprint part1 for VFBGA64 (SOT1307-2)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

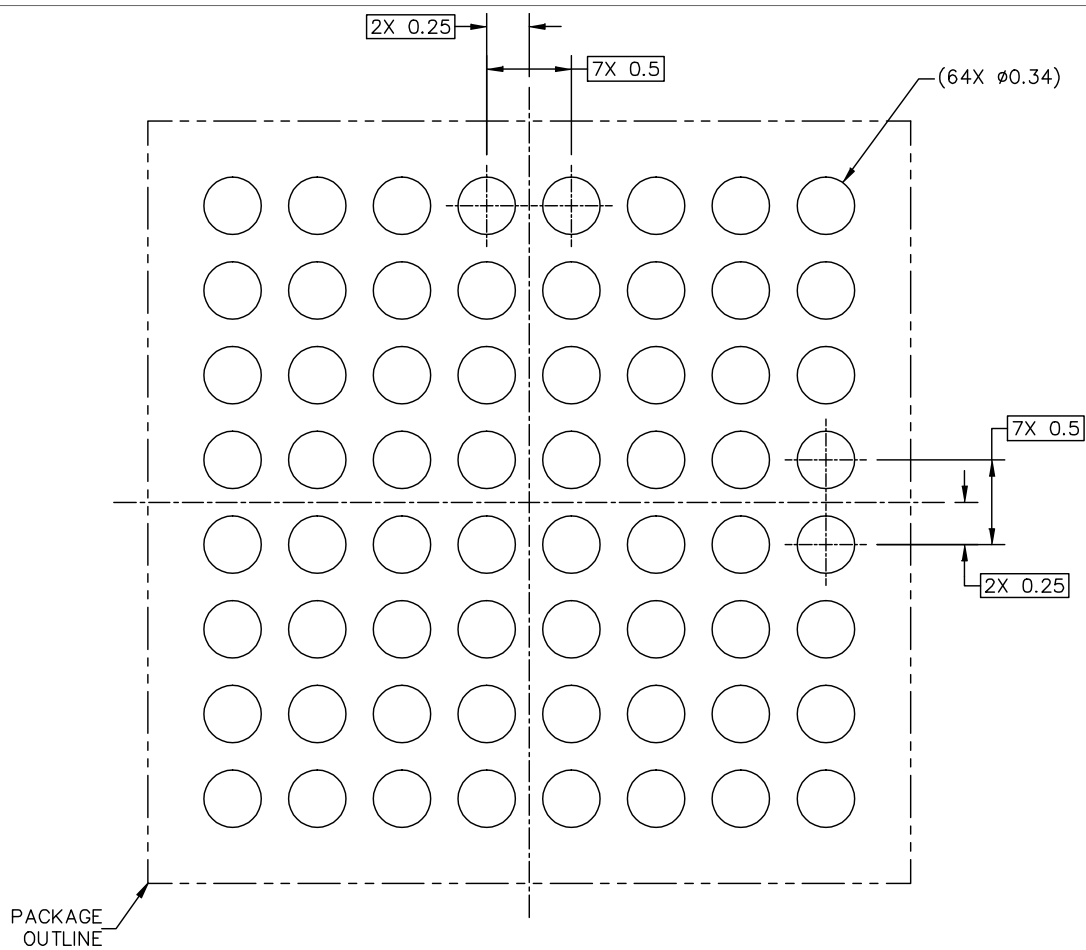
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Figure 30. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 31. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)

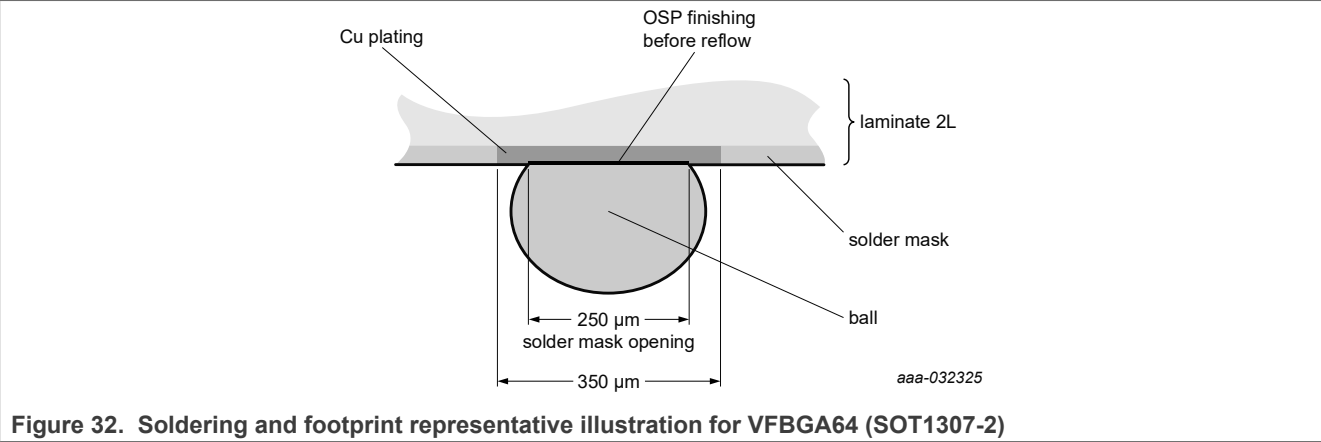


Figure 32. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)

15 Surface mount reflow soldering

For information on surface mount, reflow soldering and component handling, refer to the [Application note – AN10365 Surface mount reflow soldering](#). This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages

16 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, to remove any moisture that might have soaked into the package.

For MSL3:

168h out-of-pack floor life at maximum ambient temperature. Conditions: < 30 °C / 60 % RH.

For MSL2:

- 1 year out-of-pack floor life at maximum ambient temperature. Conditions: < 30 °C / 60 % RH.

For MSL1:

- No out-of-pack floor life specification required. Conditions: < 30 °C / 85 % RH.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

17 Abbreviations

Table 51. Abbreviations

Acronym	Description
AA	audio accelerator
ADC	analog-to-digital converter
AGC	automatic gain control
AHB	advanced high-performance bus
AHB-Lite	advanced high-performance bus (single-controller implementation)
AHB bus	advanced high-performance bus
APB	advanced peripheral bus
API	application programming interface
ARC	adaptive receiver control
Arm	Advanced RISC Machine
AWC	adaptive waveshape control
BBA	baseband amplifier
BOD	brownout detection
CITO	controller input target output
CLIF	contactless interface
COTI	controller output target input
CPU	central processing unit
CRC	cyclic redundancy check
CTR	current transfer ratio
CTS	clear to send
DAC	digital-to-analog converter
DC-DC	switch-mode voltage regulator, which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN76AC integrates a step-up/boost converter
DDR	double data rate
DMA	direct memory access
DPC	dynamic power control
ECC	elliptic curve cryptography
EEPROM	electrically erasable programmable read-only memory
EMC	electromagnetic compatibility
EMD	electromagnetic disturbance
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macro
EOF	end-of-frame
Fm+	Fast-mode Plus
FSM	finite state machine

Table 51. Abbreviations...continued

Acronym	Description
GND	Ground
GPIO	general-purpose input output
HID	human interface device
HPD	hard power down
HW	hardware
IC	Integrated Circuit
IIR	infinite impulse response
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
I/O	input/output
I/Q	in-phase/quadrature-phase
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout regulator
LPUART	Low-Power Universal Asynchronous Receiver / Transmitter
LSB	least significant bit
LSByte	least significant byte
MISO	SPI interface controller in target out
MSL	moisture sensitivity level
MOSI	SPI interface controller out target In
NFC	near-field communication
NRZ	non-return-to-zero
NSS	SPI interface active-low target-select signal
NTS	not target select
NVIC	nested vectored interrupt controller
OS	operating system
OTP	one time programmable
PCB	printed-circuit board
PC	personal computer
PCD	power card detection
PICC	proximity inductive coupling card
PLL	phase-locked loop
PMU	power management unit
PWM	pulse width modulation
RAM	random-access memory
RF	radio frequency

Table 51. Abbreviations...continued

Acronym	Description
RNG	random number generator
ROM	read-only memory
RSA	Rivest, Shamir, and Adleman public key cryptosystem
RSSI	receiver signal strength indicator
RTOS	real-time operating system
RTS	request to send
SCK	SPI interface serial clock
SCL	I ² C interface serial clock
SDA	serial data
SMPS	switch mode power supply
SPI	serial peripheral interface
SRAM	static random-access memory
SWD	serial wire debug
TFT	display technology: thin-film transistor-display
TX	transmit
UART	universal asynchronous receiver transmitter
UID	Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards.
ULPCD	ultra low-power card detection
USB	universal serial bus
VREF	voltage reference

18 References

- [1] User manual – UM12399 – PN76AC user manual ([link](#))
- [2] Application note – AN14518 – Crystal Oscillator Design Guide ([link](#))
- [3] Application note – AN10365 – Surface mount reflow soldering ([link](#))

19 Revision history

Table 52. Revision history

Document ID	Release date	Description
PN76AC v.1.4	22 October 2026	Objective data sheet. Document security status updated to "Public". Editorial changes. Section 4 "Quick reference data": T_{amb} condition updated.
PN76AC v.1.3	24 August 2026	Objective data sheet. Section 6 "Ordering information": updated.
PN76AC v.1.2	1 June 2026	Objective data sheet. Section 8.1 "Pin description VFBGA64": updated.
PN76AC v.1.1	24 April 2026	Objective data sheet. Removed chapters related to EMVCo functionality. Section 1 "General description": updated. Section 2.1.4 "Card emulation": added. Section 6 "Ordering information": updated. Section 8.1 "Pin description VFBGA64": updated. Section 9.5 "System power states": updated. Section 9.6.3 "Transmitter power supply": updated. Section 9.6.3.3 "Configuration example 1: TX_LDO transmitter supply connected to VBAT": updated. Section 9.6.3.4 "Configuration example 2: TX_LDO supplied independent from VBAT": updated. Section 9.6.3.5 "Configuration example 3: TX_LDO not used": updated. Section 9.6.3.6 "Supply voltage range for transmitter supply configuration examples": updated. Section 9.10 "Dynamic power control (DPC)": updated. Section 9.11 "Adaptive waveshape control (AWC)": updated. Section 9.13 "Automatic EMD error handling": updated. Section 9.14 "Energy-saving card detection": updated. Section 9.14.1 "Ultra low-power card detection (ULPCD)": updated. Section 10 "Limiting values": updated. Section 11.1 "Static characteristics": updated. Section 11.2 "Timing characteristics": added. Section 11.3 "Timing characteristics of host interface commands": updated. Section 16 "Handling information": updated. Section 18 "References": updated. - Section "System settings and configuration" moved to UM12399 – PN76AC user manual
PN76AC v.1.0	16 January 2026	Objective data sheet. Initial version.

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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