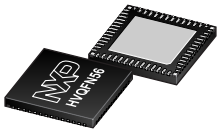
PF09

Nine-channel power management IC with advanced system safety monitoring

Rev. 1.0 — 22 January 2026 **Product short data sheet**



1 General description

The PF09 is a power management integrated circuit (PMIC) optimized for high performance i.MX9x based applications. It Integrates multiple high-efficiency switch mode and linear voltage regulators to support base system power from a pre-regulated system rail (3.3 V to 5.0 V). It provides low quiescent current in STANDBY (STBY) and low-power Off modes. Built-in multiple time programmable configuration stores key startup configurations, drastically reducing the number of external components typically used to set the output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C communication after startup, offering flexibility for different system states.

The PF09 is developed in compliance with the ISO 26262 standard, including safety features, with Fail-safe outputs and integrated self-test mechanisms, becoming part of a safety-oriented system partitioning targeting high-integrity safety levels up to ASIL D, and complying with the IEC61508 industrial safety specification targeting high safety integrity levels up to SIL 2.

2 Features and benefits

- Up to five buck regulators with internal power stage and programable current limits
- Three low-dropout linear regulators with load switch operation
- Ultra-low power always-on LDO supply
- Two external voltage monitoring inputs
- Programmable I/O interfacing pins
- Advanced frequency management with frequency spread spectrum
- Multi-channel analog multiplexer for system voltage monitoring
- High speed I^2C interface with up to 3.4 MHz operation
- Advanced thermal monitoring and thermal shutdown protection
- Functional safety architecture to target up to ASIL D automotive applications
- Functional safety architecture to target up to SIL 2 industrial applications
- Multiple-time programmable configuration (MTP)
- 56-pin QFN Package with exposed pad
- Automotive qualified by AEC-Q100 rev J up to Grade 1

3 Applications

- Automotive infotainment
- High-end consumer and industrial
- Connectivity domain controller
- Telematics

4 Simplified application diagram

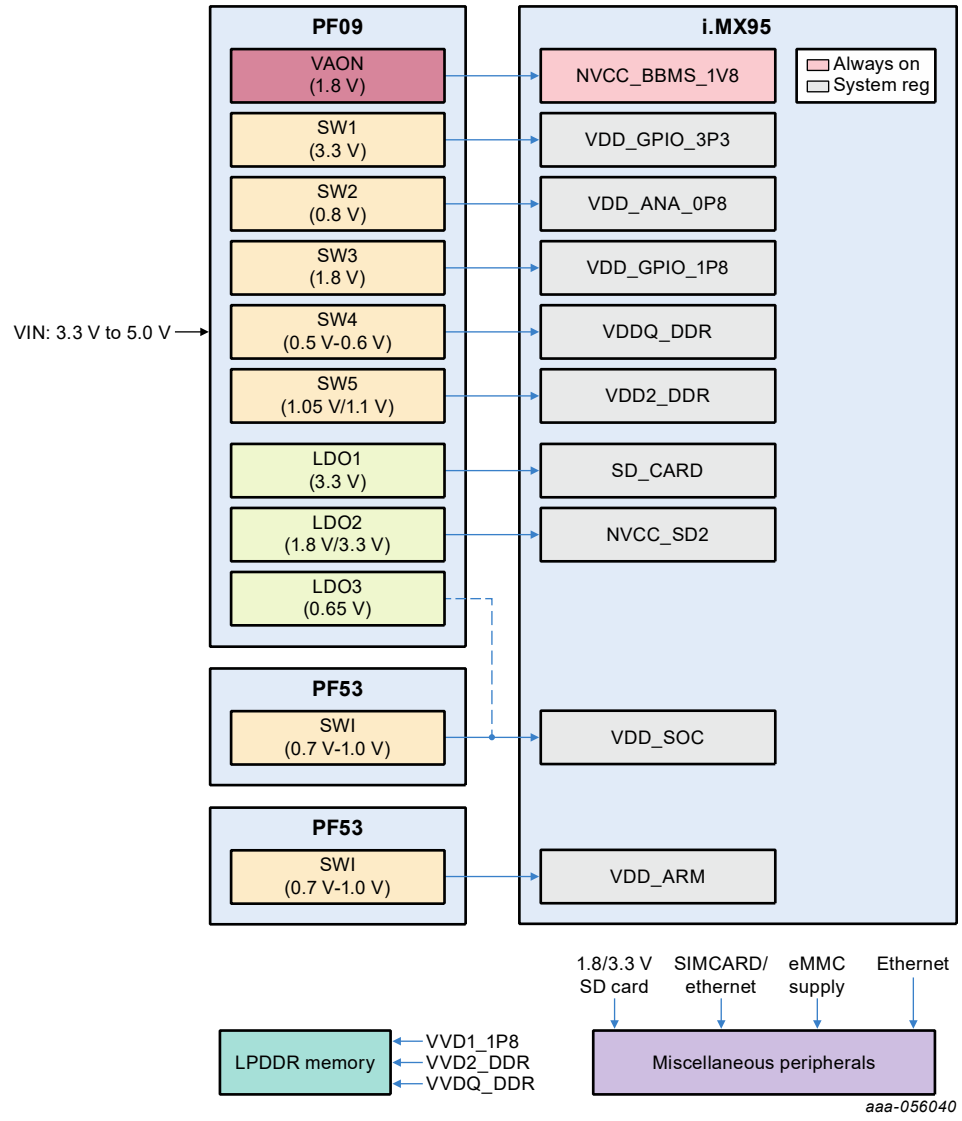


Figure 1. Simplified application diagram i.MX95

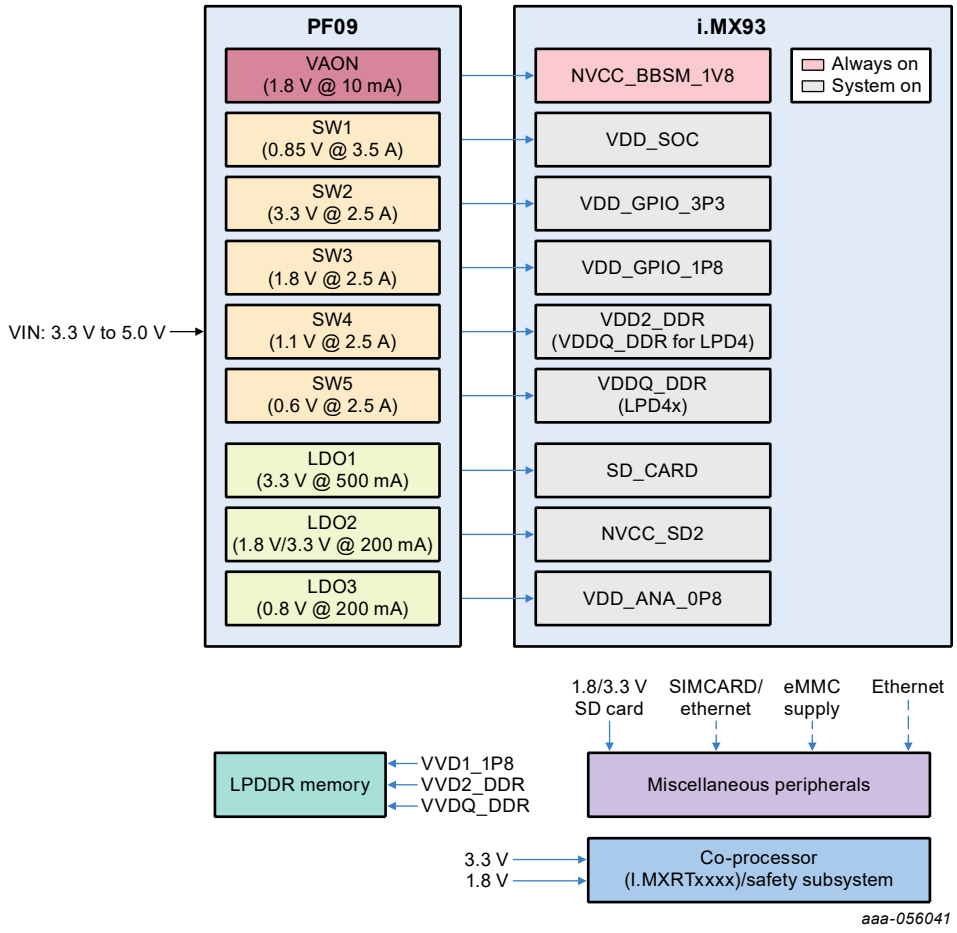


Figure 2. Simplified application diagram i.MX93

5 Ordering information

Table 1. Ordering information

Type number [1]	Package		
	Name	Description	Version
PF0900	HVQFN56	HVQFN56, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 56 terminals, 0.5 mm pitch, 8 mm x 8 mm x 0.53 mm body	SOT684-32(DD)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

Table 2. Ordering options

Part number [1][2]	Target market	NXP processor	System comments	Safety grade	OTP ID
MPF0900AMDA0ES	Automotive	N/A	Not programmed	ASIL D	DA0
MPF0900AMBA0ES	Automotive	N/A	Not programmed	ASIL B	BA0
MPF0900AMMA0ES	Automotive	N/A	Not programmed	QM	MA0
MPF0900AMBA1ES	Automotive	i.MX 95	LPDDR5 memory	ASIL B	BA1
MPF0900AMBA2ES	Automotive	i.MX 95	LPDDR4X memory	ASIL B	BA2
MPF0900AMMA1ES	Automotive	i.MX 95	LPDDR5 memory	QM	MA1
MPF0900AMMA2ES	Automotive	i.MX 95	LPDDR4X memory	QM	MA2
MPF0900AMMA5ES	Automotive	i.MX 93	LPDDR4X memory	QM	MA5
MPF0900AVNA0ES	Industrial	N/A	Not programmed	QM	NA0
MPF0900AVSA0ES	Industrial	N/A	Not programmed	SIL 2	SA0
MPF0900AVNA1ES	Industrial	i.MX 95	LPDDR5 memory	QM	NA1
MPF0900AVNA2ES	Industrial	i.MX 95	LPDDR4X memory	QM	NA2
MPF0900AVNA5ES	Industrial	i.MX 93	LPDDR4X memory	QM	NA5
MPF0900AVSA1ES	Industrial	i.MX 95	LPDDR5 memory	SIL 2	SA1
MPF0900AVSA2ES	Industrial	i.MX 95	LPDDR4X memory	SIL 2	SA2
PPF0900AMBA7ES	Automotive	i.MX943 Auto	LPDDR5	ASIL B	BA7
PPF0900AMBA8ES	Automotive	i.MX943 Auto	LPDDR4	ASIL B	BA8
PPF0900AMMA7ES	Automotive	i.MX943 Auto	LPDDR5	QM	MA7
PPF0900AMMA8ES	Automotive	i.MX943 Auto	LPDDR4	QM	MA8

[1] P = Engineering sample part number (PPF09x)
[2] M = Production part number (MPF09x)

6 Internal block diagram

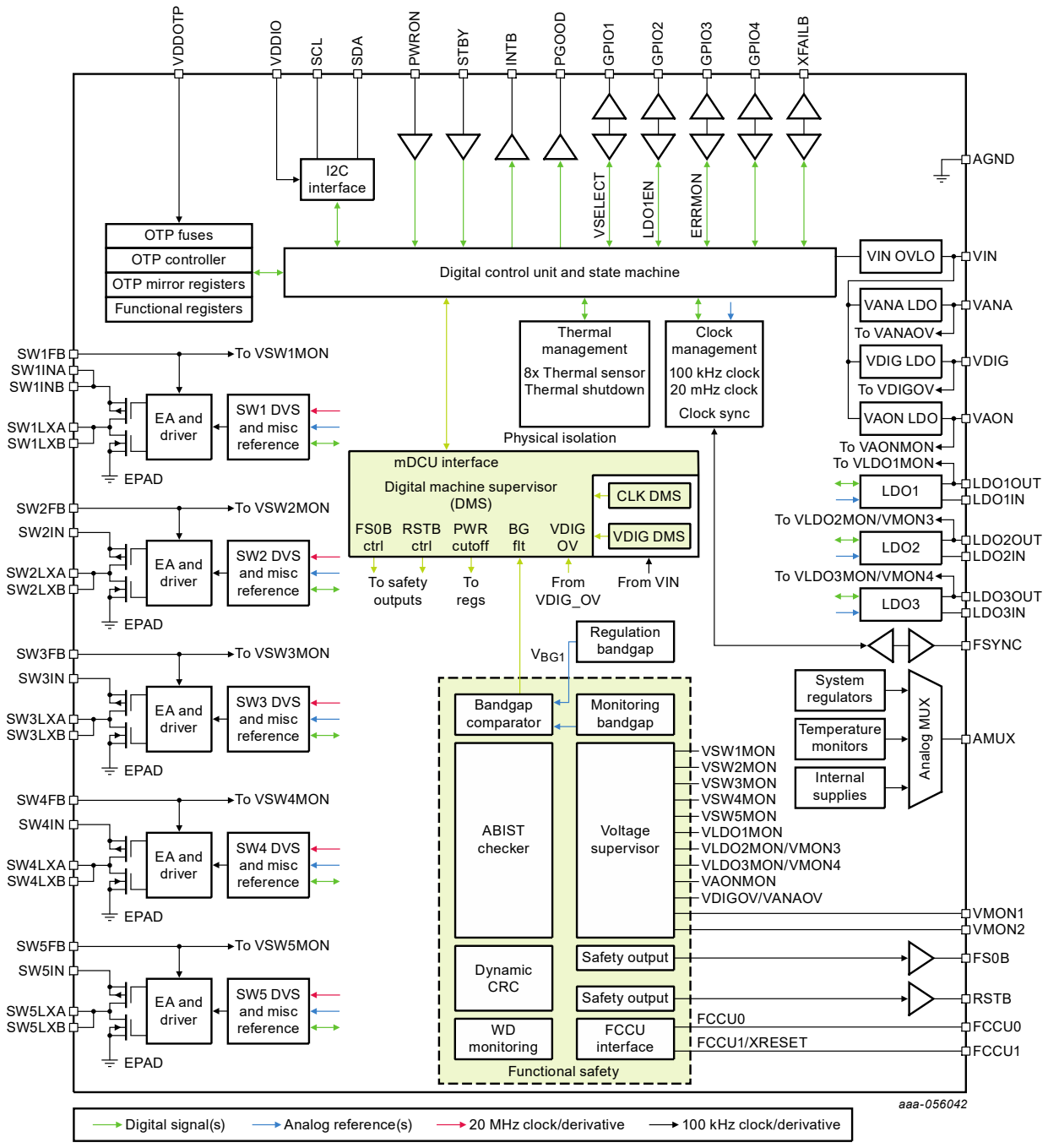


Figure 3. Internal block diagram

7 Pinning information

7.1 Pinning

The PF09 is offered in a 56-pin, 8 x 8 mm^2 body size QFN with exposed pad and wettable flanks.

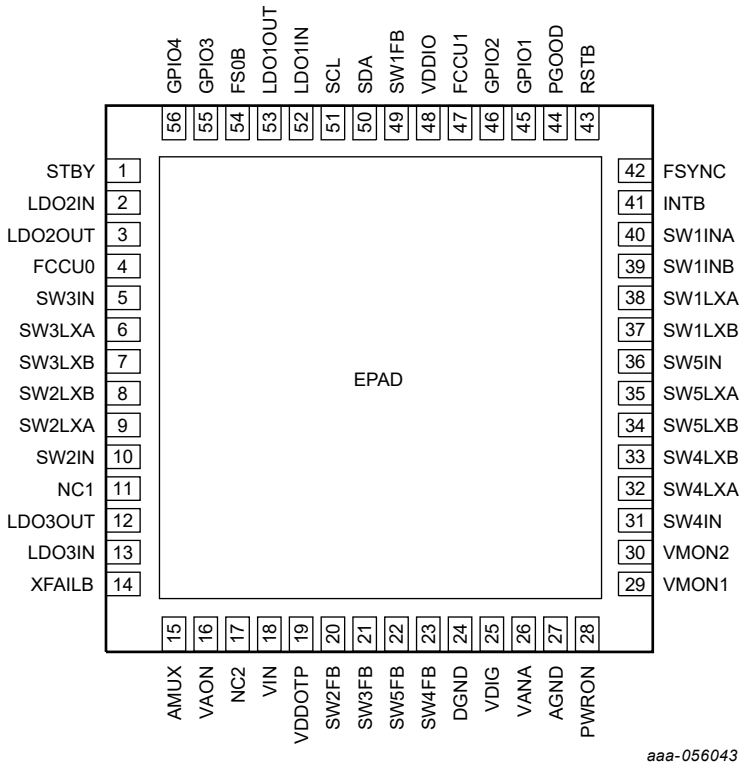


Figure 4. PF09 package pinout (top view)

7.2 Pin description

Table 3. QFN56 Pin description

Pin	Pin name	Description	Min	Max	Units
1	STBY	STANDBY request	-0.3	6.0	V
2	LDO2IN	LDO2 input	-0.3	6.0	V
3	LDO2OUT	LDO2 output	-0.3	6.0	V
4	FCCU0	FCCU fault monitoring input 0	-0.3	6.0	V
5	SW3IN	SW3 Input	-0.3	6.0	V
6	SW3LXA	SW3 switching node A	-0.3	6.0	V
7	SW3LXB	SW3 switching node B	-0.3	6.0	V
8	SW2LXB	SW2 switching node B	-0.3	6.0	V
9	SW2LXA	SW2 switching node A	-0.3	6.0	V
10	SW2IN	SW2 input	-0.3	6.0	V
11	NC1	Not connected	-0.3	6.0	V

Table 3. QFN56 Pin description*...continued*

Pin	Pin name	Description	Min	Max	Units
12	LDO3OUT	LDO3 output	-0.3	6.0	V
13	LDO3IN	LDO3 input	-0.3	6.0	V
14	XFAILB	External fail	-0.3	6.0	V
15	AMUX	Analog multiplexer output	-0.3	6.0	V
16	VAON	Always-on output	-0.3	6.0	V
17	NC2	Not connected	-0.3	6.0	V
18	VIN	PMIC input supply	-0.3	6.0	V
19	VDDOTP	OTP supply	-0.3	10.0	V
20	SW2FB	SW2 feedback	-0.3	6.0	V
21	SW3FB	SW3 feedback	-0.3	6.0	V
22	SW5FB	SW5 feedback	-0.3	6.0	V
23	SW4FB	SW4 feedback	-0.3	6.0	V
24	DGND	Digital ground	-0.3	0.3	V
25	VDIG	Internal digital supply	-0.3	2.0	V
26	VANA	Internal analog supply	-0.3	2.0	V
27	AGND	Analog ground	-0.3	0.3	V
28	PWRON	Power on request	-0.3	6.0	V
29	VMON1	External VMON1	-0.3	6.0	V
30	VMON2	External VMON2	-0.3	6.0	V
31	SW4IN	SW4 Input	-0.3	6.0	V
32	SW4LXA	SW4 switching node A	-0.3	6.0	V
33	SW4LXB	SW4 switching node B	-0.3	6.0	V
34	SW5LXB	SW5 switching node B	-0.3	6.0	V
35	SW5LXA	SW5 switching node A	-0.3	6.0	V
36	SW5IN	SW5 input	-0.3	6.0	V
37	SW1LXB	SW1 switching node B	-0.3	6.0	V
38	SW1LXA	SW1 switching node A	-0.3	6.0	V
39	SW1INB	SW1 input B	-0.3	6.0	V
40	SW1INA	SW1 input A	-0.3	6.0	V
41	INTB	Interrupt request	-0.3	6.0	V
42	FSYNC	Clock sync input	-0.3	6.0	V
43	RSTB	MCU reset pin	-0.3	6.0	V
44	PGOOD	Power good	-0.3	6.0	V
45	GPIO1	Programmable IO1	-0.3	6.0	V
46	GPIO2	Programmable IO2	-0.3	6.0	V
47	FCCU1	XRESET/FCCU fault monitoring input 1	-0.3	6.0	V

Table 3. QFN56 Pin description*...continued*

Pin	Pin name	Description	Min	Max	Units
48	VDDIO	I/O supply input	-0.3	6.0	V
49	SW1FB	SW1 feedback	-0.3	6.0	V
50	SDA	I^2C data	-0.3	6.0	V
51	SCL	I^2C clock	-0.3	6.0	V
52	LDO1IN	LDO1 input	-0.3	6.0	V
53	LDO1OUT	LDO1 output	-0.3	6.0	V
54	FS0B	Fail-safe output	-0.3	6.0	V
55	GPIO3	Programmable IO3	-0.3	6.0	V
56	GPIO4	Programmable IO4	-0.3	6.0	V
57	EPAD	Exposed pad ground	-0.3	0.3	V

8 Maximum ratings

Table 4. UVDET electrical characteristics

All parameters are specified at T_A = -40 °C to 125 °C, unless otherwise noted. Typical values are characterized at T_A = 25 °C, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{UVDET_RISE}	Rising UVDET	2.8	2.85	2.9	V
V_{UVDET_FALL}	Falling UVDET	2.7	2.75	2.8	V

Table 5. VIN_OV electrical characteristics

Symbol	Description	Min	Typ	Max	Unit
V_{IN_OV}	VIN overvoltage rising	5.65	5.8	5.95	V
$V_{IN\_OV\_HYS}$	VIN overvoltage hysteresis	50	100	125	mV

Table 6. Electrical characteristics

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
PWRON					
$V_{IN\_MAX\_PWRON}$	Maximum input voltage	—	—	5.5	V
V_{IH_PWRON}	PWRON input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_PWRON}	PWRON input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_PWRON}	PWRON input buffer hysteresis	60	—	—	mV
R_{PD_PWRON}	PWRON internal pulldown	—	10	25	MΩ
STBY					
$V_{IN\_MAX\_STBY}$	Maximum input voltage	—	—	5.5	V
V_{IH_STBY}	STBY input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_STBY}	STBY input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_STBY}	STBY input buffer hysteresis	100	—	—	mV
FCCU1 (XRESET Mode)					
$V_{IN\_MAX\_XRESET}$	Maximum input voltage	—	—	5.5	V
V_{IH_XRESET}	XRESET input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	—	—	V
V_{IL_XRESET}	XRESET input low voltage	—	—	$0.3*V_{DDIO}$	V

Table 6. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• Maximum voltage to ensure a low state				
I_{HYS_XRESET}	XRESET input buffer hysteresis	100	—	—	mV
R_{PD_XRESET}	XRESET internal pull-down	400	800	1300	kΩ
INTB					
V_{OL_INTB}	INTB output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_INTB}	INTB output low current	—	—	10	mA
t_{INTB_PULSE}	INTB test pulse	90	100	110	µs
$V_{IN\_MAX\_RSTB}$	Maximum input voltage	—	—	5.5	V
RSTB					
V_{IH_RSTB}	RSTB input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_RSTB}	RSTB input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_RSTB}	RSTB input buffer hysteresis	100	—	—	mV
$V_{OH\_RSTB\_VDDIO}$	RSTB output high voltage • OTP_RSTB_MODE [1:0] = 01	V_{DDIO} – 0.5	—	—	V
$V_{OH\_RSTB\_VAON}$	RSTB output high voltage • OTP_RSTB_MODE [1:0] = 10	V_{AON} – 0.5	—	—	V
V_{OL_RSTB}	RSTB output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_RSTB}	RSTB output low current	—	—	10	mA
I_{OH_RSTB}	RSTB output high current • OTP_RSTB_MODE = 01 or 10	—	—	2	mA
t_{RSTB_PULSE}	RSTB pulse duration	90	100	110	µs
PGOOD					
$V_{IN\_MAX\_PGOOD}$	Maximum input voltage	—	—	5.5	V
V_{IH_PGOOD}	PGOOD input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_PGOOD}	PGOOD input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_PGOOD}	PGOOD input buffer hysteresis	100	—	—	mV
V_{OL_PGOOD}	PGOOD output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_PGOOD}	PGOOD output low current	—	—	10	mA
GPIO1					

Table 6. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
$V_{IN\_MAX\_GPIO1}$	Maximum input voltage	—	—	5.5	V
V_{IH_GPIO1}	GPIO1 input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_GPIO1}	GPIO1 input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_GPIO1}	GPIO1 input buffer hysteresis	100	—	—	mV
V_{OL_GPIO1}	GPIO1 output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_GPIO1}	GPIO1 output low current	—	—	10	mA
$V_{OH\_GPIO1\_VIN}$	GPIO1 output high voltage • OTP_GPIO1_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	—	—	V
I_{OH_GPIO1}	GPIO1 output high current	—	—	2	mA
R_{PD_GPIO1}	GPIO1 internal pull-down • In VESELECT mode	1	2	4	MΩ
GPIO2					
$V_{IN\_MAX\_GPIO2}$	Maximum input voltage	—	—	5.5	V
V_{IH_GPIO2}	GPIO2 input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_GPIO2}	GPIO2 input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_GPIO2}	GPIO2 input buffer hysteresis	100	—	—	mV
V_{OL_GPIO2}	GPIO2 output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_GPIO2}	GPIO2 output low current	—	—	10	mA
$V_{OH\_GPIO2\_VIN}$	GPIO2 output high voltage • OTP_GPIO2_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	—	—	V
I_{OH_GPIO2}	GPIO2 output high current	—	—	2	mA
R_{PD_GPIO2}	GPIO2 internal pulldown • In LDO1EN mode	1	2	4	MΩ
GPIO3					
$V_{IN\_MAX\_GPIO3}$	Maximum input voltage	—	—	5.5	V
V_{IH_GPIO3}	GPIO3 input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_GPIO3}	GPIO3 input low voltage	—	—	0.4	V

Table 6. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
	• Maximum voltage to ensure a low state				
I_{HYS_GPIO3}	GPIO3 input buffer hysteresis	100	—	—	mV
V_{OL_GPIO3}	GPIO3 output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_GPIO3}	GPIO3 output low current	—	—	10	mA
$V_{OH\_GPIO3\_VIN}$	GPIO3 output high voltage • OTP_GPIO3_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	—	—	V
I_{OH_GPIO3}	GPIO3 output high current	—	—	2	mA
GPIO4					
$V_{IN\_MAX\_GPIO4}$	Maximum input voltage	—	—	5.5	V
V_{IH_GPIO4}	GPIO4 input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_GPIO4}	GPIO4 input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_GPIO4}	GPIO4 input buffer hysteresis	100	—	—	mV
V_{OL_GPIO4}	GPIO4 output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_GPIO4}	GPIO4 output low current	—	—	10	mA
$V_{OH\_GPIO4\_VIN}$	GPIO4 output high voltage • OTP_GPIO4_MODE[1:0] = 01 (push-pull to VIN) • Load current = 2 mA	VIN – 0.5	—	—	V
FS0B					
$V_{IN\_MAX\_FS0B}$	Maximum input voltage	—	—	5.5	V
V_{IH_FS0B}	FS0B input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V
V_{IL_FS0B}	FS0B input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_FS0B}	FS0B input buffer hysteresis	100	—	—	mV
V_{OL_FS0B}	FS0B output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_FS0B}	FS0B output low current	—	—	10	mA
XFAILB					
$V_{IN\_MAX\_XFAILB}$	Maximum input voltage	—	—	5.5	V
V_{IH_XFAILB}	XFAILB input high voltage • Minimum voltage to ensure a high state	1.4	—	—	V

Table 6. Electrical characteristics...*continued*

All parameters are specified at T_A = -40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5 V and T_A = 25 °C unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
V_{IL_XFAILB}	XFAILB input low voltage • Maximum voltage to ensure a low state	—	—	0.4	V
I_{HYS_XFAILB}	XFAILB input buffer hysteresis	100	—	—	mV
V_{OL_XFAILB}	XFAILB output low voltage • Maximum voltage at 10 mA load	—	—	0.4	V
I_{OL_XFAILB}	XFAILB output low current	—	—	10	mA
R_{XPU_XFAILB}	XFAILB external pullup • Pullup to VANA	—	10	—	kΩ
C_{XFAILB}	XFAIL recommended decoupling EMC capacitance	—	100	—	nF
I^2C interface					
V_{OL_SDA}	SDA output low voltage • Maximum voltage at 20 mA load	—	—	0.4	V
V_{IH_SDA}	SDA input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	—	—	V
V_{IL_SDA}	SDA input low voltage • Maximum voltage to ensure a low state	—	—	$0.3*V_{DDIO}$	V
V_{IH_SCL}	SCL input high voltage • Minimum voltage to ensure a high state	$0.7*V_{DDIO}$	—	—	V
V_{IL_SCL}	SCL input low voltage • Maximum voltage to ensure a low state	—	—	$0.3*V_{DDIO}$	V
F_{I2C_FMP}	I^2C operating frequency • Fast-mode plus	—	—	1	MHz
F_{I2C_HS}	I^2C operating frequency • High speed	—	—	3.4	MHz
$R_{XPU\_SCL\_FMP}$	SCL external pullup Fast mode plus • Pullup to VDDIO • I^2C Fast mode	—	2.2	—	kΩ
$R_{XPU\_SDA\_FMP}$	SDA external pullup Fast mode plus • Pullup to VDDIO • I^2C Fast mode	—	2.2	—	kΩ
$R_{XPU\_SCL\_HS}$	SCL external pullup high speed • Pullup to VDDIO • I^2C high speed	—	0.8	—	kΩ
$R_{XPU\_SDA\_HS}$	SDA external pullup high speed • Pullup to VDDIO • I^2C high speed	—	0.8	—	kΩ

9 Electrostatic discharge (ESD) requirements

Table 7. Electrostatic discharge (ESD) ratings

Symbol	Description	Min	Typ	Max	Unit
V_{ESDHBM}	Human body model	—	—	2000	V
V_{ESDCDM}	Charge device model • QFN package - all pins	—	—	500	V
$I_{LATCHUP}$	Latch-up current	—	—	100	mA

All ESD specifications will be compliant with the AEC-Q100 specification.

10 Thermal characteristics

Table 8. Thermal characteristics

All parameters are specified up to a junction temperature of 150 °C. All parameters are tested at T_A from −40 °C to 105 °C, to allow headroom for self-heating during operation. If higher T_A operation is required, proper thermal and loading consideration must be made to ensure device operation below the maximum T_J = 150 °C.

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient operating temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{ST}	Storage temperature range	-55	—	150	°C
T_{PPRT}	Peak package reflow temperature	—	—	260	°C

Table 9. QFN56 thermal resistance package dissipation ratings

Symbol	Description	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance[1] JESD51-7, 2s2p	—	—	24.4	°C/W
Ψ_{JT}	Junction-to-Top of Package Thermal Characterization Parameter[1] Eight-layer board (4S4P)	—	—	0.2	°C/W
$R_{\theta JC}$	Junction to Case Thermal Resistance[2] JESD51-7, 1s	—	—	1.0	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

11 Revision history

Table 10. Revision history

Document ID	Release date	Description
PF09_SDS v.1.0	22 January 2026	Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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