PCF8525UK

Nano-Power RTC IC with I2C Interface

Rev. 2.0 — 3 June 2026 **Product data sheet**

1 General description

The PCF8525UK is a CMOS Real Time Clock (RTC) and calendar optimized for low power consumption. All addresses and data are transferred serially via I2C buses.

The WLCSP package serves as a specialized option for designs where space is more critical.

The PCF8525UK has many features like backup battery switch-over circuit, programmable watchdog function, configurable interrupt outputs, and timestamp function.

The device supports the -40 °C to +85 °C extended temperature range.

2 Features and benefits

- Operating temperature ranges from -40 °C to +85 °C
- Ultra-low power: 64 nA (Typ) in timekeeping at VDD = 3.3 V
- Integrated oscillator load capacitors for CL = 7 pF
- Full function operating voltage: 1.2 V to 5.5 V
- Clock operating voltage: 0.9 V to 5.5 V (including timekeeping function)
- I2C-bus interface (400 kHz)
- Provides year, month, day, weekday, hours, minutes, seconds, and 1/100 seconds
- Programmable alarm function with interrupt
- Programmable watchdog timer with interrupt
- Timestamp function with interrupt
- Battery backup input pin and switch-over circuitry
- Power-on Reset (POR)
- Software reset function
- Two interrupt outputs ($\overline{\text{INTB}}$ multiplexed with CLKOUT)
- Package: WLCSP12 (1.6 mm x 1.2 mm with 0.4 mm pitch)

3 Applications

- Portable Instruments
- Wearables
- Industrial
- IOT

4 Ordering information

Table 1 describes the ordering information for PCF8525UK.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCF8525UK	525U	WLCSP12	Wafer Level Chip Scale Package, 12 bumps; body dimensions: 1.6 x 1.2 x 0.525 mm with 0.4 mm pitch	SOT1390-13

4.1 Ordering options

Table 2 describes the ordering options for PCF8525UK.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCF8525UK	PCF8525UKZ	WLCSP12	Reel dry pack, SMD, 7" Q1 standard product orientation	5000	T_{amb} = -40 °C to +85 °C

5 Block diagram

Figure 1 shows the labeled block diagram of PCF8525UK.

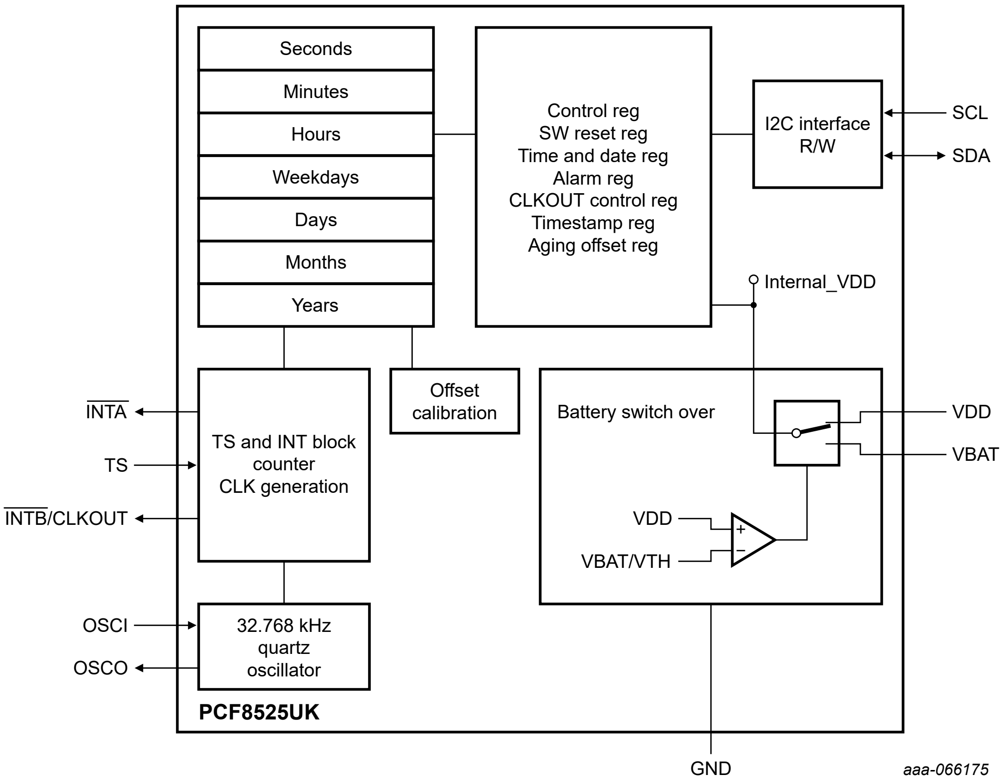


Figure 1. Block diagram of PCF8525UK

6 Pinning information

This section provides the pin configuration and description for PCF8525UK.

6.1 Pinning

This section provides pin configuration for packages under PCF8525UK.

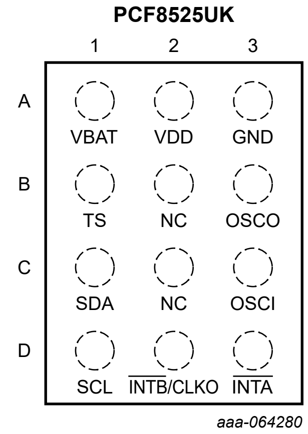


Figure 2. Pin configuration for PCF8525UK (transparent top view)

6.2 Pin description

Table 3 provides detailed description of various pins on PCF8525UK.

Table 3. Pin description

Symbol	Pin	Description
GND	A3	Ground
OSCO	B3	Oscillator output
OSCI	C3	Oscillator input
$\overline{\text{INTA}}$	D3	Open-drain active-low interrupt output
$\overline{\text{INTB}}$/CLKOUT	D2	If configured as $\overline{\text{INTB}}$ = open-drain active-low interrupt output. An external pullup resistor is required. If configured as CLKOUT = push-pull square wave output.
SCL	D1	I2C-bus serial clock
SDA	C1	I2C-bus serial bidirectional data line
TS	B1	Timestamp input with 500 kΩ internal pullup resistor
VBAT	A1	Battery backup supply voltage
VDD	A2	Supply voltage
EP	N.A.	Tie to ground (preferred) or leave floating
NC	B2, C2	These pins are connected to the ground internally and must be floating or connected to the ground on the PCB.

7 Functional description

The PCF8525UK is a Real Time Clock (RTC) and calendar. It uses an external 32.768 kHz quartz crystal.

The I2C-bus interface transfers the address and data (400 kHz maximum).

The PCF8525UK has a backup battery input pin and backup battery switch-over circuit, which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see section Section 7.5.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

7.1 Register overview

The PCF8525UK contains an auto-incrementing address register. The built-in address register will increment automatically after each read or write of a data byte up to the register 2Eh. After register 2Eh, the auto-incrementing will wrap around to address 00h (see Figure 3).

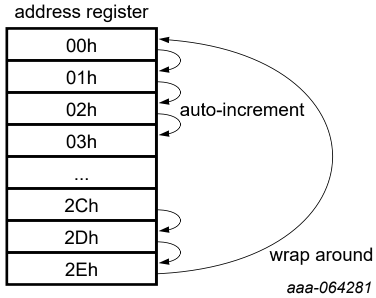


Figure 3. Handling address registers

- The first five registers (memory address 00h, 01h, 02h, 03h, and 04h) are used as control registers (see Section 7.2).
- The register at address 05h is for software reset.
- The memory addresses 06h through to 0Dh are used as counters for the clock function (1/100 seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 7.9).
- The registers at addresses 0Eh through 14h define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 7.10).
- The register at address 15h defines and the clock out mode. CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 17).
- The registers at addresses 16h to 1Ch are used for the timestamp1 function. When a trigger event happens, the actual time is saved in the timestamp1 registers (see Section 7.12).
- The registers at addresses 1Dh to 23h are used for the second timestamp, which always represents the last write of the date/time registers.
- The registers at addresses 24h to 25h are used for random code generation. This field is updated with a unique number every time the date/time registers are written.
- The registers at addresses 26h and 27h are used for the correction of the crystal aging effect (see Section 7.4.1).
- The registers at addresses 28h to 2Bh are used for interrupt configuration.
- The registers at addresses 2Ch and 2Dh are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 20 ms to greater than 4 hours. An interrupt is generated when the watchdog times out.

- The registers 100th Seconds, Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bitwise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen and all registers hold their state during I2C transactions. The timestamp registers get updated when the bus transaction completes. This operation prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 7.9.9).

7.1.1 Register map

Table 4 describes the register overview of PCF8525UK.

Table 4. Register overview

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
Control registers											
00h	Control_1	R		STOP	100TH_ S_DIS	R	12_24	MI	SI	0000 1000	Table 5
01h	Control_2	MSF	TI_TP	WDTF	AF	OSFE[1:0]		AIE	SMBUS_ TIMEOUT	0000 1101	Table 7
02h	Control_3	-	PWRMNG[1:0]		-	BF	OSIE	BIE	-	0110 0000	Table 9
03h	Control_4	TSF	-	-	-	-	-	-	-	0000 0000	Table 11
04h	Control_5	TSIE	-	-	-	-		CL		0000 0000	Table 13
Software Reset											
05h	SR_Reset	CPR	-	R	-	SR	R	-	CTS	0010 0100	Table 24
Time and date registers											
06h	100th_Seconds	100TH_SECONDS(0 to 99)								0000 0000	Table 25
07h	Seconds	OSF	SECONDS (0 to 59)							1000 0000	Table 28
08h	Minutes	VLF	MINUTES (0 to 59)							1000 0000	Table 31
09h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode					0000 0000	Table 33
				HOURS (0 to 23) in 24-hour mode						0000 0000	
0Ah	Days	-	-	DAYS (1 to 31)						0000 0001	Table 35
0Bh	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			0000 0001	Table 37
0Ch	Months	-	-	-	MONTHS (1 to 12)					0000 0001	Table 40
0Dh	Years	YEARS (0 to 99)								0000 0001	Table 43
Alarm registers											
0Eh	Second_alarm	AE_S	SECOND_ALARM (0 to 59)							1000 0000	Table 45
0Fh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)							1000 0000	Table 47
10h	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode					1000 0000	Table 49
				HOUR_ALARM (0 to 23) in 24-hour mode						1000 0000	
11h	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)						1000 0000	Table 51
12h	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1000 0000	Table 53
13h	Month_alarm	AE_Y	AE_MO	-	MONTHS (1 to 12)					1100 0000	Table 55
14h	Year_alarm	YEARS (0 to 99)								0000 0000	Table 57
CLKOUT control register											
15h	CLKOUT_ctl				OTPR	CLKOE	COF[2:0]			000X 1000	Table 15
Timestamp 1 registers											
16h	Timestp_ctl1	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 63
17h	Sec_timestp1	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 67

Table 4. Register overview*...continued*

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
18h	Min_timestp1	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 69
19h	Hour_timestp1	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 71
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
1Ah	Day_timestp1	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 73
1Bh	Mon_timestp1	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 75
1Ch	Year_timestp1	YEAR_TIMESTP (0 to 99)								0000 0000	Table 77
Timestamp 2 registers											
1Dh	Subsec_timestp2	-	-	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 65
1Eh	Sec_timestp2	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 67
1Fh	Min_timestp2	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 69
20h	Hour_timestp2	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 71
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
21h	Day_timestp2	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 73
22h	Mon_timestp2	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 75
23h	Year_timestp2	YEAR_TIMESTP (0 to 99)								0000 0000	Table 77
R-Code registers											
24h	R_code1	CODE[15:8]								Random	Section 7.13
25h	R_code2	CODE[7:0]								Random	
Aging offset registers											
26h	AgingOffset_High	AO[15:8]								0000 0000	Table 18
27h	AgingOffset_Low	AO[7:0]								0000 0000	Table 19
Interrupt mask registers											
28h	INTA_MASK1	-	-	MIA	SIA	OSIEA	AIEA	BIEA	WD_CDA	0011 1111	Table 80
29h	INTA_MASK2	-	-	-	-	TSIEA	-	-	-	0000 1000	Table 82
2Ah	INTB_MASK1	-	-	MIB	SIB	OSIEB	AIEB	BIEB	WD_CDB	0011 1111	Table 80
2Bh	INTB_MASK2	-	-	-	-	TSIEB	-	-	-	0000 1000	Table 82
Watchdog registers											
2Ch	Watchdg_tim_ctl	WD_CD	-	-	-	-	-	TF[1:0]		0000 0011	Table 84
2Dh	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								0000 0000	Table 86

7.2 Control registers

The first five registers of the PCF8525UK, with the addresses 00h, 01h, 02h, 03h, and 04h, are used as control registers.

7.2.1 Register Control_1

Table 5 and Table 6 describe the bit allocation and bit description of the Control_1 register, respectively.

Table 5. Control_1 - control and status register 1 (address 00h) bit allocation
Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	R	TC_DIS	STOP	100TH_S_DIS	R	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

Table 6. Control_1 - control and status register 1 (address 00h) bit description
Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	R	0	Reserved bit with reset value of 0. The user must not write 1 to this bit.	
6[1]	TC_DIS	0	Temperature compensation enabled	
		1	Temperature compensation disabled	
5	STOP	0	RTC source clock runs	Section 7.16
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT output frequencies are still available	
4	100TH_S_DIS	0	100th seconds counter enabled	
		1	100th seconds counter disabled, register 06h reset to 00h.	
3	R	1	Reserved bit with reset value of 1. The user must not write 0 to this bit.	
2	12_24	0	24-hour mode selected	Table 34, Table 50, and Table 72
		1	12-hour mode selected	
1	MI	0	Minute interrupt disabled	Section Section 7.14.1
		1	Minute interrupt enabled	
0	SI	0	Second interrupt disabled	

[1] The user must write **1** to Control_1 register, bit 6 (TC_DIS), on every power-on reset or software reset.

7.2.2 Register Control_2

Table 7 and Table 8 describe the bit allocation and bit description of the Control_2 register, respectively.

Table 7. Control_2 - control and status register 2 (address 01h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	TI_TP	WDTF	AF	OSFE[1:0]		AIE	SMBUS_TIMEOUT
Reset value	0	0	0	0	1	1	0	1

Table 8. Control_2 - control and status register 2 (address 01h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	MSF	0	No minute or second interrupt generated	Section 7.14.1
		1	Flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	TI_TP	0	The interrupt pin INTA is configured to generate a permanent active signal when MSF is set	
		1	The interrupt pin $\overline{INTA}$ is configured to generate a pulsed signal when MSF flag is set (see Figure 13)	
5	WDTF	0	No watchdog timer interrupt generated	Section 7.15.3
		1	Flag set when watchdog timer interrupt generated; flag must be cleared to clear interrupt	
4	AF	0	No alarm was interrupted triggered	Section 7.10.8
		1	Flag set when alarm triggered; flag must be cleared to clear interrupt	
3:2	OSFE[1:0]	See Table 23	Control of the oscillator stop detection function	Section 7.6
1	AIE	0	No interrupt generated from the alarm flag	Section 7.14.3
		1	Interrupt generated when alarm flag set	
0	SMBUS_TIMEOUT	0	SMBus SCL timeout feature disabled	
		1	SMBus SCL timeout feature enabled	

7.2.3 Register Control_3

Table 9 and Table 10 describe the bit allocation and bit description of the Control_3 register, respectively.

Table 9. Control_3 - control and status register 3 (address 02h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PWRMNG[1:0]		-	BF	OSIE	BIE	-

Table 9. Control_3 - control and status register 3 (address 02h) bit allocation*...continued*

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Reset value	0	1	1	0	0	0	0	0

Table 10. Control_3 - control and status register 3 (address 02h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	-	0	Unused	
6 to 5	PWRMNG[1:0]	See Table 21	Control of the battery switch-over function	Section 7.5
4	-	0	Unused	
3	BF	0	No battery switch-over interrupt occurred	Section 7.5.1 and section Section 7.14.5
		1	Flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	OSIE	0	No interrupt generated when OSF is set	Section 7.6 and Section Section 7.14.6
		1	Interrupt generated when OSF is set (only applicable when OSFE[1:0]=01 (always ON)	
1	BIE	0	No interrupt generated from the battery flag (BF)	Section 7.14.5
		1	Interrupt generated when BF is set	
0	-	0	Unused	

7.2.4 Register Control_4

Table 11 and Table 12 describe the bit allocation and bit description of the Control_4 register, respectively.

Table 11. Control_4 - control and status register 4 (address 03h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	TSF	-	-	-	-	-	-	-
Reset value	0	0	0	0	0	0	0	0

Table 12. Control_4 - control and status register 4 (address 03h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	TSF	0	No timestamp interrupt generated for pin TS	Section 7.12.1
		1	Flag set when TS input is driven to ground; flag must be cleared to clear interrupt	
6 to 0	-	0	Unused	

7.2.5 Register Control_5

Table 13 and Table 14 describe the bit allocation and bit description of the Control_5 register, respectively.

Table 13. Control_5 - control and status register 5 (address 04h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	TSIE	-	-	-	-		R	
Reset value	0	0	0	0	0	0	0	0

Table 14. Control_5 - control and status register 5 (address 04h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	TSIE	0	No interrupt generated from timestamp flag of TS	Section 7.14.4
		1	Interrupt generated when timestamp flag set of TS	
6 to 3	-	0	Unused	-
2[1]	TEMP_RD_EN	0	Enable temperature sensor digital readout from register 2Eh	
		1	Disable temperature sensor digital readout from register 2Eh	
1	R	0	Reserved bit with reset value of 0. The user must not write 1 to this bit.	
0		0	Unsused	

[1] The user must write **1** to Control_5 register, bit 2 (TEMP_RD_EN), on every power-on reset or software reset.

7.3 Register CLKOUT_ctl

Table 15 and Table 16 describe the bit allocation and bit description of the CLKOUT_ctl register, respectively.

Table 15. CLKOUT_ctl - CLKOUT control register (address 15h) bit allocation

Bits labeled as - are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[2:0]			OTPR	CLKOE	COF[2:0]		
Reset value	0	0	0	X	1	0	0	0

Table 16. CLKOUT_ctl - CLKOUT control register (address 15h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7 to 5		0	Unused	
4	OTPR	0	No OTP refresh	Section 7.3.1

Table 16. CLKOUT_ctl - CLKOUT control register (address 15h) bit description*...continued*

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
		1	OTP refresh performed	
3	CLKOE	0	$\overline{INTB}$/CLKOUT pin configured as $\overline{INTB}$ (open-drain interrupt output)	
		1	$\overline{INTB}$/CLKOUT pin configured as CLKOUT (push-pull clock output)	
2 to 0	COF[2:0]	See Table 17	CLKOUT frequency selection	Section 7.3.2

7.3.1 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

When read OTPR bit, its state is:

1. "0" until the OTP read state machine completes copying of the eFuse data into the shadow registers. It could be due to a POR event or writing a 0 > 1 to the OTPR register bit.
2. "1" when the OTP read state machine completes copying to the shadow registers from the eFuse instances. During normal operation, OTPR must be kept at 1 to prevent higher power usage.

The OTP logic is not reset or affected by the Software Reset. The OTPR functionality is only reset by the initial digital POR.

During OTP refresh, V_{DD} has to be above 1.6 V. The rising speed to 1.6 V must be faster than 2 V/100 ms. After the OTP refresh has finished, the PCF8525UK can fully operate with V_{DD} as low as 1.2 V.

7.3.2 Clock output

A programmable square wave is available at pin CLKOUT. The COF[2:0] control bits in register CLKOUT_ctl control the operation. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator at 25 °C to determine the aging offset.

CLKOUT is a push-pull output and is enabled at power on. When disabled, the output is high-impedance. When configured as $\overline{INTB}$, this pin is an open-drain output.

Table 17. CLKOUT frequency selection

COF[2:0]		CLKOUT frequency (Hz)	Typical duty cycle[1]
000	Default	32 768	60 : 40 to 40 : 60
001		16 384	50 : 50
010		8 192	50 : 50
011		4 096	50 : 50
100		2 048	50 : 50
101		1 024	50 : 50
110		1	50 : 50

Table 17. CLKOUT frequency selection...*continued*

COF[2:0]		CLKOUT frequency (Hz)	Typical duty cycle[1]
111		$\overline{\text{INTB}}$/CLKOUT = High-Z	-

[1] Duty cycle definition: % HIGH-level time: % LOW-level time

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all but the 32.768 kHz frequencies are 50 : 50.

7.4 Register Aging_offset

This section describes the bit allocation and bit description of the Aging_offset register, respectively.

Table 18. AgingOffset_High - crystal aging offset register (address 26h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	AO[15:8]							
Reset value	0	0	0	0	0	0	0	0

Table 19. AgingOffset_Low - crystal aging offset register (address 27h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	AO[7:0]							
Reset value	0	0	0	0	0	0	0	0

Table 20. Aging offset - crystal aging offset registers (address 26h and 27h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
15 to 0	AO[15:0]	Section 7.4.1	Aging offset value

7.4.1 Crystal aging correction

The PCF8525UK has AgingOffset registers to correct the crystal aging effects.

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative.

Follow the steps below to measure and enter the frequency offset into the aging offset registers. The compensation logic then applies a correction that is equal and opposite to the offset.

1. Power up the PCF8525UK. Wait one second for the oscillations to settle.
2. Write 0x01 to register CLKOUT_ctl (13h) to drive the uncompensated 16.384 kHz signal on the $\overline{\text{INTB}}$/CLKOUT pin.
3. Measure the frequency (FREQ) on the $\overline{\text{INTB}}$/CLKOUT pin using a high-accuracy frequency counter.
4. Convert the frequency to ppm as FREQ_PPM = (FREQ - 16384)*10^6/16384.

5. Calculate the offset value as OFFSET = FREQ_PPM/0.0298 and round it up to the nearest integer.
6. Convert OFFSET to a 16-bit binary (use two's complement for negative values) and enter it into AgingOffset_High (26h) and AgingOffset_Low (27h) registers.
7. The new offset correction will begin after the AgingOffset_Low byte is written.

7.5 Power management functions

The PCF8525UK has two power supplies:

- V_{DD}: The main power supply
- V_{BAT}: The battery backup supply

Internally, PCF8525UK operates with the internal operating voltage $V_{oper(int)}$. Depending on the condition of the main power supply and the selected power management function, $V_{oper(int)}$ is either on the potential of V_{DD} or V_{BAT}.

Battery switch-over function monitors the main power supply V_{DD} and switching to V_{BAT} if a power fail condition is detected (see Section 7.5.1).

The power management functions are controlled by the control bits PWRMNG[1:0] (see Table 21) in register Control_3 (see Table 10):

Table 21. Power management control bit description

PWRMNG[1:0]		Function
00		The battery switch-over function is enabled in standard mode
01		Battery switch-over function is enabled in direct switching mode
10, 11 (Default)	[1]	Battery switch-over function is disabled, only one power supply (V_{DD})

[1] When the battery switch-over function is disabled, the device works only with the power supply VDD. VBAT must be connected to the ground.

7.5.1 Battery switch-over function

PCF8525UK has a backup battery switch-over circuit, which monitors the main power supply VDD. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

- Standard mode: The power failure condition happens when VDD < VBAT AND VDD < Vth(sw)bat. Vth(sw)bat is the battery switch threshold voltage whose typical value is 1.45 V. The battery switch-over in standard mode works only when VDD > 1.6 V during initial power up. Applying back-up battery voltage to VBAT without applying VDD supply does not power on the device. Only when VDD main power is supplied, the device starts operating.
- Direct switching mode: The power failure condition happens when VDD < VBAT. Direct switching from VDD to VBAT without requiring VDD to drop below Vth(sw)bat

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set to logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 7.14.5)
3. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

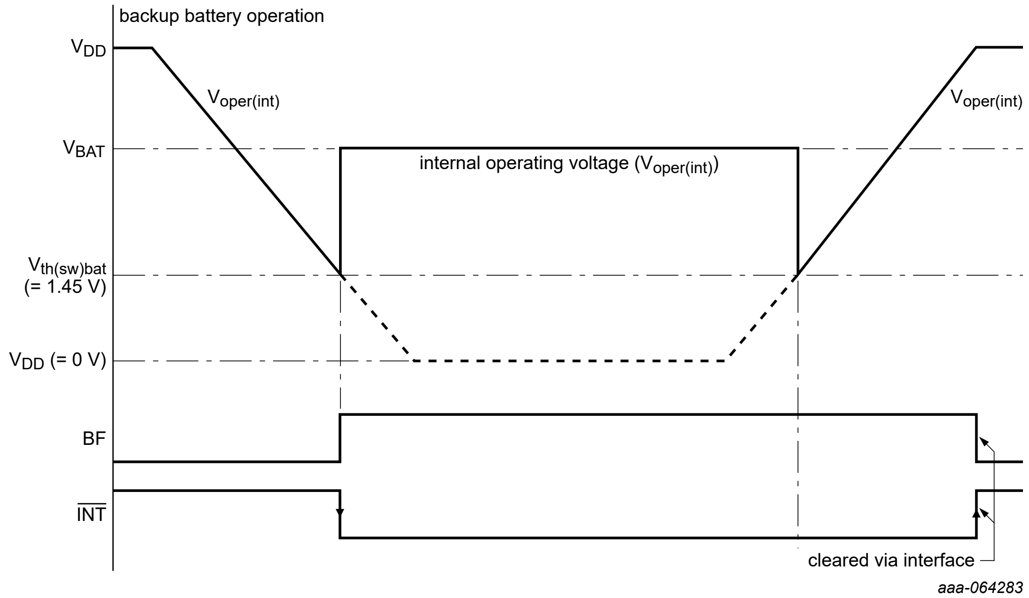
The interface and CLKOUT output are disabled in battery backup operation:

1. Interface inputs are not recognized, preventing extraneous data being written to the device
2. Interface outputs are high-impedance.

7.5.1.1 Standard mode

If VDD > VBAT OR VDD > Vth(sw)bat, Voper(int) is at VDD potential.

If VDD < VBAT AND VDD < Vth(sw)bat, Voper(int) is at VBAT potential.



Vth(sw)bat is the battery switch threshold voltage. The typical value is 1.45 V.

VDD can be lower than VBAT (for example VDD = 1.8 V, VBAT = 3.0 V).

Figure 4. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

7.5.1.2 Direct switching mode

If VDD > VBAT, Voper(int) is at VDD potential.

If VDD < VBAT, Voper(int) is at VBAT potential.

The direct switching mode is useful in systems where VDD is always higher than VBAT. This mode is not recommended if the VDD and VBAT values are similar (for example, VDD = 3.3 V, VBAT ≥ 3.0 V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of VDD and Vth(sw)bat is not performed.

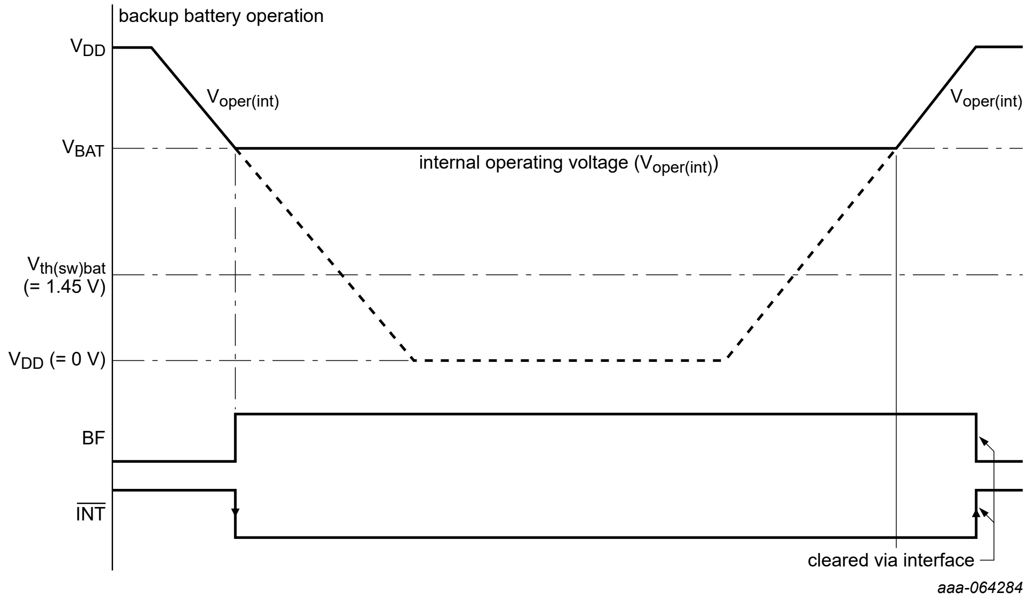


Figure 5. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

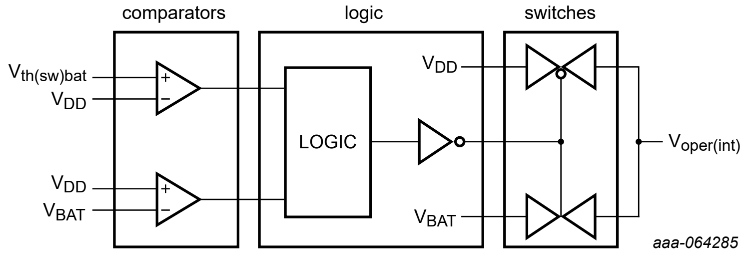
7.5.1.3 Battery switch-over disabled: Only one power supply (VDD)

When the battery switch-over function is disabled:

- The power supply is applied on the VDD pin.
- The VBAT pin must be connected to the ground.
- Voper(int) is at VDD potential.
- The battery flag (BF) is always logic 0.

7.5.1.4 Battery switch-over architecture

Figure 6 shows the architecture of the battery switch-over circuit.



Voper(int) is at VDD or VBAT potential.

Note: *Assure that there are decoupling capacitors on the pins VDD and VBAT.*

Figure 6. Battery switch-over circuit, simplified block diagram

7.5.2 Internal operating voltage (Voper(int))

The voltage level of the internal supply rail, Voper(int), depends on the selected battery switch-over function mode:

Table 22. Internal Operating Voltage

Battery switch-over function mode	Conditions	Potential of Voper(int)
Standard	VDD > VBAT OR VDD > Vth(sw)bat	VDD
	VDD < VBAT AND VDD < Vth(sw)bat	VBAT
Direct switching	VDD > VBAT	VDD
	VDD < VBAT	VBAT
Disabled	Only V_{DD} available, V_{BAT} must be put to the ground	VDD
	VDD > VBAT OR VDD > Vth(sw)bat	VDD

7.6 Oscillator stop and voltage low detection functions

The PCF8525UK has an on-chip oscillator detection circuit, which indicates the status of oscillations. There is also an on-chip supply voltage detection circuit, which indicates the low status of the supply voltage. When the supply is below V_{LOW}, the VLF flag is set to logic 1. When the oscillator stops, the OSF (Oscillator Stop Flag) is set to logic 1.

7.6.1 Power on

When the PCF8525UK is powered on from VDD = VBAT = 0 V:

1. The oscillator is not running and the chip is in reset (OSF and VLF bit are logic 1).
2. When the oscillator starts running and the supply is OK after power on, the chip exits from reset.
3. The flag OSF and VLF are still logic 1 and must be cleared (OSF and VLF bit set logic 0) by I2C command.
4. OTP refresh must be performed (see Section 7.3.1).
5. The user must write **1** to Control_1 register, bit 6 (TC_DIS), on every power-on reset or software reset.
6. The user must write **1** to Control_5 register, bit 2 (TEMP_RD_EN), on every power-on reset or software reset.

7.6.2 Power supply failure and Voltage Low Flag (VLF)

When the active power supply of the chip drops below a certain value (V_{LOW}), VLF is set to logic 1. I2C and interrupt functions are not guaranteed at this supply level. The oscillator and time keeping function can still work until the supply voltage is 0.9 V. The $V_{LOW(max)}$ is 1.2 V.

Once the supply voltage increases again to a level greater than V_{LOW}, the flags can be read. At this point, VLF = 1 indicates to the MCU that the active supply of the RTC has dropped below V_{LOW}. The VLF flag can be cleared (VLF bit set logic 0) by I2C command.

7.6.3 Oscillator Stop Flag (OSF)

The oscillator can stop due to two reasons:

1. The active supply has dropped below $V_{DD:CLK(min)}$ = 0.9 V. Now, both OSF and VLF are set to logic 1, and both can only be cleared once the supply voltage has risen above $V_{LOW(max)}$ = 1.2 V.
2. The crystal is no longer producing oscillations due to a defect/failure. There is no dependence with VLF in this scenario (OSFE must be set to 01); and OSF is set to logic 1. It can only be cleared once the oscillations start again.

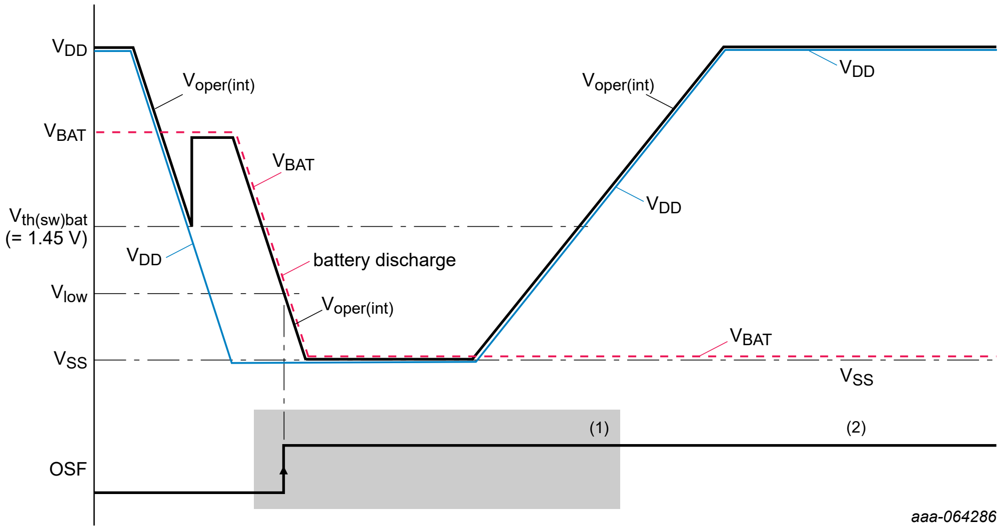
When OSF flag is cleared, an OTP refresh must be performed (see Section 7.3.1).

7.6.4 Oscillator Stop Flag Enable (OSFE)

The oscillator stop detection function (OSF flag) can be enabled or disabled using the OSFE[1:0] bit field. By default, OSF is only enabled after VLF has been set (VDD drops below V_{LOW}).

Table 23. Oscillator Stop Function Enable bit description

OSFE[1:0]	Function
00	Oscillator stop detection function is always disabled.
01	The oscillator stop detection function is always enabled.
10,11 (Default)	The oscillator stop detection function is only enabled after VLF = 1 (VDD drops below V_{LOW}). The OSF function is disabled again when VDD rises above V_{LOW}.



1. Theoretical state of the signals since there is no power.
2. When supply voltage less than Vlow (1.2 V max), flag VLF set logic 1.
3. When the oscillator has stopped, the OSF sets logic 1.

Figure 7. Power failure event due to battery discharge; reset occurs

7.7 Power-On Reset (POR) function

The PCF8525UK has a POR function implemented.

7.7.1 POR

The POR is active whenever the oscillator is stopped. The oscillator is considered stopped during the time between power on and stable crystal resonance (see Figure 8). This time can be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see Section 7.3.1) is ideally executed as the first instruction after startup and also after a reset due to an oscillator stop.

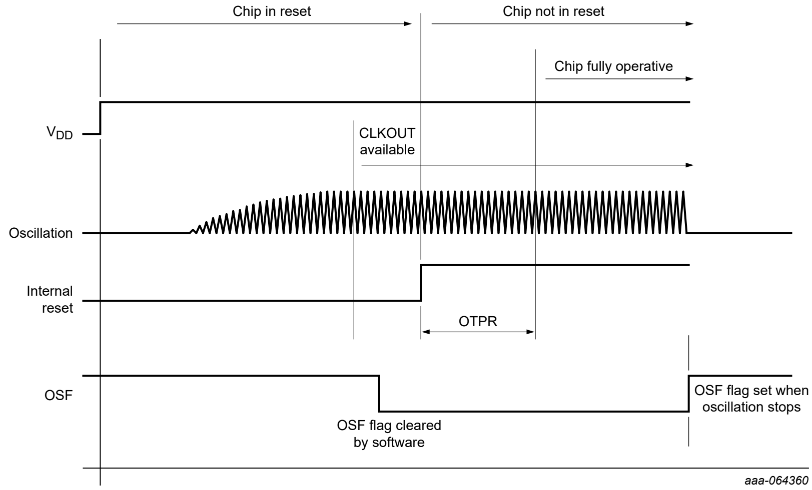


Figure 8. Dependency between POR, OSF flag, and oscillator

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- OSF and Vlow flag (VLF) are set to 1 and ready to be cleared
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (VDD)
- 100th second enabled
- Time 00:00:00.00
- Date 2000.01.01
- Weekday Monday

The register values after power on are shown in Table 4.

7.8 Software Reset register

Table 24 describes the Software Reset register bit description.

Table 24. Reset - software reset control (address 05h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CPR	-	R	-	SR	R	-	CTS
Reset value	0	0	1	0	0	1	0	0

- To trigger a software reset (SR), 0010 1100 (2Ch) must be sent to register Reset (address 05h). A software reset also triggers CPR and CTS.
- The user must write **1** to Control_1 register, bit 6 (TC_DIS), on every power-on reset or software reset.
- The user must write **1** to Control_5 register, bit 2 (TEMP_RD_EN), on every power-on reset or software reset.
- To clear prescaler (CPR), 1010 0100 (A4h) must be sent to register Reset (address 05h).
- To clear the timestamp (CTS), 0010 0101 (25h) must be sent to register Reset (address 05h). It is possible to combine CPR and CTS by sending 1010 0101 (A5h).

Read of the SR_RESET register returns a fixed pattern of 00100100.

Note: *Any other value sent to this register is ignored.*

7.8.1 SR: Software reset

A reset is automatically generated at power on as POR, as described in Section 7.7. A reset can also be initiated with the software reset command.

After software reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- OTP not reloaded, OTPR unchanged
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (VDD)
- 100th second enabled
- Time 00:00:00.00
- Date 2001.01.01
- Weekday Monday

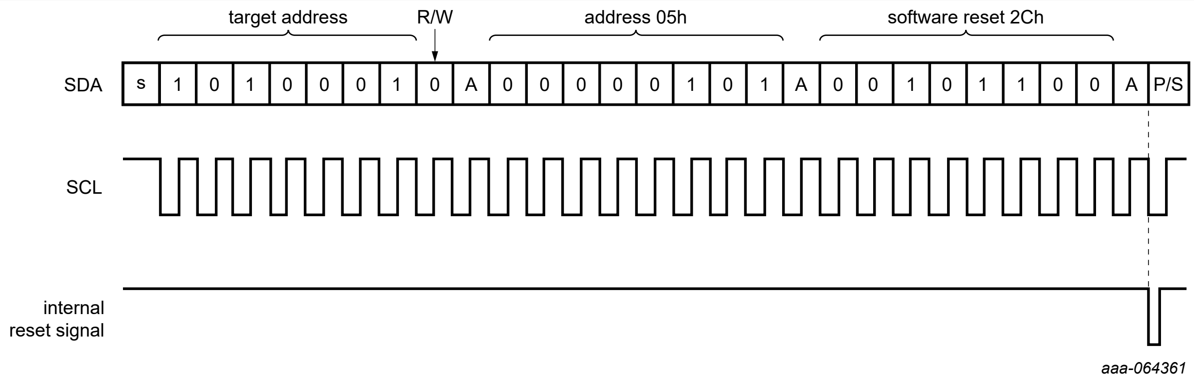


Figure 9. Software reset command

7.8.2 CPR: Clear prescaler

To set the time for RTC mode, the clear prescaler instruction is needed. Before sending this instruction, it is mandatory to first set stop by the STOP bit. See the STOP definition for an explanation on using this instruction.

7.8.3 CTS: Clear timestamp

The timestamp registers (address 16h to 23h) can be set to all 0 with this instruction.

7.9 Time and date function

Most of these registers are coded in the Binary Coded Decimal (BCD) format.

7.9.1 Register 100th Seconds

This section details the 100th Seconds register, including its bit allocation, individual bit definitions, and the representation of 100th Seconds in BCD format.

Table 25. 100th Seconds - 100th seconds (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	100TH SECONDS (0 to 99)							
Reset value	0	0	0	0	0	0	0	0

Table 26. 100th Seconds - 100th seconds register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	100TH SECONDS	0 to 9	Tens place	Actual seconds coded in BCD format
3 to 0		0 to 9	Unit place	

Table 27. 100th Seconds coded in BCD format

Bit	Upper-digit (tens place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

7.9.2 Register Seconds

This section details the Seconds register, including its bit allocation, individual bit definitions, and the representation of Seconds in BCD format.

Table 28. Seconds - seconds and clock integrity register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 29. Seconds - seconds and clock integrity register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	No oscillator stop occurred
		1	-	Oscillator stop occurred
6 to 4	SECONDS	0 to 5	Tens place	Actual seconds coded in BCD format
3 to 0		0 to 9	Unit place	

Table 30. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (tens place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

7.9.3 Register Minutes

This section details the Minutes register, including its bit allocation and individual bit definitions.

Table 31. Minutes - minutes register (address 08h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	VLF	MINUTES (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 32. Minutes - minutes register (address 08h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	VLF	0	-	Clock integrity is guaranteed
		1	-	I2C integrity is not guaranteed; Clock and timing keeping function can still work down to supply voltage = 0.9 V
6 to 4	MINUTES	0 to 5	Tens place	Actual minutes coded in BCD format
3 to 0		0 to 9	Unit place	

7.9.4 Register Hours

This section details the Hours register, including its bit allocation and individual bit definitions.

Table 33. Hours - hours register (address 09h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOURS (1 to 12) in 12-hour mode				
			HOURS (0 to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

Table 34. Hours - hours register (address 09h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
12-hour mode [1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM
4	HOURS	0 to 1	Tens place	Actual hours coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOURS	0 to 2	Tens place	Actual hours coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1 (see Table 6).

7.9.5 Register Days

This section details the Days register, including its bit allocation and individual bit definitions.

Table 35. Days - days register (address 0Ah) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAYS (1 to 31)					
Reset value	0	0	0	0	0	0	0	1

Table 36. Days - days register (address 0Ah) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
5 to 4	DAYS [1]	0 to 3	Tens place	Actual day coded in BCD format
3 to 0		0 to 9	Unit place	

[1] If the year counter contains a value exactly divisible by 4, excluding the year 00, the RTC compensates for leap years by adding the 29th day to February. Next time the year rolls over to 00 is going to be the year 2100, which is not a leap year.

7.9.6 Register Weekdays

This section details the Weekdays register, including its bit allocation, individual bit definitions, and Weekday assignments.

Table 37. Weekdays - weekdays register (address 0Bh) bit

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	T	T	WEEKDAYS (0 to 6)		
Reset value	0	0	0	0	0	0	0	1

Table 38. Weekdays - weekdays register (address 0Bh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 3	T	000	Unused
2 to 0	WEEKDAYS	0 to 6	Actual weekday value (see Table 39)

Although association of weekdays counter to actual weekday is arbitrary, PCF8525UK assumes that Sunday is 000 and Monday is 001 for determining the increment for calendar weeks.

Table 39. Weekday assignments

Day	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

7.9.7 Register Months

This section details the Months register, including its bit allocation, individual bit definitions, and the representation of Months assignments in BCD format.

Table 40. Months - months register (address 0Ch) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTHS (1 to 12)				

Table 40. Months - months register (address 0Ch) bit allocation*...continued*

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	1

Table 41. Months - months register (address 0Ch) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	Unused
4	MONTHS	0 to 1	Tens place	Actual month coded in BCD format (see Table 42)
3 to 0		0 to 9	Unit place	

Table 42. Month assignments in BCD format

Month	Upper-digit (tens place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 4	Bit 3
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

7.9.8 Register Years

This section details the Years register, including its bit allocation and individual bit definitions.

Table 43. Years - years register (address 0Dh) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	YEARS (0 to 99)							
Reset value	0	0	0	0	0	0	0	1

Table 44. Years - years register (address 0Dh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	Tens place	Actual year coded in BCD format
3 to 0		0 to 9	Unit place	

7.9.9 Setting and reading the time

Figure 10 shows the data flow and data dependencies starting from the 100 Hz/1 Hz clock tick.

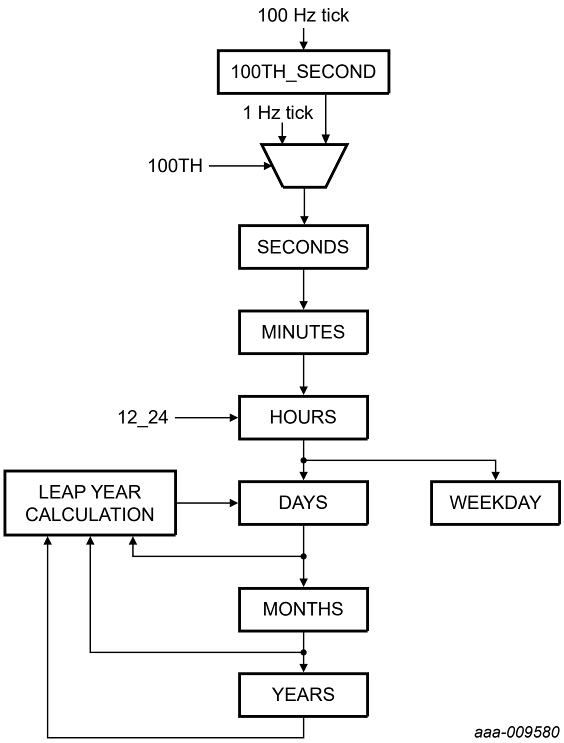


Figure 10. Data flow for the time function

Write access requires setting the STOP bit. The flow for accurately setting the time in RTC mode is:

1. Start an I2C access at register control_1
2. Set the STOP bit
3. Set CPR (register SR_RESET, CPR is logic 1)
4. The address counter rolls over to address 06h
5. Set time (100th seconds, seconds to years)
6. End I2C access
7. Wait for an external time reference to indicate the start of time counting
8. Start an I2C access at register control_1
9. Clear STOP bit (time starts counting from now)
10. End I2C access

The first increment of the time circuits is between 0 s and 122 ms after STOP is released. See description for STOP bit in Section 7.15.

During read operations, the time counting circuits (memory locations 06h through 0Dh) are blocked. It prevents:

1. Faulty reading of the clock and calendar during a carry condition
2. Incrementing the time registers during the read cycle

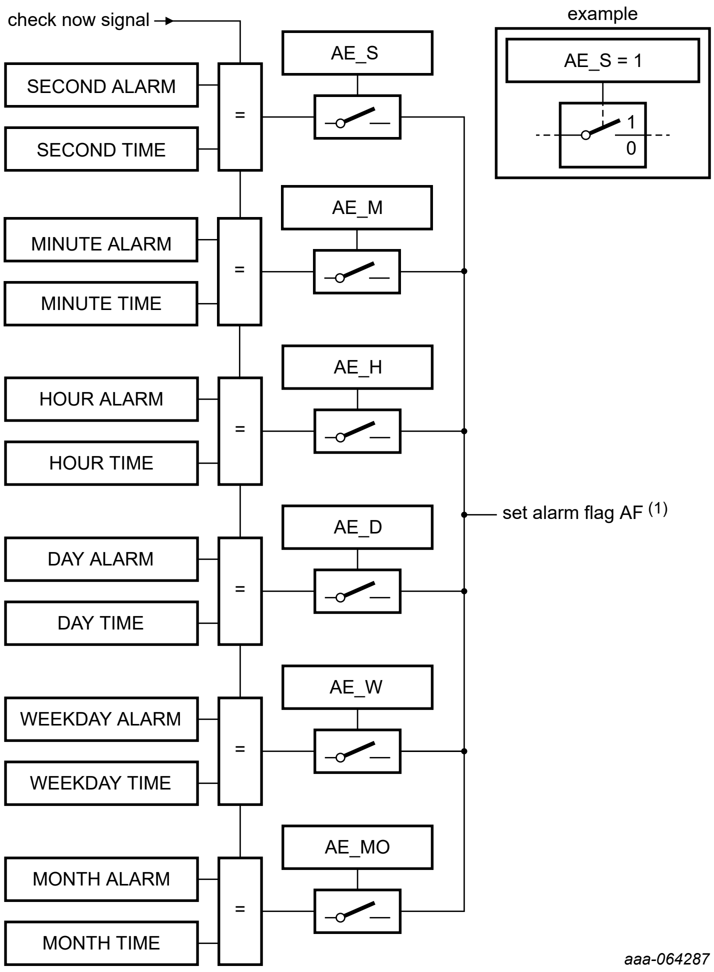
After this read access is completed, the time circuit is released again. Any pending request to increment the time counters that occurred during the read access is serviced.

As a consequence of this method, it is important to make a read access in one go. That is, reading seconds through to years must be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, a roll-over can occur between reads, therefore giving the minutes from one moment and the hours from the next. Therefore, it is advised to read all time and date registers in one access.

7.10 Alarm function

When one or more of the alarm bit fields are loaded with a valid second, minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the actual second, minute, hour, day, and weekday (see Figure 11).



Only when all enabled alarm settings are matching.

Figure 11. Alarm function block diagram

The generation of interrupts from the alarm function is described in Section 7.14.3.

7.10.1 Register Second_alarm

This section details the Second_alarm register, including its bit allocation and individual bit definitions.

Table 45. Second_alarm - second alarm register (address 0Eh) bit allocation
Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_S	SECOND_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 46. Second_alarm - second alarm register (address 0Eh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_S	0	-	A second alarm is enabled
		1	-	The second alarm is disabled
6 to 4	SECOND_ALARM	0 to 5	Tens place	Second alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.2 Register Minute_alarm

This section details the Minute_alarm register, including its bit allocation and individual bit definitions.

Table 47. Minute_alarm - minute alarm register (address 0Fh) bit allocation
Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_M	MINUTE_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 48. Minute_alarm - minute alarm register (address 0Fh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	Minute alarm is enabled
		1	-	Minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	Tens place	Minute alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.3 Register Hour_alarm

This section details the Hour_alarm register, including its bit allocation and individual bit definitions.

Table 49. Hour_alarm - hour alarm register (address 10h) bit allocation

Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_H	T	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			HOUR_ALARM (0 to 23) in 24-hour mode					
Reset value	1	0	0	0	0	0	0	0

Table 50. Hour_alarm - hour alarm register (address 10h) bit

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	Hour alarm is enabled
		1	-	Hour alarm is disabled
6	T	0	-	Unused
12-hour mode[1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM
4	HOUR_ALARM	0 to 1	Tens place	Hour alarm information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOUR_ALARM	0 to 2	Tens place	Hour alarm information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.10.4 Register Day_alarm

This section details the Day_alarm register, including its bit allocation and individual bit definitions.

Table 51. Day_alarm - day alarm register (address 11h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_D	T	DAY_ALARM (1 to 31)					
Reset value	1	0	0	0	0	0	0	0

Table 52. Day_alarm - day alarm register (address 11h) bit description

Bits labeled as - are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	Day alarm is enabled
		1	-	Day alarm is disabled
6	T	0	-	Unused
5 to 4	DAY_ALARM	0 to 3	Tens place	Day alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.5 Register Weekdays_alarm

This section details the Weekday_alarm register, including its bit allocation and individual bit definitions.

Table 53. Weekday_alarm - weekday alarm register (address 12h) bit allocation

Bits labeled as - are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_W	T	T	T	T	WEEKDAY_ALARM (0 to 6)		
Reset value	1	0	0	0	0	0	0	0

Table 54. Weekday_alarm - weekday alarm register (address 12h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7	AE_W	0	Weekday alarm is enabled
		1	Weekday alarm is disabled
6 to 3	T	0	Unused
2 to 0	WEEKDAY_ALARM	0 to 6	Weekday alarm information

7.10.6 Register Month_alarm

This section details the Month_alarm register, including its bit allocation and individual bit definitions.

Table 55. Month_alarm - month alarm register (address 13h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_Y	AE_MO	-	MONTH_ALARM (1 to 12)				
Reset value	1	1	0	0	0	0	0	0

Table 56. Month_alarm - month alarm register (address 13h) bit description

Bits labeled as - are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_Y	0	-	Year alarm is enabled
		1	-	Year alarm is disabled
6	AE_MO	0	-	Month alarm is enabled
		1	-	Month alarm is disabled
5	T	0	-	Unused
4 to 0	MONTH_ALARM	0 to 1	Tens place	Month alarm information coded in BCD format
		0 to 9	Unit place	

7.10.7 Register Year_alarm

This section details the Year_alarm register, including its bit allocation and individual bit definitions.

Table 57. Year_alarm - year alarm register (address 14h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	YEAR_ALARM (0 to 99)							
Reset value	0	0	0	0	0	0	0	0

Table 58. Year_alarm - year alarm register (address 14h) bit description

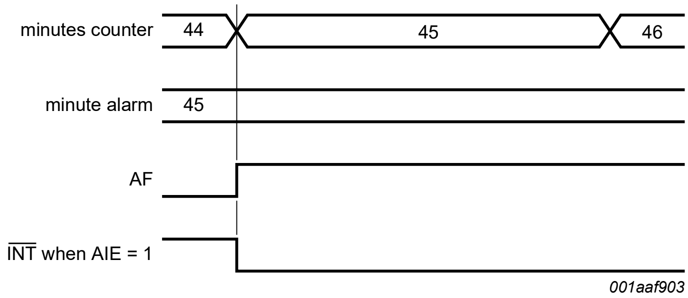
Bits labeled as - are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_ALARM	0 to 9	Tens place	Year alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.8 Alarm flag

When all enabled comparisons match for the first time, the alarm flag AF (register Control_2) is set. AF remains set until cleared by command. Once AF has been cleared, it is only set again when the time increments to match the alarm condition once more. For clearing the flags, see Section 7.11.

Alarm registers having their alarm enable bit AE_x at logic 1 are ignored.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 12. Alarm flag timing diagram

7.11 Clearing flags

Command can clear the flags MSF and AF. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

A write command clears a flag. Two examples are given for clearing the flags below:

- Bits labeled with '-' must be written with their previous values.
- Bits labeled with 'T' have to be written with logic 0.

Repeatedly rewriting these bits has no influence on the functional behavior.

Table 59. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	MSF	-	T	AF	T	-	-	T

Table 60. Example values in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	1	0	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

Table 61. Example to clear only AF (bit 4)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	0	0	0 [1]	0 [1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

Table 62. Example to clear only MSF (bit 7)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	1	1	0	0 [1]	0 [1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

7.12 Timestamp function

The PCF8525UK has an active low timestamp input pin TS, internally pulled with on-chip pullup resistors to Voper(int). It has a timestamp detection circuit, which can detect the event when input on pin TS is driven to the ground.

This Timestamp1 function is enabled by default after power on. It can be switched off by setting the control bit TSOFF (register Timestp_ctl1, register 16h to 1Ch).

The time recorded in the timestamps, when in 100 Hz disable mode (1 Hz mode), is at least two 16 Hz clocks behind the timestamp event and no more than three clocks behind. If the exact time of the timestamp event is required, then subtract 2 subseconds from the timestamp value and the result has -0 subseconds to +1 subseconds of uncertainty.

For a description of interrupt generation from the timestamp function, see Section 7.14.4.

The PCF8525UK also has a second timestamp (Timestamp2, register 1Dh to 23h). Whenever the calendar registers (06h to 0Dh) are written, their content is automatically copied into the timestamp2 registers (1Dh to 23h). Timestamp2 also has an uncertainty of -1 subseconds to +1 subseconds. Recording the RTC calendar write event in such fashion in timestamp2 serves two purposes:

1. It can serve as a security feature. The MCU can maintain a local copy/log of when the RTC calendar was last written. At a later point in time, the CPU can read the timestamp2 registers to verify if it matches with the last write event in its log. If it matches, the RTC time is secure and not tampered. If there is a mismatch, some other I2C controller has altered/tampered with the RTC time, and it is not reliable.
2. It can be used for time accuracy adjustment. If there is an accurate time source available, the MCU can calculate the offset between the accurate time and the current RTC time. The drift of the RTC can then be calculated in ppm and used to apply an equivalent offset correction using the Offset registers (26h and 27h).

7.12.1 Timestamp flag

When the TS input pin is driven to the ground, the following sequence occurs:

1. The actual date and time are stored in the timestamp registers.
2. The timestamp flag TSF flag is set.
3. If the TSIE bit is active, and the corresponding interrupt mask is disabled, an interrupt on the $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ pin is generated.

Command can clear the TSF flag. Clearing the flag clears the interrupt. Once the TSF is cleared, it is only set again when the TS pin is driven to ground once again.

7.12.2 Timestamp mode

The timestamp function has two different modes selected by the control bit TSM (timestamp mode) in register Timestp_ctl:

- If TSM is logic 1: In subsequent trigger events without clearing the timestamp flags, the first timestamp event is stored.

- If TSM is logic 0 (default): In subsequent trigger events without clearing the timestamp flags, the last timestamp event is stored.

7.12.3 Timestamp registers

This section covers the bit allocation and its description for various timestamp registers.

7.12.3.1 Register Timestp_ctl1

This section details the Timestp_ctl1 register, including its bit allocation and individual bit definitions.

Table 63. Timestp_ctl1 - timestamp control register (address 16h) bit allocation
Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]				
Reset value	0	0	0	0	0	0	0	0

Table 64. Timestp_ctl1 - timestamp control register (address 16h) bit description
Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7	TSM	0	In subsequent events without clearing the timestamp flags, the last event is stored
		1	In subsequent events without clearing the timestamp flags, the first event is stored
6	TSOFF	0	Timestamp function active
		1	Timestamp function disabled
5	-	0	Unused
4 to 0	SUBSEC_TIMESTP[4:0] [1]		$^1\!/_{16}$ second timestamp information coded in BCD format when 100TH_S_DIS = ‘1’, $^1\!/_{20}$ second timestamp information coded in BCD format when 100TH_S_DIS = ‘0’

[1] The time recorded in the timestamps, when in 100 Hz disable mode (1 Hz mode), is at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of timestamp event is required, subtract 2 subseconds from the timestamp value. Now, the result has -0 subseconds to +1 subseconds of uncertainty.

7.12.3.2 Register Subsec_Timstp2

This section details the Subsec_Timstp2 register, including its bit allocation and individual bit definitions.

Table 65. Subsec_Timstp2 – sub-second timestamp2 register (address 1Dh) bit allocation
Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	SUBSEC_TIMESTP[4:0]				
Reset value	0	0	0	0	0	0	0	0

Table 66. Subsec_Timstp2 – sub-second timestamp2 register (address 1Dh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 5	T	-	Unused
4 to 0	SUBSEC_TIMESTP[4:0] [1]		$^{1}/_{16}$ second timestamp information coded in BCD format when 100TH_S_DIS = ‘1’, $^{1}/_{20}$ second timestamp information coded in BCD format when 100TH_S_DIS = ‘0’

[1] The time recorded in the timestamps, when in 100 Hz disable mode (1 Hz mode), is at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of the timestamp event is required, then subtract 2 subseconds from the timestamp value. Now, the result has -0 subseconds to +1 subseconds of uncertainty.

7.12.3.3 Register Sec_timestp

This section details the Sec_timestp register, including its bit allocation and individual bit definitions.

Table 67. Sec_timestp1/2 - second timestamp register (address 17h/1Eh) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	SECOND_TIMESTP (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 68. Sec_timestp1/2 - second timestamp register (address 17h/1Eh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	Unused
6 to 4	SECOND_ TIMESTP	0 to 5	Tens place	Second timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.4 Register Min_timestp

This section details the Min_timestp register, including its bit allocation and individual bit definitions.

Table 69. Min_timestp1/2 - minute timestamp register (address 18h/1Fh) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	MINUTE_TIMESTP (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 70. Min_timestp1/2 - minute timestamp register (address 18h/1Fh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	Unused
6 to 4	MINUTE_TIMESTP	0 to 5	Tens place	Minute timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.5 Register Hour_timestp

This section details the Hour_timestp register, including its bit allocation and individual bit definitions.

Table 71. Hour_timestp1/2 - hour timestamp register (address 19h/20h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
			HOUR_TIMESTP (0 to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

Table 72. Hour_timestp1/2 - hour timestamp register (address 19h/20h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	Unused
12-hour mode [1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM
4	HOUR_TIMESTP	0 to 1	Tens place	Hour timestamp information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOUR_TIMESTP	0 to 2	Tens place	Hour timestamp information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.12.3.6 Register Day_timestp

This section details the Day_timestp register, including its bit allocation and individual bit definitions.

Table 73. Day_timestp1/2 - day timestamp register (address 1Ah/21h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAY_TIMESTP (1 to 31)					

Table 73. Day_timestp1/2 - day timestamp register (address 1Ah/21h) bit allocation...*continued*

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 74. Day_timestp1/2 - day timestamp register (address 1Ah/21h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
5 to 4	DAY_TIMESTP	0 to 3	Tens place	Day timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.7 Register Mon_timestp

This section details the Mon_timestp register, including its bit allocation and individual bit definitions.

Table 75. Mon_timestp1/2 - month timestamp register (address 1Bh/22h) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTHS (1 to 12)				
Reset value	0	0	0	0	0	0	0	0

Table 76. Mon_timestp1/2 - month timestamp register (address 1Bh/22h) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	Unused
4	MONTH_ TIMESTP	0 to 1	Tens place	Month timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.8 Register Year_timestp

This section details the Year_timestp register, including its bit allocation and individual bit definitions.

Table 77. Year_timestp1/2 - year timestamp register (address 1Ch/23h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	YEARS (0 to 99)							
Reset value	0	0	0	0	0	0	0	0

Table 78. Year_timestp1/2 - year timestamp register (address 1Ch/23h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_TIMESTP	0 to 9	Tens place	Year timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.13 Random code registers

The R-code registers (24h and 25h) are two-byte random numbers and read only for security application. It takes a maximum of 200 µs to generate the R-code after a timestamp2 event.

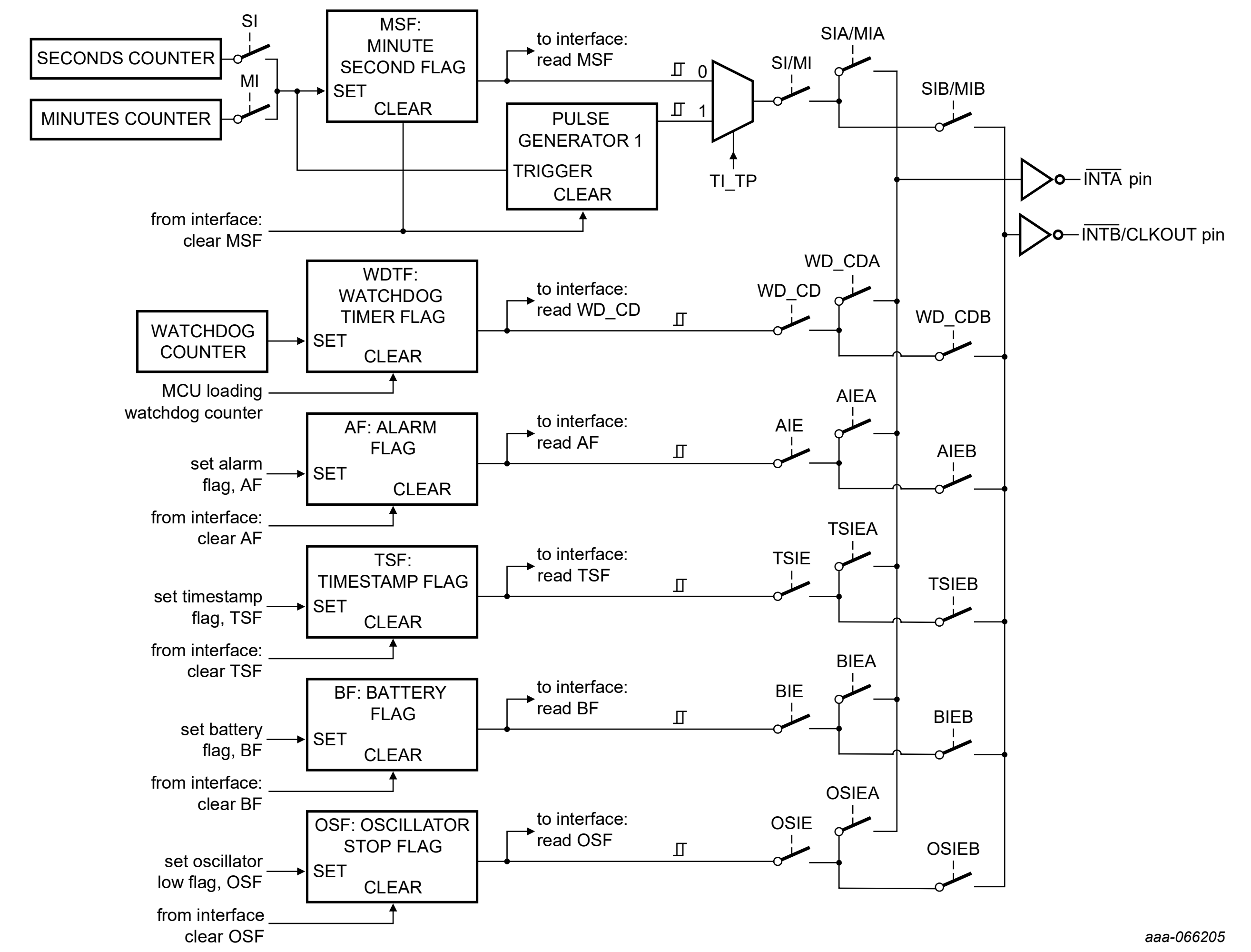
7.14 Interrupt outputs

PCF8525UK has two interrupt output pins, $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$, which are open-drain, active LOW (requiring a pullup resistor if used). Interrupts can be sourced from different places:

- Second or minute timer
- Alarm
- Timestamp
- Battery switch-over

The control bit TI_TP (register Control_2) is used to configure whether the interrupts generated from the second/minute timer (flag MSF in register Control_2) are pulsed signals or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags. When the interrupt sources are all disabled, $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ remain high-impedance.

Command can clear the flags MSF, AF, TSF, and BF.



When all the interrupts are disabled, INTA and INTB/CLKOUT remain high-impedance.

Figure 13. Interrupt block diagram

7.14.1 Minute and second interrupts

Predefined timers generate minute and second interrupts. The timers can be enabled independently from one another by the bits MI and SI in register Control_1. However, a minute interrupt enabled on top of a second interrupt cannot be distinguishable since it occurs at the same time.

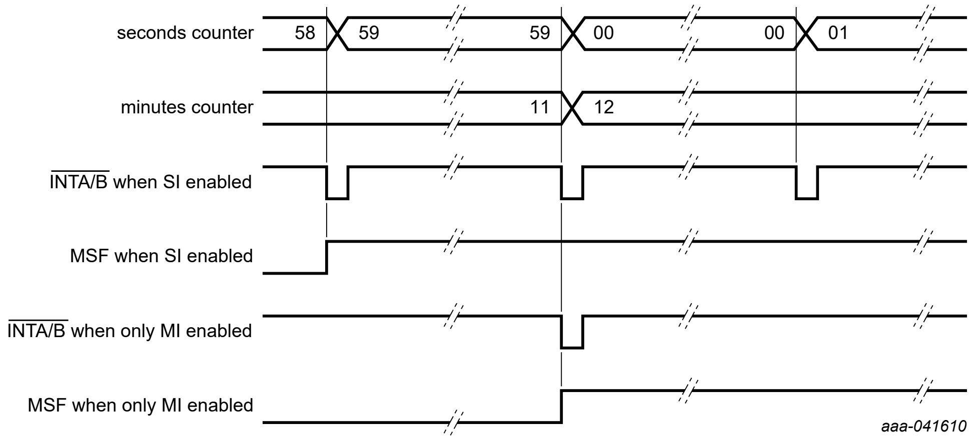
The minute/second flag MSF (register Control_2) is set logic 1 when either the seconds or the minutes counter increments according to the enabled interrupt (see Table 79). Command can clear the MSF flag.

Table 79. Effect of bits MI and SI on pins INTA, INTB, and bit MSF

MI	SI	Result in INTA/INTB	Description
0	0	No interrupt generated	MSF is never set
1	0	An interrupt once per minute	MSF is set when **minutes** counter increments
0	1	An interrupt once per second	MSF is set when **seconds** counter increments
1	1	An interrupt once per second	MSF is set when **seconds** counter increments

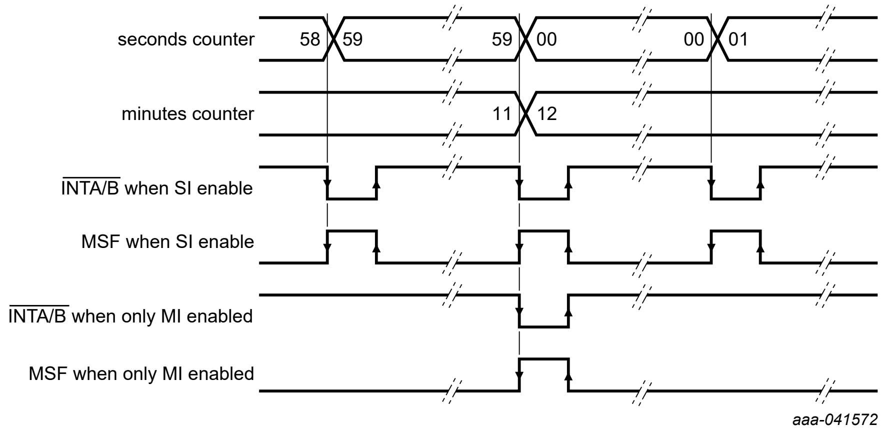
When MSF is set logic 1:

- If TI_TP is logic 1, the interrupt is generated as a pulsed signal if not masked.
- If TI_TP is logic 0, the interrupt is a permanently active signal that remains until MSF is cleared.



In this example, bit TI_TP is logic 1 and the MSF flag is not cleared after an interrupt.

Figure 14. INT example for SI and MI when TI_TP is logic 1



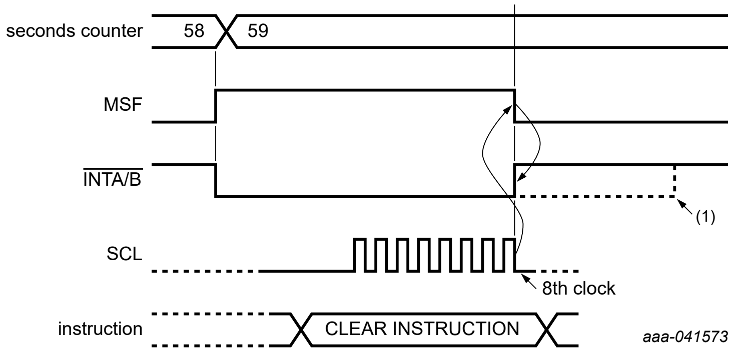
In this example, bit TI_TP is logic 0 and the MSF flag is not cleared after an interrupt.

Figure 15. INT example for SI and MI when TI_TP is logic 0

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and generates a pulse of 1⁄64 seconds in duration.

7.14.2 INT pulse shortening

If the MSF flag (register Control_2) is cleared before the end of the INT pulse, then the INT pulse is shortened. This situation allows the source of a system interrupt to be cleared immediately when it is serviced. The system does not have to wait for the completion of the pulse before continuing; see Figure 16. Instructions for clearing the bit MSF can be found in Section 7.11.



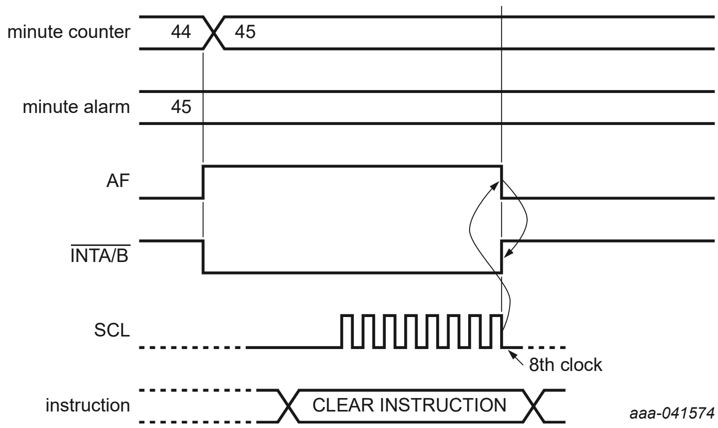
1. Indicates normal duration of INT pulse.

The timing shown for clearing bit MSF is also valid for the non-pulsed interrupt mode, that is, when TI_TP is logic 0, where the INT pulse can be shortened by setting both bits MI and SI logic 0.

Figure 16. Example of shortening the INT pulse by clearing the MSF flag

7.14.3 Alarm interrupts

The bit AIE (register Control_2) controls the generation of interrupts from the alarm function. If AIE is enabled, the INTA/INTB pin follows the status of bit AF (register Control_2) if not masked. Clearing AF immediately clears INTA/INTB. No pulse generation is possible for alarm interrupts.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 17. AF timing diagram

7.14.4 Timestamp interrupts

Interrupt generation from the timestamp function is controlled using the TSIE bit (register Control_5). If TSIE is enabled, the INTA/INTB pin follows the status of the flags TSF, if not masked. Clearing the flags TSF immediately clears INTA/INTB. No pulse generation is possible for timestamp interrupts.

7.14.5 Battery switch-over interrupts

The BIE bit (register Control_3) controls the generation of interrupts from the battery switch-over. If BIE is enabled, the INTA/INTB pin follows the status of bit BF in register Control_3 if not masked. Clearing BF immediately clears INTA/INTB. No pulse generation is possible for battery switch-over interrupts.

7.14.6 Oscillator stop interrupts

Interrupt generation from the oscillator stop detection function is controlled using the OSIE bit (register Control_3). If OSIE is enabled, the $\overline{INTA}/\overline{INTB}$ pin follows the status of the OSF flag, if not masked. The OSF enabled bits further gate this interrupt function. When OSFE[1:0] = 00 (OSF detection function disabled), setting OSIE = 1 does not affect.

7.14.7 Interrupt masks

This section details the Interrupt masks register, including its bit allocation and individual bit definitions.

Table 80. INTA/B_MASK1 - interrupt mask 1 register (address 28h/2Ah) bit allocation
Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INTA_MASK1							
Reset value	0	0	1	1	1	1	1	1

Table 81. INTA/B_MASK1 - interrupt mask 1 register (address 28h/2Ah) bit description
Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 6	T	00	Unused
5	MI	1	A minute interrupt mask
4	SI	1	A second interrupt mask
3	OSIE	1	OSF interrupt mask
2	AIE	1	Alarm interrupt mask
1	BIE	1	Battery flag interrupt mask
0	WD_CD	1	Watchdog interrupt mask

Table 82. INTA/B_MASK2 - interrupt mask 2 register (address 29h/2Bh) bit allocation
Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INTA_MASK2							
Reset value	0	0	0	0	1	0	0	0

Table 83. INTA/b_MASK2 - interrupt mask 2 register (address 29h/2Bh) bit description
Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	T	0000	Unused
3	TSIE	1	Timestamp interrupt mask

Table 83. INTA/b_MASK2 - interrupt mask 2 register (address 29h/2Bh) bit description*...continued*

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
2	T	0	Unused
1	T	0	Unused
0	T	0	Unused

The registers at addresses 28h to 2Bh are used to configure interrupt source for $\overline{\text{INTA}}$/$\overline{\text{INTB}}$ pin.

All of above interrupts could be masked from $\overline{\text{INTA}}$/$\overline{\text{INTB}}$, with corresponding bit set to '1', as shown in Figure 13.

7.15 Watchdog timer functions

The PCF8525UK has a watchdog timer function. The timer can be switched on and off by using the control bit WD_CD in the register Watchdg_tim_ctl. The watchdog timer has four selectable source clocks. It can, for example, be used to detect a microcontroller with interrupt and reset capability, which is out of control (see Section 7.15.3).

To control the timer function and timer output, the registers Control_2, Watchdg_tim_ctl, and Watchdg_tim_val are used.

7.15.1 Register Watchdg_tim_ctl

Table 5 and Table 6 describe the bit allocation and bit description of the Watchdg_tim_ctl register, respectively.

Table 84. Watchdg_tim_ctl - watchdog timer control register (address 2Ch) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	WD_CD	-	-	-	-	-	TF[1:0]	
Reset value	0	0	0	0	0	0	1	1

Table 85. Watchdg_tim_ctl - watchdog timer control register (address 2Ch) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7	WD_CD	0	Watchdog timer interrupt disabled
		1	Watchdog timer interrupt enabled; the interrupt pin $\overline{\text{INTA}}$/$\overline{\text{INTB}}$ is activated when timed out
6 to 2	-	0	Unused
1 to 0	TF[1:0]		Timer source clock for watchdog timer
		00	64 Hz
		01	4 Hz
		10	1⁄4 Hz
		11	1⁄64 Hz

7.15.2 Register Watchdg_tim_val

Table 86 and Table 87 describe the bit allocation and bit description of the Watchdg_tim_val register, respectively.

Table 86. Watchdg_tim_val - watchdog timer value register (address 2Dh) bit allocation

Bits labeled as - are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDG_TIM_VAL[7:0]							
Reset value	0	0	0	0	0	0	0	0

Table 87. Watchdg_tim_val - watchdog timer value register (address 2Dh) bit description

Bits labeled as - are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 0	WATCHDG_TIM_ VAL[7:0]	00 to FF	Timer period (in seconds): $$TimerPeriod = \frac{(n-1)+/-0.5}{SourceClockFrequency} \quad (1)$$ Here, n is the timer value (n > 1). Write only

Table 88. Programmable watchdog timer

TF[1:0]	Timer source clock frequency	Unit	Minimum timer period (n = 2)	Unit	Maximum timer period (n = 255)	Unit
00	64	Hz	15.625	ms	3.984	s
01	4	Hz	250	ms	63.744	s
10	1⁄4	Hz	4	s	1020	s
11	1⁄64	Hz	64	s	16320	s

7.15.3 Watchdog timer function

The WD_CD bit of the register Watchdg_tim_ctl enables or disables the watchdog timer interrupt function (see Table 85).

The 2 bits (TF[1:0]) in register Watchdg_tim_ctl determine one of the four source clock frequencies for the watchdog timer: 64 Hz, 4 Hz, 1⁄4 Hz or 1⁄64 Hz (see Table 85).

When the watchdog timer function is enabled, the 8-bit timer in register Watchdg_tim_val determines the watchdog timer period (see Table 88).

The watchdog timer counts down from the software programmed 8-bit binary value n in register Watchdg_tim_val. When the counter reaches 1, the watchdog timer flag WDTF (register Control_2) is set to logic 1, and an interrupt is generated. The period accuracy corresponds to n ± 0.5.

The register Watchdg_tim_val is write only and not readable after set.

The counter does not automatically reload.

When WD_CD is logic 1/0 (watchdog timer interrupt enabled/disabled) and the microcontroller unit loads a watchdog timer value n, then:

- Flag WDTF is reset.
- $\overline{INTA}/\overline{INTB}$ is cleared.
- The watchdog timer starts again.

Loading the counter with 0 or 1 will:

1. Reset the flag WDTF.
2. Clear $\overline{INTA}/\overline{INTB}$.
3. Stop the watchdog timer.

WDTF can be cleared by:

1. Loading a value in register Watchdg_tim_val.
2. Writing a logic 0 to WDTF.
3. When the watchdog timer counter reaches 1, the watchdog timer flag WDTF is set logic 1.
4. When a minute or second interrupt occurs, the minute/second flag MSF is set to logic 1 (see Section 7.14.1).

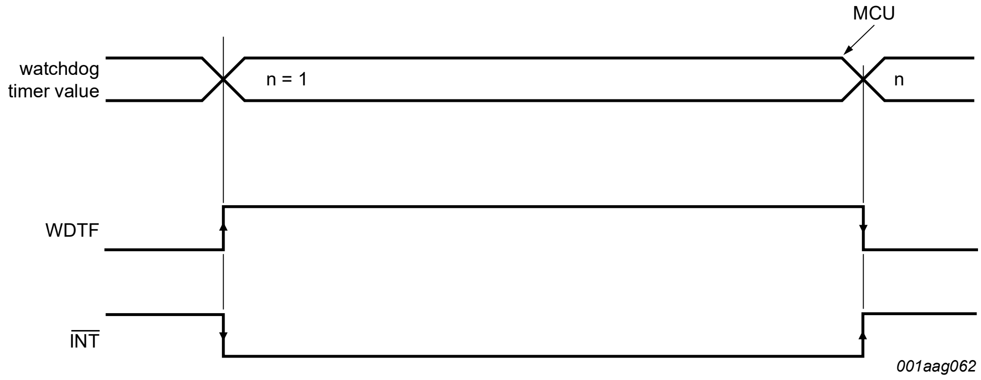


Figure 18. WD_CD set logic 1 watchdog activates an interrupt when timed out

7.15.4 Predefined timers: Second and minute interrupt

PCF8525UK has two predefined timers, which are used to generate an interrupt either once per second or once per minute (see Section 7.14.1). The pulse generator for the minute or second interrupt operates from an internal 64 Hz clock. It is independent of the watchdog timer. The bits SI (second interrupt) and MI (minute interrupt) in register Control_1 can enable each of these timers.

7.15.5 Clearing flags

The command can clear the flags MSF and AF. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Two examples are given for clearing the flags. Clearing a flag is made by a write command:

- Bits labeled with '-' must be written with their previous values.
- Bits labeled with 'T' have to be written with logic 0.
- WDTF must be written with logic 0 to clear the flag.

Repeatedly rewriting these bits has no influence on the functional behavior.

Table 89. Flag location in register Control_2

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	T	AF	T	-	-	T
Example value	1	0	1	1	0	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

Table 90. Example to clear only AF (bit 4)

Bit	7	6	5	4	3	2	1	0
Reset value	1	0	1	0	0	0[1]	0 [1]	0

[1] The bits labeled as '-' have to be rewritten with the previous values.

Table 91. Example to clear only MSF (bit 7)

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	1	1	0	0 [1]	0 [1]	0

[1] The bits labeled as '-' have to be rewritten with the previous values.

7.16 STOP bit function

The STOP bit stops the time from counting in the RTC. STOP must be set to unlock the time and date registers to set the time.

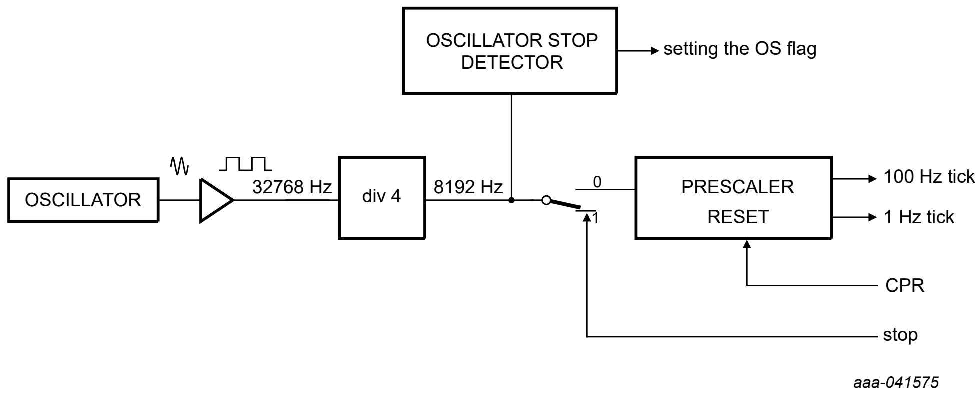


Figure 19. CPR and STOP bit functional diagram

The stop signal blocks the 8.192 kHz clock from generating system clocks and freezes the time. In this state, the prescaler can be cleared with the CPR command in the Resets register.

Note: *The CLKOUT output of clock frequencies is not affected.*

The time circuits can then be set and do not increment until the STOP bit is released. There is a slight chance that STOP is set during a carry over of multiple time registers, which can have incomplete execution. Therefore, a time must be set before clearing STOP to maintain time integrity.

The stop acts on the 8.192 kHz signal. Because the I2C-bus or TS pin input is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero, and one 8.192 kHz cycle (see Figure 20).

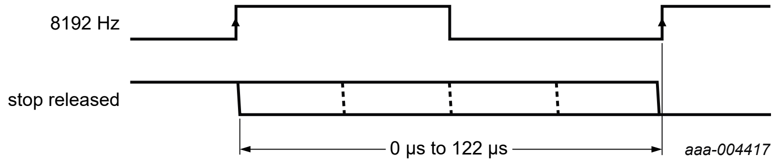


Figure 20. STOP release timing

7.17 I2C-bus interface

The I2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are SDA and SCL. Both lines are connected to a positive supply by a pullup resistor. Data transfer is initiated only when the bus is not busy.

7.17.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line are now interpreted as control signals.

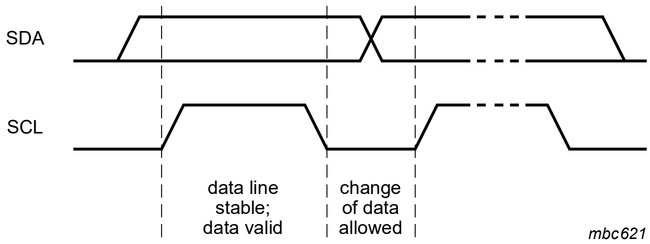


Figure 21. Bit transfer

7.17.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition S. A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition P.

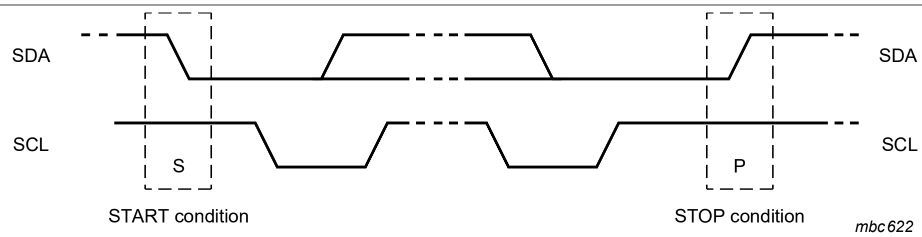


Figure 22. Definition of START and STOP conditions

7.17.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the controller; and the devices that are controlled by the controller are the targets.

The PCF8525UK can act as a target transmitter and a target receiver.

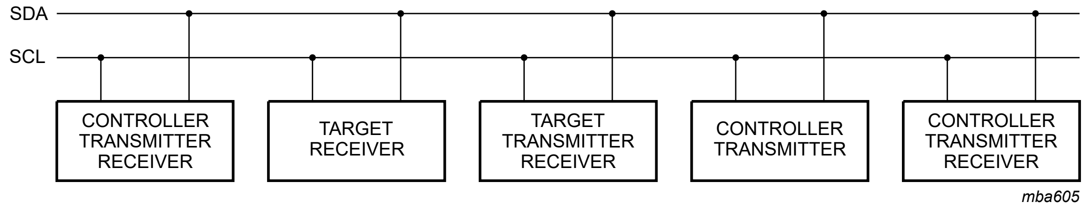


Figure 23. System configuration

7.17.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A target receiver that is addressed must generate an acknowledge after the reception of each byte.
- A controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

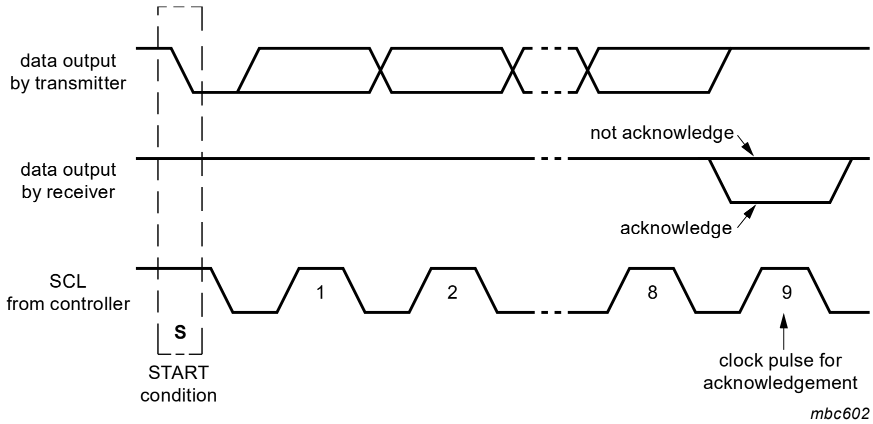


Figure 24. Acknowledgment on the I2C-bus

7.17.5 I2C-bus protocol

After a start condition, a valid hardware address has to be sent to a PCF8525UK device. The appropriate I2C-bus target address is 1010 001. The entire I2C-bus target address byte is shown in Table 92.

Table 92. I2C target address byte

Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	1	0	1	0	0	0	1	R/W

The R/W bit defines the direction of the following single or multiple byte data transfers (read is logic 1, write is logic 0).

For the format and the timing of START condition (S), STOP condition (P), and acknowledge (A), refer to the I2C-bus specification and the characteristics table (Table 96). In the write mode, a data transfer is terminated by sending a STOP condition.

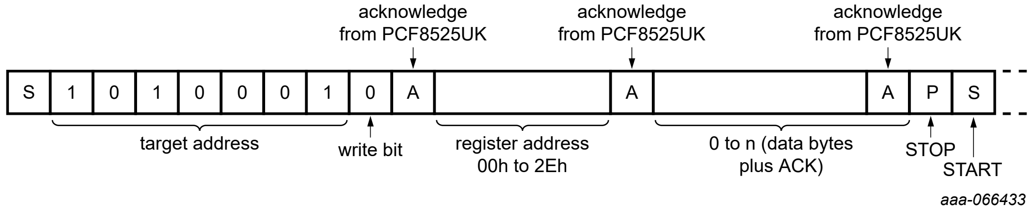


Figure 25. Bus protocol, writing to registers

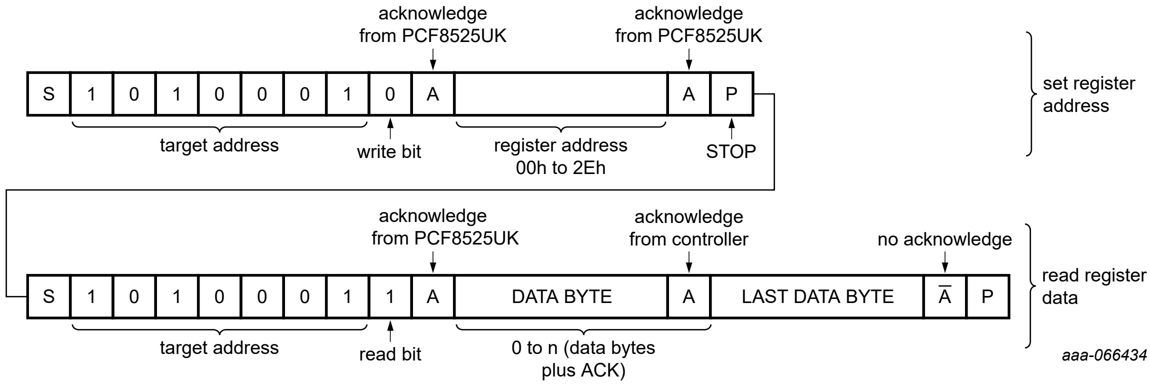


Figure 26. Bus protocol, reading from registers

7.17.6 I2C-bus communication and battery backup operation

To save power during battery backup operation (see Section 7.5.1), the I2C-bus interface is inactive. Therefore, the communication via I2C must be terminated before the supply of the PCF8525UK is switched from VDD to VBAT.

The PCF8525UK terminates the transaction before switching from VDD to VBAT.

If the I2C-bus communication was terminated uncontrollably, the I2C-bus has to be reinitialized by sending a STOP followed by a START after the device switched back from battery backup operation to VDD supply operation.

8 Limiting values

Table 93 describes the limiting values of PCF8525UK.

Table 93. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		-0.5	+6.5	V
V_{BAT}	Battery supply voltage		-0.5	+6.5	V
V_{IO}	Voltage on all other pins	$\overline{\text{INTA}}$, $\overline{\text{INTB}}$/CLKOUT, SCL, SDA, TS	-0.5	+6.5	V
V_{OSC}	Voltage on oscillator pins	OSCI, OSCO	-0.5	+2.0	V
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) JS-001-2017; all pins	-	±2000	V
		Charge Device Model (CDM) JEDEC JS-002-2018; all pins	-	±500	V
I_{lu} (IO)	Latch-up current	JESD78: -0.5 x VDD < VI < 1.5 x VDD; Tj = 85 °C	-100	100	mA
T_{stg}	Storage temperature		-55	+125	°C

Note: *The PCF8525UK part is not guaranteed (or characterized) above the operating range as denoted in the data sheet. NXP recommends not to bias the PCF8525UK device during reflow (for example, if using a* ***coin*** *type battery in the assembly). If chosen to use this assembly method, there must be an allowance for a full* ***0 V level power supply reset*** *to re-enable the device. Without a proper POR, the device can remain in an indeterminate state.*

9 Recommended operating conditions

Table 94 describes the operating conditions of PCF8525UK.

Table 94. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	Supply voltage		1.2	5.5	V
VBAT	Supply voltage battery		1.2	5.5	V
T_{amb}	Ambient temperature	Operating	-40	+85	°C

10 Static characteristics

Table 95 describes the static characteristics of PCF8525UK.

Table 95. Static characteristics

T_{amb} = -40 °C to +85 °C; V_{DD} = 1.2 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	Supply voltage		[1]	1.2	-	5.5	V
V_{BAT}	Battery supply voltage			1.2	-	5.5	V
$V_{DD\ CLK}$	Clock supply voltage		[2]	0.9	-	5.5	V
V_{LOW}	Low voltage detection (VLF flag)			0.9	-	1.2	V
I_{DD}	Supply current[3]	Interface active; supplied by V_{DD}					
		I2C-bus (f_{SCL} = 400 kHz)		-	-	200	µA
		Interface inactive (f_{SCL} = 0 Hz)[4]; TCR[2:0] = 000 (see Table 16)					
		PWRMNG[1:0] = 11 (see Table 21); COF[2:0] = 111 (see Table 17) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V		-	88	380	nA
		V_{DD} = 3.3 V		-	64	340	nA
		V_{DD} = 5.5 V		-	71	430	nA
		PWRMNG[1:0] = 11 (see Table 21); COF[2:0] = 000 (see Table 17) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V	[5]	-	460	910	nA
		V_{DD} = 3.3 V	[5]	-	1035	1470	nA
		V_{DD} = 5.5 V	[5]	-	1670	2210	nA
		PWRMNG[1:0] = 00 (see Table 21); COF[2:0] = 111 (see Table 17) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V		-	118	550	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V		-	104	550	nA
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V		-	107	660	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	104	550	nA
		V_{BAT} = 3.3 V, I_{BAT}	[6]	-	83	510	nA
		V_{BAT} = 5.5 V, I_{BAT}	[6]	-	91	610	nA
		PWRMNG[1:0] = 00 (see Table 21) COF[2:0] = 000 (see Table 17) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V	[5]	-	640	1070	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V	[5]	-	1060	1500	nA

Table 95. Static characteristics*...continued*

T_{amb} = -40 °C to +85 °C; V_{DD} = 1.2 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V	[5]	-	1705	2230	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	130	570	nA
		V_{BAT} = 3.3 V, I_{BAT}	[6]	-	145	560	nA
		V_{BAT} = 5.5 V, I_{BAT}	[6]	-	210	720	nA
$I_{L(bat)}$	Battery leakage current	V_{DD} is active supply; V_{BAT} = 3.0 V		-	0.1	-	nA
Power management							
$V_{th(sw)bat}$	Battery switch threshold voltage			1.25	1.45	1.6	V
Inputs [7]							
V_I	Input voltage			-0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage			-	-	0.25V_{DD}	V
		T_{amb} = -40 °C to +85 °C; V_{DD} > 2.0 V		-	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
I_{LI}	Input leakage current	V_O = V_{DD} or V_{SS}		-1	-	+1	μA
C_i	Input capacitance		[8]	-	-	7	pF
Outputs							
V_O	Output voltage	On pins $\overline{INTA}$ and $\overline{INTB}$, referring to the external pullup		-0.5	-	5.5	V
V_{OH}	HIGH output voltage	On pins $\overline{INTB}$/CLKOUT and $\overline{INTA}$, at 1 mA source current		0.8V_{DD}	-	VDD	V
V_{OL}	LOW output voltage	On pins $\overline{INTB}$/CLKOUT and $\overline{INTA}$, at 1 mA sink current		VSS	-	0.2V_{DD}	V
		On pin SDA, V_{DD} > 2.0 V, 3 mA sink current		-	-	0.4	V
		On pin SDA, V_{DD} < 2.0 V, 2 mA sink current		-	-	0.2V_{DD}	V
I_{OL}	LOW-level output current	Output sink current; V_{OL} = 0.4 V					
		On pin SDA		3	-	-	mA
		On all other outputs		1.0	-	-	mA
I_{OH}	HIGH-level output current	Output source current on CLKOUT		1.0	-	-	mA
I_{LO}	Output leakage current	V_O = V_{DD} or V_{SS}		-1	-	+1	μA
Oscillator							
Δf/ΔV	Frequency variation with voltage	On pin CLKOUT		-	±1	-	ppm/V
Jitter	Output clock peak-to-peak jitter	On pin CLKOUT		-	70	-	ns

Table 95. Static characteristics*...continued*

T_{amb} = -40 °C to +85 °C; V_{DD} = 1.2 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_L	Integrated load capacitance	On pins OSCO, OSCI; V_{DD} = 3.3 V	[9]	6.5	7	7.5	pF

[1] For reliable oscillator startup and OTP refresh at power on, VDD must be above 1.8 V.
[2] Timekeeping (oscillator and date/time) is working down to 0.9 V. Power management functions, interrupts, and I2C interface are not functional below 1.2 V.
[3] Max IDD and IBAT determined by characterization.
[4] Timer source clock = 1⁄60 Hz, level of pins SDA and SCL is VDD.
[5] Any load in the application driven by CLKOUT adds to this value. For example, 10 pF, VDD = 3V3 adds 32768 Hz * 10 pF * 3.3 V = 1.1 µA.
[6] When the device is supplied by the VBAT pin instead of the VDD pin, the VDD = 0 V. The device can only start up from VDD.
[7] The I2C-bus of PCF8525UK is 5 V tolerant.
[8] Tested on a sample basis.
[9] $C_L = (C_{OSCI} * C_{OSCO})/(C_{OSCI} + C_{OSCO})$

11 Dynamic characteristics

Table 96 describes the static characteristics of PCF8525UK.

Table 96. I2C-bus interface dynamic characteristics[1]

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of VSS to VDD (see Figure 27).

Symbol	Parameter	Conditions	Fast Mode		Unit
			Min	Max	
Pin SCL					
f_{SCL}	SCL clock frequency	[2]	1	400	kHz
t_{LOW}	LOW period of the SCL clock	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	-	0.6	-	µs
t_{TO}	SMBus SCL timeout	[3]	25	35	ms
Pin SDA					
$t_{SU;DAT}$	Data set-up time	-	100	-	ns
$t_{HD;DAT}$	Data hold time	[4]	0	-	ns
Pins SCL and SDA					
t_{BUF}	Bus free time between a STOP and START condition	-	1.3	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	-	0.6	-	µs
$t_{HD;STA}$	Hold time (repeated) START	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	-	0.6	-	µs
t_r	Rise time of both SDA and SCL signals	[5]	20 + 0.1Cb	300	ns
t_f	Fall time of both SDA and SCL signals	[6]	20 + 0.1Cb	300	ns
C_b	Capacitive load for each bus line	-	-	400	pF
$t_{VD;ACK}$	Data valid acknowledge time	[6]	-	0.9	µs
$t_{VD;DAT}$	Data valid time	[7]	-	0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	[8]	-	50	ns

[1] These specifications are guaranteed by design and not tested in production.
[2] The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if either the SCL or SDA is held low for a minimum of 25 ms. The bus timeout feature must be disabled for DC operation.
[3] Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of tTO(min). After the controller in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than tTO(max).
[4] A controller device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the VIL of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum tf for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, tf is 250 ns. These values allow series protection resistors to be connected between the SDA pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum tf.
[6] tVD;ACK = time for acknowledgment signal from SCL LOW to SDA output LOW.
[7] tVD;DAT = minimum time for valid SDA output following SCL LOW.
[8] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

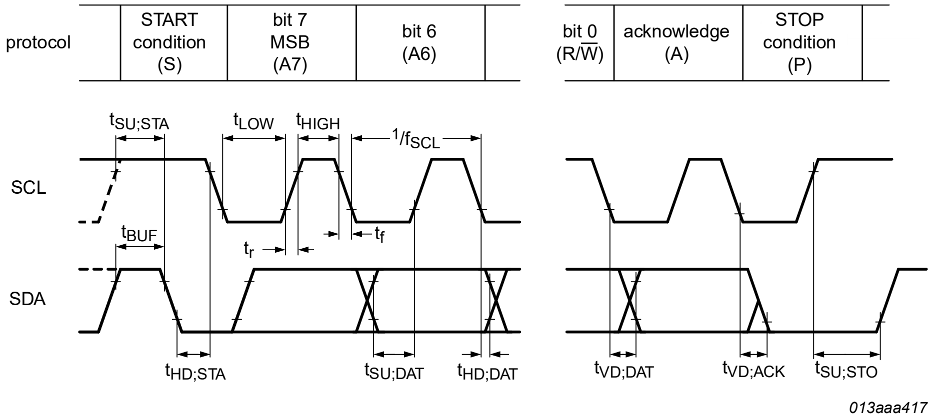


Figure 27. I2C-bus timing diagram; rise and fall times refer to 30 % and 70 %

12 Recommended crystal parameters

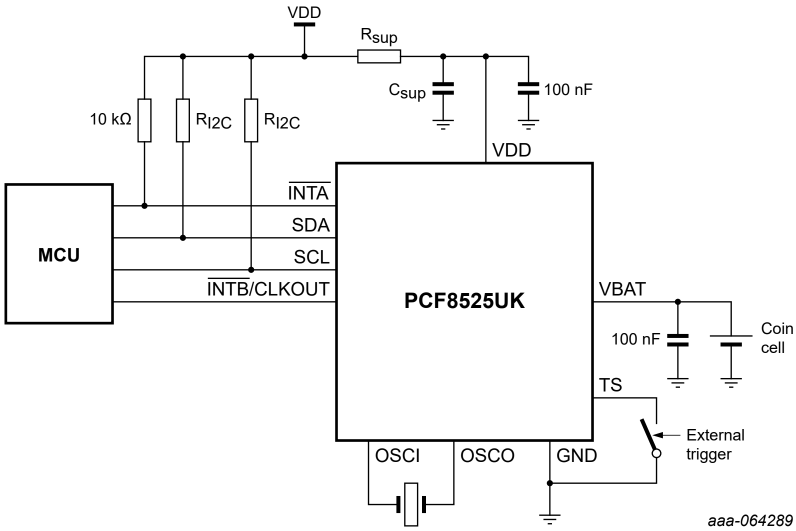
Table 97 describes the recommended crystal parameters of PCF8525UK.

Table 97. Crystal parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_O	Nominal frequency			32768		Hz
ESR	Equivalent Series Resistance				80	kΩ
C_L	Load capacitance			7		pF

13 Application information

Figure 28 shows the detailed application diagram for PCF8525UK.



$R_{I2C(max)}$ = tr/Cb

R_{SUP} and C_{SUP}: An appropriate RC filter must be added to guarantee that the chip only sees < 0.35 V/ms ramp down rate on VDD.

Figure 28. General application diagram

14 Package information

14.1 Package outline: WLCSP12 SOT1390-13

This section shows the package outline for the PCF8525UK.

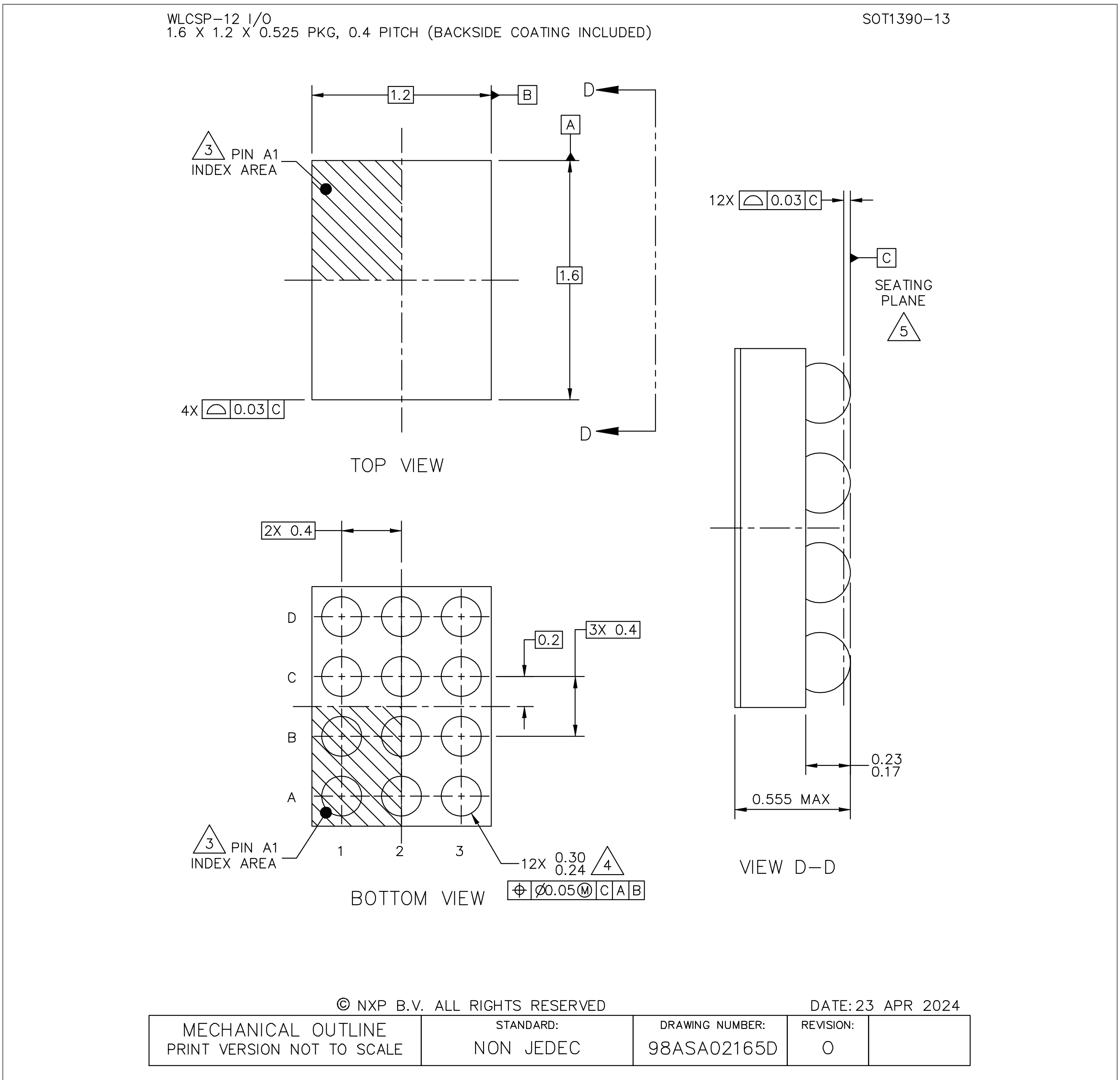


Figure 29. SOT1390-13

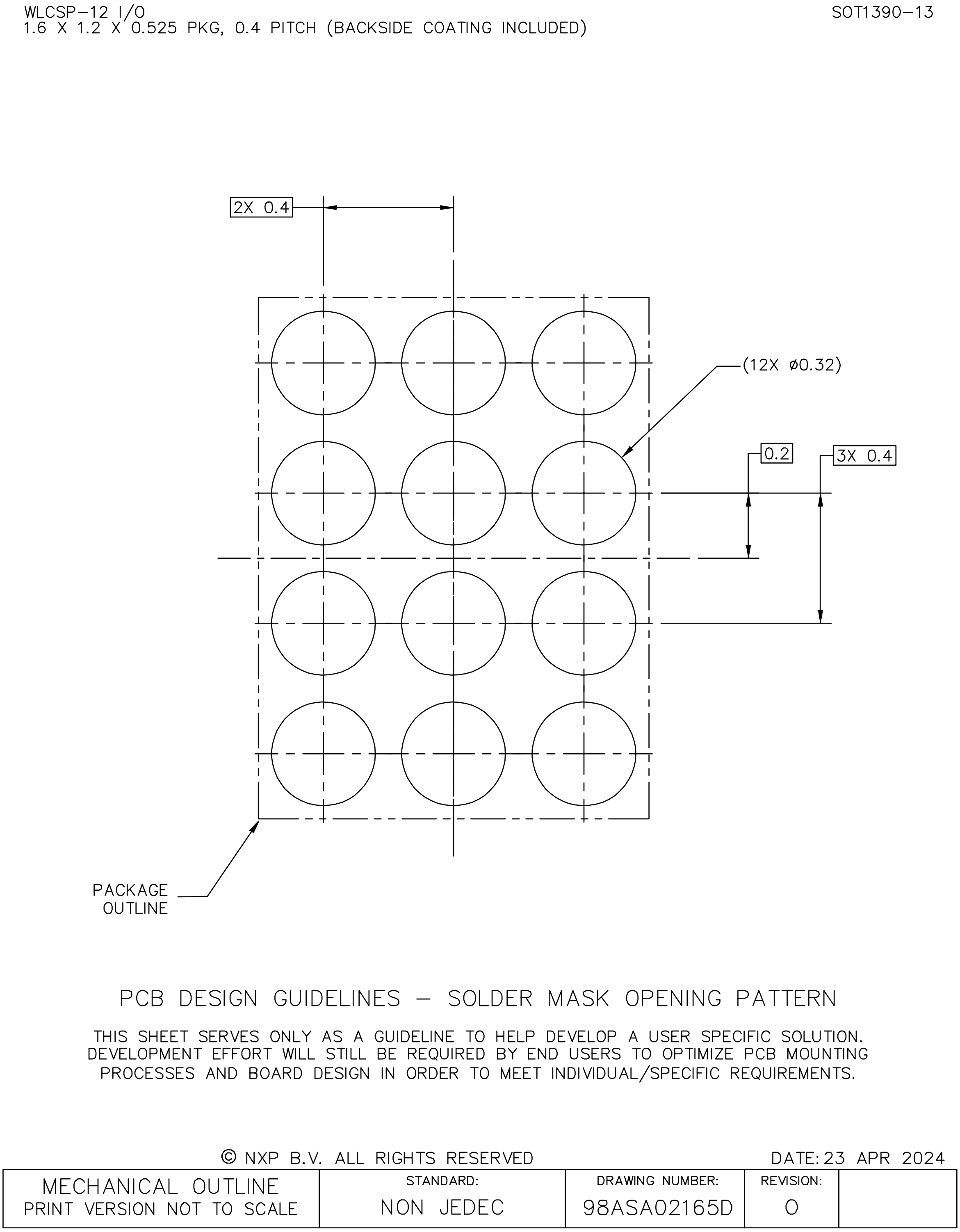
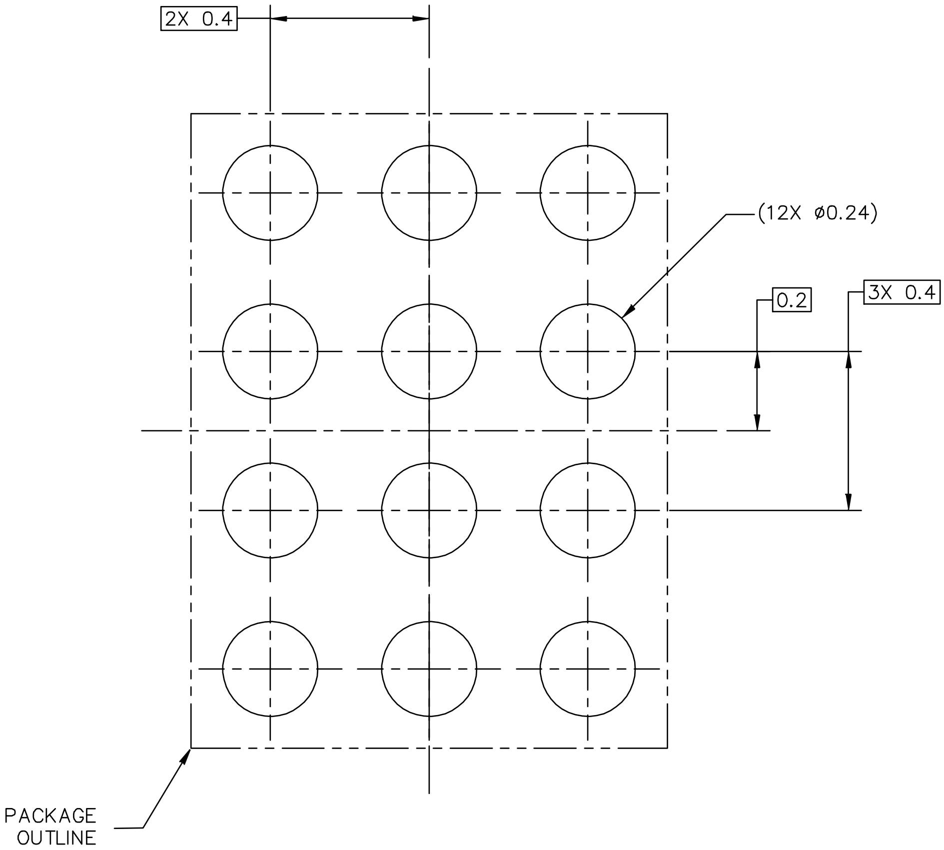


Figure 30. Reflow soldering footprint part1 for WLCSP12

WLCSP-12 I/O
1.6 X 1.2 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1390-13



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 23 APR 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02165D	REVISION: O	

Figure 31. Reflow soldering footprint part2 for WLCSP12

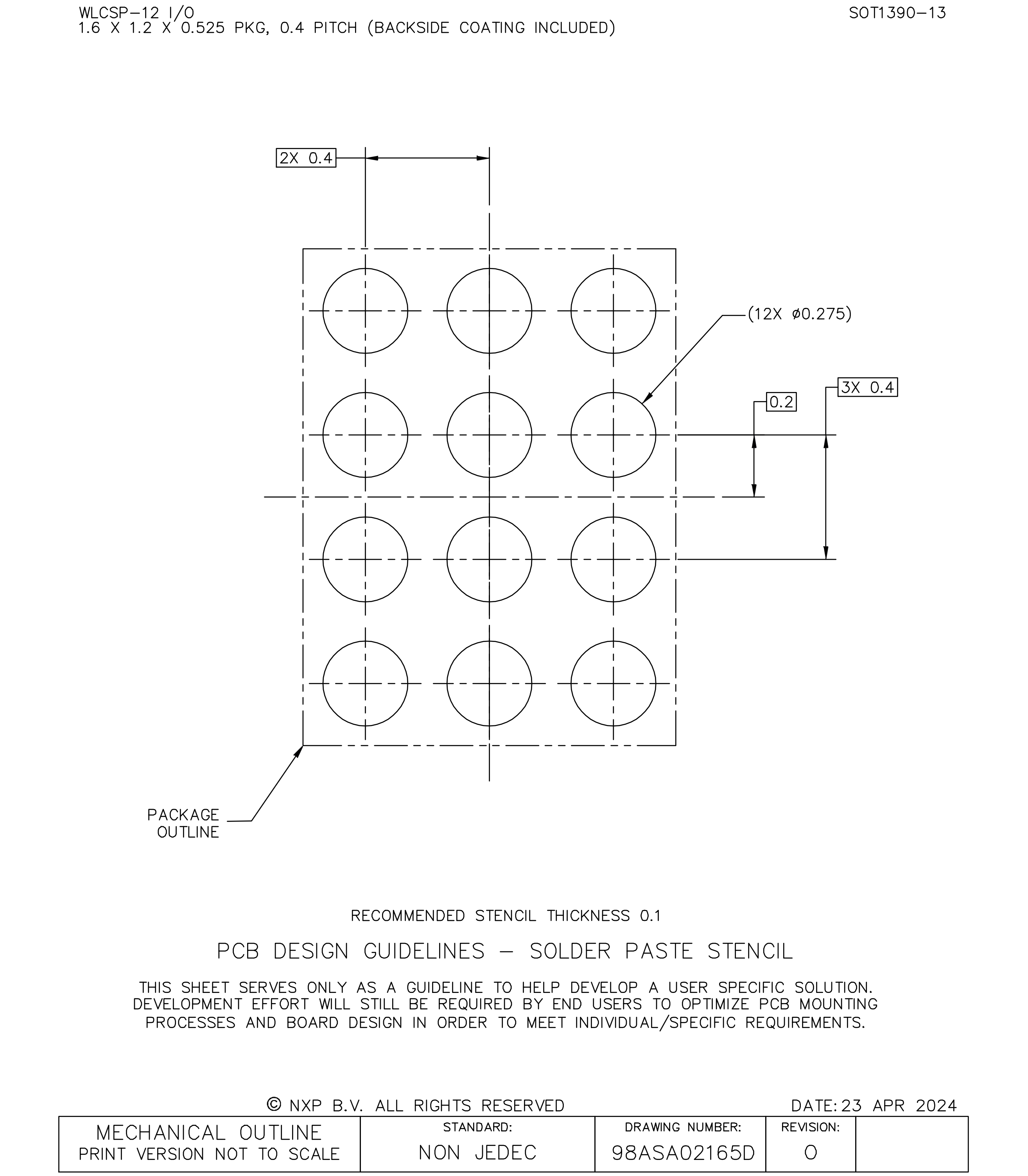


Figure 32. Reflow soldering footprint part3 for WLCSP12

WLCSP-12 I/O
1.6 X 1.2 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1390-13

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

DATE: 23 APR 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02165D	REVISION: O	

Figure 33. Package outline note WLCSP12 (SOT1390-13)

14.1.1 Package thermal characteristics

Table 98 describes the package thermal characteristics.

Table 98. Thermal characteristics

Heat dissipation on die: Uniform die power.

Rating	Board Type[1]	Symbol	Value	Unit
Junction to ambient thermal resistance [2]	JESD51-9, 2s2p	RθJA	113.4	°C/W
Junction-to-top of package thermal characterization parameter [2]	JESD51-9, 2s2p	ΨJT	1	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-9).

[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

15 Acronyms

Table 99 describes the acronyms used in this data sheet.

Table 99. Acronyms

Acronym	Description
ACK	Acknowledge
AF	Alarm Flag
BCD	Binary Coded Decimal
CDM	Charged Device Model
CL	Load Capacitance
CMOS	Complementary Metal-Oxide Semiconductor
COF	Clock Output Frequency
CTS	Clear Timestamp
DAT	Data
ESR	Equivalent Series Resistance
I2C	Inter-Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
OSF	Oscillator Stop Flag
OSFE	Oscillator Stop Flag Enable
OTP	One Time Programmable
POR	Power-On Reset
PCB	Printed Circuit Board
RTC	Real Time Clock
SCL	Serial Clock Line
SDA	Serial Data Line
SI	Second Interrupt
SIB	Serial Interface Block
SMBus	System Management Bus
SMD	Surface-Mount Device
SR	Software Reset
STA	Start Condition
VBAT	Battery Voltage
VLF	Voltage Low Flag

16 Revision history

Table 100 summarizes revisions to this document.

Table 100. Revision history

Document ID	Release date	Description
PCF8525UK v.2.0	03 June 2026	Updated the following as per CIN# 202606011I: • PCF8525 into PCF8525UK • Section 2 "Features and benefits" • Table 1 "Ordering information" • Table 2 "Ordering options" • Section 6.1 "Pinning" • Table 3 "Pin description" • Table 59 "Flag location in register Control_2" • Table 60 "Example values in register Control_2" • Table 61 "Example to clear only AF (bit 4)" • Table 62 "Example to clear only MSF (bit 7)" • Table 95 "Static characteristics" • Deleted section: HVSON10 SOT650-3(DD) • Added: Section 14.1 "Package outline: WLCSP12 SOT1390-13" • Table 98 "Thermal characteristics" • Minor editorial changes
PCF8525 v.1.0	20 January 2026	Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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