



PREFACE

**Section 1
OVERVIEW**

1.1	Introduction	1-1
1.2	Block Diagram	1-2
1.2.1	Detailed Feature List	1-2
1.2.1.1	MPC565 / MPC566 Optional Features	1-6
1.2.1.2	Supporting Documentation List	1-6
1.2.2	Module or Mode Descriptions	1-7
1.2.2.1	Comparison of MPC565 / MPC566 and MPC555 / MPC556	1-7
1.2.2.2	Additional MPC565 / MPC566 Differences	1-7
1.2.2.3	SRAM Keep-Alive Power Behavior	1-9
1.3	MPC565 / MPC566 Address Map	1-9

**Section 2
SIGNAL DESCRIPTIONS**

2.1	Pad Function Description	2-1
2.1.1	MPC565 / MPC566 Pin Sharing	2-3
2.2	Pad Module Configuration Register (PDMCR)	2-3
2.3	Pad Module Configuration Register (PDMCR2)	2-5
2.4	Signal Descriptions	2-6
2.4.1	USIU Pads	2-6
2.4.1.1	ADDR[8:31]/SGPIOA[8:31]	2-6
2.4.1.2	DATA[0:31]/SGPIOD[0:31]	2-6
2.4.1.3	$\overline{\text{IRQ}}[0]/\text{SGPIOC}[0]$	2-6
2.4.1.4	$\overline{\text{IRQ}}[1]/\text{RSV}/\text{SGPIOC}[1]$	2-6
2.4.1.5	$\overline{\text{IRQ}}[2]/\text{CR}/\text{SGPIOC}[2]/\text{MTS}$	2-7
2.4.1.6	$\overline{\text{IRQ}}[3]/\text{KR}/\text{RETRY}/\text{SGPIOC}[3]$	2-7
2.4.1.7	$\overline{\text{IRQ}}[4]/\text{AT}[2]/\text{SGPIOC}[4]$	2-7
2.4.1.8	$\overline{\text{IRQ}}[5]/\text{SGPIOC}[5]/\text{MODCK}[1]$	2-8
2.4.1.9	$\overline{\text{IRQ}}[6:7]/\text{MODCK}[2:3]$	2-8
2.4.1.10	TSIZ[0:1]	2-8
2.4.1.11	RD/WR	2-8
2.4.1.12	$\overline{\text{BURST}}$	2-8
2.4.1.13	$\overline{\text{BDIP}}$	2-9
2.4.1.14	$\overline{\text{TS}}$	2-9
2.4.1.15	$\overline{\text{TA}}$	2-9
2.4.1.16	$\overline{\text{TEA}}$	2-9
2.4.1.17	$\overline{\text{RSTCONF}}/\text{TEXP}$	2-9
2.4.1.18	$\overline{\text{OE}}$	2-10

Paragraph Number

Page Number



2.4.1.19	$\overline{BI}/\overline{STS}$	2-10
2.4.1.20	$\overline{CS}[0:3]$	2-10
2.4.1.21	$\overline{WE}[0:3]/\overline{BE}[0:3]/\overline{AT}[0:3]$	2-10
2.4.1.22	$\overline{PORESET}/\overline{TRST}$	2-10
2.4.1.23	\overline{HRESET}	2-11
2.4.1.24	\overline{SRESET}	2-11
2.4.1.25	$\overline{SGPIOC}[6]/\overline{FRZ}/\overline{PTR}$	2-11
2.4.1.26	$\overline{SGPIOC}[7]/\overline{IRQOUT}/\overline{LWP}[0]$	2-11
2.4.1.27	$\overline{BG}/\overline{VF}[0]/\overline{LWP}[1]$	2-12
2.4.1.28	$\overline{BR}/\overline{VF}[1]/\overline{IWP}[2]$	2-12
2.4.1.29	$\overline{BB}/\overline{VF}[2]/\overline{IWP}[3]$	2-12
2.4.1.30	$\overline{IWP}[0:1]/\overline{VFLS}[0:1]$	2-12
2.4.1.31	\overline{TMS}	2-13
2.4.1.32	$\overline{TDI}/\overline{DSDI}$	2-13
2.4.1.33	$\overline{TCK}/\overline{DSCK}$	2-13
2.4.1.34	$\overline{TDO}/\overline{DSDO}$	2-13
2.4.1.35	\overline{JCOMP}	2-13
2.4.1.36	\overline{XTAL}	2-14
2.4.1.37	\overline{EXTAL}	2-14
2.4.1.38	\overline{XFC}	2-14
2.4.1.39	\overline{CLKOUT}	2-14
2.4.1.40	\overline{EXTCLK}	2-14
2.4.1.41	\overline{VDDSYN}	2-14
2.4.1.42	\overline{VSSSYN}	2-14
2.4.1.43	$\overline{ENGCLK}/\overline{BUCLK}$	2-14
2.4.1.44	$\overline{PULLSEL}$	2-15
2.4.2	$\overline{QSMCM_A}/\overline{QSMCM_B}/\overline{DLCMD2}$ (J1850) PADS	2-15
2.4.2.1	$\overline{PCS}[0]/\overline{SS}/\overline{QGPIO}[0]$	2-15
2.4.2.2	$\overline{PCS}[1:2]/\overline{QGPIO}[1:2]$	2-16
2.4.2.3	$\overline{PCS}[3]/\overline{QGPIO}[3]/\overline{J1850_TX}$	2-16
2.4.2.4	$\overline{MISO}/\overline{QGPIO}[4]$	2-16
2.4.2.5	$\overline{MOSI}/\overline{QGPIO}[5]$	2-16
2.4.2.6	$\overline{SCK}/\overline{QGPIO}[6]$	2-16
2.4.2.7	$\overline{TXD}[1:2]/\overline{QGPIO}[1:2]$	2-17
2.4.2.8	$\overline{RXD}[1:2]/\overline{QGPI}[1:2]$, $\overline{RXD}[1]/\overline{QGPI1}$, $\overline{RXD}[2]/\overline{J1850_RX}$	2-17
2.4.2.9	\overline{ECK}	2-17
2.4.3	$\overline{MIOS14}$ Pads	2-17
2.4.3.1	$\overline{MDA}[11, 13, 27, 30]$	2-17
2.4.3.2	$\overline{MDA}[12, 14, 28, 31]$	2-18
2.4.3.3	$\overline{MDA}[15], [27:31]$	2-18
2.4.3.4	$\overline{MPWM}[0:3]$	2-18
2.4.3.5	$\overline{MPWM}[16, 18]$	2-18
2.4.3.6	$\overline{MPWM}[17, 19]$	2-18

Paragraph Number

Page Number



2.4.3.7	VF[0:2]/MPIO32B[0:2]	2-19
2.4.3.8	VFLS[0:1]/MPIO32B[3:4]	2-19
2.4.3.9	MPWM[4:5]/MPIO32B[5:6]	2-19
2.4.3.10	MDO[7:4]/MPIO32B[7:10]	2-19
2.4.3.11	MPWM[20:21]/MPIO32B[11:12]	2-19
2.4.3.12	C_CNTX0/C_CNRX0/MPIO32B[13:14]	2-20
2.4.3.13	MPIO32B15	2-20
2.4.4	32-KHz Oscillator Pads	2-20
2.4.4.1	XTAL32	2-20
2.4.4.2	EXTAL32	2-20
2.4.4.3	VDDRTC	2-20
2.4.4.4	VSSRTC	2-20
2.4.5	TPU3_A/TPU3_B/TPU3_C Pads	2-20
2.4.5.1	TPUCH[0:15]	2-20
2.4.5.2	T2CLK	2-21
2.4.6	QADC64_A/QADC64_B Pads	2-21
2.4.6.1	ETRIG[1:2]	2-21
2.4.6.2	AN[44]/ANw/PQB[0]	2-21
2.4.6.3	AN[45]/ANx/PQB[1]	2-21
2.4.6.4	AN[46]/ANY/PQB[2]	2-21
2.4.6.5	AN[47]/ANz/PQB[3]	2-22
2.4.6.6	AN[48:51]/PQB[4:7]	2-22
2.4.6.7	AN[52:54]/MA[0:2]/PQA[0:2]	2-22
2.4.6.8	AN[55:59]/PQA[3:7]	2-22
2.4.6.9	AN[64:71]/PQB[0:7]	2-22
2.4.6.10	AN[72:74]/MA[0:2]/PQA[0:2]	2-23
2.4.6.11	AN[75:79]/PQA[3:7]	2-23
2.4.6.12	AN[80:87]	2-23
2.4.6.13	VRH	2-23
2.4.6.14	VRL	2-23
2.4.6.15	ALTREF	2-23
2.4.6.16	VDDA	2-24
2.4.6.17	VSSA	2-24
2.4.7	TOUCAN_A / TOUCAN_B / TOUCAN_C Pads	2-24
2.4.7.1	CNTX0	2-24
2.4.7.2	CNRX0	2-24
2.4.8	READI Pads	2-24
2.4.8.1	$\overline{\text{MSE0}}$	2-24
2.4.8.2	MDO[0:3]	2-24
2.4.8.3	MCKO	2-25
2.4.8.4	$\overline{\text{RSTI}}$	2-25
2.4.8.5	$\overline{\text{EVTI}}$	2-25
2.4.8.6	$\overline{\text{MSEI}}$	2-25



2.4.8.7	MDI[0:1]	2-25
2.4.8.8	MCKI	2-25
2.4.9	UC3F Pads	2-25
2.4.9.1	EPEE	2-25
2.4.9.2	B0EPEE	2-26
2.4.9.3	VFLASH	2-26
2.4.9.4	VDDF	2-26
2.4.9.5	VSSF	2-26
2.4.10	Global Power Supplies	2-26
2.4.10.1	NVDDL	2-26
2.4.10.2	QVDDL	2-26
2.4.10.3	VDDH	2-27
2.4.10.4	VDD	2-27
2.4.10.5	KAPWR	2-27
2.4.10.6	VDDSRAM1	2-27
2.4.10.7	VDDSRAM2	2-27
2.4.10.8	VDDSRAM3	2-27
2.4.10.9	VSS	2-27
2.5	Reset State	2-27
2.5.1	Pin Functionality Configuration Out of Reset	2-28
2.5.2	Pin State During Reset	2-28
2.5.3	Power-On Reset and Hard Reset	2-28
2.5.4	Pin Reset States	2-29
2.6	Pad Types	2-36
2.7	Electrical Characteristics	2-39
2.7.1	Target DC Characteristics	2-39
2.7.2	Pad Measurement Criteria	2-39
2.7.2.1	Input Buffer	2-40
2.7.2.2	Output Driver	2-41
2.8	Package Description	2-53
2.8.1	Package Diagrams	2-53
2.8.2	Bumped Die	2-56
2.8.3	MPC565 / MPC566 Ball Diagram	2-57

Section 3 CENTRAL PROCESSING UNIT

3.1	RCPU Features	3-1
3.2	RCPU Block Diagram	3-2
3.3	Instruction Sequencer	3-3
3.4	Independent Execution Units	3-4
3.4.1	Branch Processing Unit (BPU)	3-5
3.4.2	Integer Unit (IU)	3-5
3.4.3	Load/Store Unit (LSU)	3-6



3.4.4 Floating-Point Unit (FPU)	3-6
3.5 Levels of the PowerPC Architecture	3-7
3.6 RCPU Programming Model	3-7
3.7 PowerPC UISA Register Set	3-11
3.7.1 General-Purpose Registers (GPRs)	3-12
3.7.2 Floating-Point Registers (FPRs)	3-12
3.7.3 Floating-Point Status and Control Register (FPSCR)	3-12
3.7.4 Condition Register (CR)	3-15
3.7.4.1 Condition Register CR0 Field Definition	3-16
3.7.4.2 Condition Register CR1 Field Definition	3-16
3.7.4.3 Condition Register CR n Field — Compare Instruction	3-17
3.7.5 Integer Exception Register (XER)	3-17
3.7.6 Link Register (LR)	3-18
3.7.7 Count Register (CTR)	3-19
3.8 PowerPC VEA Register Set — Time Base	3-19
3.9 PowerPC OEA Register Set	3-20
3.9.1 Machine State Register (MSR)	3-20
3.9.2 DAE/Source Instruction Service Register (DSISR)	3-22
3.9.3 Data Address Register (DAR)	3-22
3.9.4 Time Base Facility (TB) — OEA	3-23
3.9.5 Decrementer Register (DEC)	3-23
3.9.6 Machine Status Save/Restore Register 0 (SRR0)	3-24
3.9.7 Machine Status Save/Restore Register 1 (SRR1)	3-24
3.9.8 General SPRs (SPRG0–SPRG3)	3-25
3.9.9 Processor Version Register (PVR)	3-25
3.9.10 Implementation-Specific SPRs	3-26
3.9.10.1 EIE, EID, and NRI Special-Purpose Registers	3-26
3.9.10.2 Floating-Point Exception Cause Register (FPECR)	3-26
3.9.10.3 Additional Implementation-Specific Registers	3-27
3.10 Instruction Set	3-28
3.10.1 Instruction Set Summary	3-29
3.10.2 Recommended Simplified Mnemonics	3-33
3.10.3 Calculating Effective Addresses	3-33
3.11 Exception Model	3-34
3.11.1 Exception Classes	3-34
3.11.2 Ordered Exceptions	3-34
3.11.3 Unordered Exceptions	3-35
3.11.4 Precise Exceptions	3-35
3.11.5 Exception Vector Table	3-35
3.12 Instruction Timing	3-36
3.13 PowerPC User Instruction Set Architecture (UISA)	3-38
3.13.1 Computation Modes	3-38
3.13.2 Reserved Fields	3-38

Paragraph Number

Page Number



3.13.3	Classes of Instructions	3-39
3.13.4	Exceptions	3-39
3.13.5	The Branch Processor	3-39
3.13.6	Instruction Fetching	3-39
3.13.7	Branch Instructions.	3-39
3.13.7.1	Invalid Branch Instruction Forms	3-39
3.13.7.2	Branch Prediction	3-39
3.13.8	The Fixed-Point Processor.	3-40
3.13.8.1	Fixed-Point Instructions	3-40
3.13.9	Floating-Point Processor	3-40
3.13.9.1	General.	3-40
3.13.9.2	Optional instructions.	3-41
3.13.10	Load/Store Processor.	3-41
3.13.10.1	Fixed-Point Load With Update and Store With Update Instructions.	3-41
3.13.10.2	Fixed-Point Load and Store Multiple Instructions.	3-41
3.13.10.3	Fixed-Point Load String Instructions.	3-41
3.13.10.4	Storage Synchronization Instructions.	3-41
3.13.10.5	Floating-Point Load and Store With Update Instructions	3-41
3.13.10.6	Floating-Point Load Single Instructions	3-41
3.13.10.7	Floating-Point Store Single Instructions	3-42
3.13.10.8	Optional Instructions.	3-42
3.13.10.9	Little-Endian Byte Ordering	3-42
3.14	PowerPC Virtual Environment Architecture (VEA).	3-42
3.14.1	Atomic Update Primitives	3-42
3.14.2	Effect of Operand Placement on Performance	3-42
3.14.3	Storage Control Instructions	3-43
3.14.4	Instruction Synchronize (isync) Instruction	3-43
3.14.4.1	Enforce In-Order Execution of I/O (eieio) Instruction	3-43
3.14.5	Timebase	3-43
3.15	PowerPC Operating Environment Architecture (OEA).	3-43
3.15.1	Branch Processor Registers.	3-43
3.15.1.1	Machine State Register (MSR).	3-43
3.15.1.2	Branch Processors Instructions	3-44
3.15.2	Fixed-Point Processor	3-44
3.15.2.1	Special Purpose Registers	3-44
3.15.3	Storage Control Instructions	3-44
3.15.4	Interrupts	3-44
3.15.4.1	System Reset Interrupt.	3-44
3.15.4.2	Machine Check Interrupt	3-45
3.15.4.3	Data Storage Interrupt	3-46
3.15.4.4	Instruction Storage Interrupt.	3-46
3.15.4.5	Alignment Interrupt.	3-46
3.15.4.6	Floating-Point Enabled Exception Type Program Interrupt	3-47



3.15.4.7	Illegal Instruction Type Program Interrupt	3-47
3.15.4.8	Privileged Instruction Type Program interrupt	3-47
3.15.4.9	Floating-Point Unavailable Interrupt.	3-47
3.15.4.10	Trace Interrupt	3-47
3.15.4.11	Floating-Point Assist Interrupt	3-48
3.15.4.12	Implementation-Dependent Software Emulation Interrupt	3-49
3.15.4.13	Implementation-Specific Instruction Storage Protection Error Interrupt	3-50
3.15.4.14	Implementation-Specific Data Storage Protection Error Interrupt	3-51
3.15.4.15	Implementation-Specific Debug Interrupts	3-52
3.15.4.16	Partially Executed Instructions	3-53
3.15.5	Timer Facilities	3-54
3.15.6	Optional Facilities and Instructions.	3-54

Section 4

BURST BUFFER CONTROLLER MODULE

4.1	Overview and General Description	4-1
4.2	Feature List	4-2
4.2.1	BIU Key Features	4-2
4.2.2	IMPU Key Features	4-3
4.2.3	ICDU Key Features	4-3
4.2.3.1	DECRAM Key Features	4-4
4.3	Class Based Compression Model Main Principles.	4-4
4.3.1	Compression Model Features	4-4
4.3.2	Model Limitations	4-5
4.3.3	Instruction Classes Based Compression Algorithm	4-5
4.3.4	Compression Process	4-7
4.3.5	Decompression.	4-8
4.3.6	Compression Environment Initialization	4-9
4.4	Operation Modes	4-9
4.4.1	Instruction Fetch.	4-9
4.4.1.1	“Decompression OFF” Mode	4-10
4.4.1.2	“Decompression ON” Mode	4-10
4.4.1.3	Show Cycles in “Decompression ON” Mode	4-10
4.4.2	Burst Operation of the BBC	4-11
4.4.3	Access Violation Detection	4-11
4.4.4	Slave Operation	4-12
4.4.5	Reset Behavior	4-12
4.4.6	Debug Operation Mode	4-13
4.5	Exception Table Relocation (ETR).	4-13
4.5.1	ETR Overview	4-13
4.5.2	ETR Operation	4-14
4.5.3	Enhanced External Interrupt Relocation (EEIR).	4-17
4.6	Decompressor RAM (DECRAM) Functionality.	4-18

Paragraph Number

Page Number



4.6.1	Vocabulary Table Storage Operation	4-19
4.6.2	General Purpose Memory Operation	4-19
4.6.2.1	Memory Protection Violations.	4-20
4.6.2.2	DECRAM StandBy Operation Mode.	4-20
4.7	Branch Target Buffer	4-21
4.7.1	BTB Operation	4-21
4.7.1.1	BTB Invalidation	4-22
4.7.1.2	BTB Enabling/Disabling	4-23
4.7.1.3	BTB Inhibit Regions	4-23
4.8	BBC Programming Model	4-23
4.8.1	Address Map	4-23
4.8.1.1	BBC Special Purpose Registers (SPRs)	4-24
4.8.1.2	DECRAM and DCCR Block	4-24
4.8.2	BBC Registers Description	4-25
4.8.2.1	BBC Module Configuration Register BBCMCR	4-25
4.8.2.2	Region Base Address Registers MI_RBA0-3.	4-27
4.8.2.3	Region Attribute Registers MI_RA[1:3].	4-27
4.8.2.4	Global Region Attribute Register MI_GRA	4-29
4.8.2.5	External Interrupt Relocation Table Base Address Register — EIBADR	4-31
4.8.2.6	Decompressor Class Configuration Registers (DCCR1-15).	4-31
4.8.2.7	Decompressor Class Configuration Registers (DCCR1-DCCR15)	4-32

Section 5

UNIFIED SYSTEM INTERFACE UNIT (USIU)

5.1	USIU Introduction.	5-1
5.2	USIU Module Overview	5-1
5.2.1	USIU Address Map.	5-3
5.2.2	USIU Special Purpose Registers	5-7

Section 6

SYSTEM CONFIGURATION AND PROTECTION

6.1	System Configuration.	6-3
6.1.1	USIU Pins Multiplexing	6-4
6.1.2	Memory Mapping	6-4
6.1.3	Arbitration Support	6-5
6.2	External Master Modes	6-5
6.2.1	Operation in External Master Modes	6-6
6.2.2	Address Decoding for External Accesses	6-7
6.3	USIU General-Purpose I/O	6-7
6.4	Enhanced Interrupt Controller	6-9
6.4.1	Key Features	6-9
6.4.2	Interrupt Configuration	6-9
6.4.3	Regular Interrupt Controller Operation (MPC555/MPC556 Compatible Mode)	6-11
6.4.4	Enhanced Interrupt Controller	6-12

Paragraph Number

Page Number



6.4.4.1	General Operation	6-12
6.4.4.2	Lower Priority Request Masking	6-14
6.4.4.3	Backward Compatibility with MPC555/MPC556.	6-15
6.5	Interrupt Overhead Estimation for Enhanced Interrupt Controller Mode	6-17
6.6	Hardware Bus Monitor	6-18
6.7	MPC565 / MPC566 Decrementer	6-19
6.8	MPC565 / MPC566 Time Base (TB)	6-20
6.9	Real-Time Clock (RTC)	6-21
6.10	Periodic Interrupt Timer (PIT).	6-21
6.11	Software Watchdog Timer (SWT)	6-22
6.12	Freeze Operation	6-24
6.13	Low Power Stop Operation	6-24
6.14	System Configuration and Protection Registers	6-24
6.14.1	System Configuration Registers	6-25
6.14.1.1	SIU Module Configuration Register (SIUMCR)	6-25
6.14.1.2	Internal Memory Map Register	6-28
6.14.1.3	External Master Control Register (EMCR)	6-29
6.14.2	SIU Interrupt Controller Registers	6-30
6.14.2.1	SIU Interrupt Pending Register.	6-31
6.14.2.2	SIU Interrupt Pending Register 2	6-31
6.14.2.3	SIU Interrupt Pending Register 3	6-32
6.14.2.4	SIU Interrupt Mask Register	6-32
6.14.2.5	SIU Interrupt Mask Register 2	6-33
6.14.2.6	SIU Interrupt Mask Register 3	6-33
6.14.2.7	SIU Interrupt Edge Level Register (SIEL).	6-33
6.14.2.8	SIU Interrupt Vector Register	6-34
6.14.2.9	Interrupt In-Service Registers.	6-35
6.14.3	System Protection Registers	6-36
6.14.3.1	System Protection Control Register (SYPCR)	6-36
6.14.3.2	Software Service Register (SWSR)	6-37
6.14.3.3	Transfer Error Status Register (TESR).	6-38
6.14.4	System Timer Registers	6-39
6.14.4.1	Decrementer Register	6-39
6.14.4.2	Time Base SPRs	6-39
6.14.4.3	Time Base Reference Registers.	6-40
6.14.4.4	Time Base Control and Status Register.	6-40
6.14.4.5	Real-Time Clock Status and Control Register	6-41
6.14.4.6	Real-Time Clock Register (RTC)	6-42
6.14.4.7	Real-Time Clock Alarm Register (RTCAL).	6-42
6.14.4.8	Periodic Interrupt Status and Control Register (PISCR).	6-43
6.14.4.9	Periodic Interrupt Timer Count Register (PITC)	6-43
6.14.4.10	Periodic Interrupt Timer Register (PITR)	6-44
6.14.5	General-Purpose I/O Registers	6-45



6.14.5.1 SGPIO Data Register 1 (SGPIODT1).....	6-45
6.14.5.2 SGPIO Data Register 2 (SGPIODT2).....	6-45
6.14.5.3 SGPIO Control Register (SGPIOCR).....	6-46

Section 7 RESET

7.1 Reset Operation.....	7-1
7.1.1 Power-On Reset.....	7-1
7.1.2 Hard Reset.....	7-2
7.1.3 Soft Reset.....	7-2
7.1.4 Loss of Lock.....	7-3
7.1.5 On-Chip Clock Switch.....	7-3
7.1.6 Software Watchdog Reset.....	7-3
7.1.7 Checkstop Reset.....	7-3
7.1.8 Debug Port Hard Reset.....	7-3
7.1.9 Debug Port Soft Reset.....	7-3
7.1.10 JTAG Reset.....	7-3
7.2 Reset Actions Summary.....	7-4
7.3 Data Coherency During Reset.....	7-4
7.4 Reset Status Register.....	7-5
7.5 Reset Configuration.....	7-6
7.5.1 Hard Reset Configuration.....	7-6
7.5.2 Hard Reset Configuration Word.....	7-11
7.5.3 Soft Reset Configuration.....	7-13

Section 8 CLOCKS AND POWER CONTROL

8.1 Overview.....	8-1
8.2 System Clock Sources.....	8-3
8.3 System PLL.....	8-3
8.3.1 Frequency Multiplication.....	8-4
8.3.2 Skew Elimination.....	8-4
8.3.3 Pre-Divider.....	8-4
8.3.4 PLL Block Diagram.....	8-4
8.3.5 PLL Pins.....	8-5
8.4 System Clock During PLL Loss of Lock.....	8-6
8.5 Low-Power Divider.....	8-6
8.6 MPC565 / MPC566 Internal Clock Signals.....	8-7
8.6.1 General System Clocks.....	8-9
8.6.2 Clock Out (CLKOUT).....	8-12
8.6.3 Engineering Clock (ENGCLK).....	8-12
8.7 Clock Source Switching.....	8-13
8.8 Low-Power Modes.....	8-15
8.8.1 Entering a Low-Power Mode.....	8-15

Paragraph Number

Page Number



8.8.2	Power Mode Descriptions	8-16
8.8.3	Exiting from Low-Power Modes	8-16
8.8.3.1	Exiting from Normal-Low Mode	8-17
8.8.3.2	Exiting From Doze Mode	8-17
8.8.3.3	Exiting From Deep-Sleep Mode	8-18
8.8.3.4	Exiting from Power-Down Mode	8-18
8.8.3.5	Low-Power Modes Flow	8-18
8.9	Basic Power Structure	8-20
8.9.1	General Power Supply Definitions	8-20
8.9.2	Chip Power Structure	8-21
8.9.2.1	NVDDL	8-21
8.9.2.2	QVDDL	8-21
8.9.2.3	VDD	8-21
8.9.2.4	VDDSYN, VSSSYN	8-21
8.9.2.5	KAPWR	8-21
8.9.2.6	VDDA, VSSA	8-22
8.9.2.7	VFLASH	8-22
8.9.2.8	VDDF, VSSF	8-22
8.9.2.9	VDDH	8-22
8.9.2.10	VDDSRAM1	8-22
8.9.2.11	VDDSRAM2	8-22
8.9.2.12	VDDSRAM3	8-22
8.9.2.13	VDDRTC	8-22
8.9.2.14	VSS	8-22
8.9.3	Keep Alive Power	8-23
8.9.3.1	Keep Alive Power Configuration	8-23
8.9.3.2	Keep-Alive Power Registers Lock Mechanism	8-24
8.10	VDDSRAM Supply Failure Detection	8-26
8.11	Power-Up/Down Sequencing	8-26
8.12	Clocks Unit Programming Model	8-29
8.12.1	System Clock Control Register (SCCR)	8-29
8.12.2	PLL, Low-Power, and Reset-Control Register (PLPRCR)	8-33
8.12.3	Change of Lock Interrupt Register (COLIR)	8-36
8.12.4	VDDSRAM Control Register (VSRMCR)	8-36

Section 9 EXTERNAL BUS INTERFACE

9.1	Features	9-1
9.2	Bus Transfer Signals	9-1
9.3	Bus Control Signals	9-2
9.4	Bus Interface Signal Descriptions	9-3
9.5	Bus Operations	9-7
9.5.1	Basic Transfer Protocol	9-8

Paragraph Number

Page Number



9.5.2 Single Beat Transfer	9-8
9.5.2.1 Single Beat Read Flow	9-8
9.5.2.2 Single Beat Write Flow	9-11
9.5.2.3 Single Beat Flow with Small Port Size	9-14
9.5.3 Burst Transfer	9-15
9.5.4 Burst Mechanism	9-16
9.5.5 Alignment and Packaging of Transfers	9-28
9.5.6 Arbitration Phase	9-30
9.5.6.1 Bus Request	9-31
9.5.6.2 Bus Grant	9-32
9.5.6.3 Bus Busy	9-32
9.5.6.4 Internal Bus Arbiter	9-33
9.5.7 Address Transfer Phase Signals	9-35
9.5.7.1 Transfer Start	9-36
9.5.7.2 Address Bus	9-36
9.5.7.3 Read/Write	9-36
9.5.7.4 Burst Indicator	9-36
9.5.7.5 Transfer Size	9-37
9.5.7.6 Address Types	9-37
9.5.7.7 Burst Data in Progress	9-39
9.5.8 Termination Signals	9-39
9.5.8.1 Transfer Acknowledge	9-39
9.5.8.2 Burst Inhibit	9-39
9.5.8.3 Transfer Error Acknowledge	9-39
9.5.8.4 Termination Signals Protocol	9-39
9.5.9 Storage Reservation	9-41
9.5.10 Bus Exception Control Cycles	9-44
9.5.10.1 Retrying a Bus Cycle	9-44
9.5.10.2 Termination Signals Protocol Summary	9-48
9.5.11 Bus Operation in External Master Modes	9-48
9.5.12 Contention Resolution on External Bus	9-53
9.5.13 Show Cycle Transactions	9-55

Section 10 MEMORY CONTROLLER

10.1 Overview	10-1
10.2 Memory Controller Architecture	10-3
10.2.1 Associated Registers	10-4
10.2.2 Port Size Configuration	10-5
10.2.3 Write-Protect Configuration	10-5
10.2.4 Address and Address Space Checking	10-5
10.2.5 Burst Support	10-5
10.3 Chip-Select Timing	10-6



10.3.1	Memory Devices Interface Example	10-7
10.3.2	Peripheral Devices Interface Example	10-9
10.3.3	Relaxed Timing Examples	10-11
10.3.4	Extended Hold Time on Read Accesses	10-15
10.3.5	Summary of GPCM Timing Options	10-19
10.4	Global (Boot) Chip-Select Operation	10-21
10.5	Write and Byte Enable Signals.	10-22
10.6	Dual Mapping of the Internal Flash EEPROM Array	10-23
10.7	Memory Controller External Master Support	10-25
10.8	Programming Model.	10-28
10.8.1	General Memory Controller Programming Notes	10-28
10.8.2	Memory Controller Status Registers (MSTAT)	10-29
10.8.3	Memory Controller Base Registers (BR[0] – BR[3])	10-29
10.8.4	Memory Controller Option Registers (OR[0]– OR[3])	10-31
10.8.5	Dual-Mapping Base Register (DMBR)	10-33
10.8.6	Dual-Mapping Option Register	10-34

Section 11 L-BUS TO U-BUS INTERFACE (L2U)

11.1	General Features	11-1
11.2	DMPU Features	11-1
11.3	L2U Block Diagram	11-2
11.4	Modes Of Operation.	11-2
11.4.1	Normal Mode	11-3
11.4.2	Reset Operation	11-3
11.4.3	Factory Test Mode	11-3
11.4.4	Peripheral Mode	11-4
11.5	Data Memory Protection	11-4
11.5.1	Functional Description	11-4
11.5.2	Associated Registers	11-5
11.5.3	L-bus Memory Access Violations	11-7
11.6	Reservation Support	11-7
11.6.1	The Reservation Protocol	11-7
11.6.2	L2U Reservation Support	11-8
11.6.3	Reserved Location (Bus) and Possible Actions	11-9
11.7	L-Bus Show Cycle Support	11-9
11.7.1	Programming Show Cycles	11-9
11.7.2	Performance Impact	11-10
11.7.3	Show Cycle Protocol	11-10
11.7.4	L-Bus Write Show Cycle Flow	11-10
11.7.5	L-Bus Read Show Cycle Flow	11-11
11.7.6	Show Cycle Support Guidelines	11-11
11.8	L2U Programming Model	11-12



11.8.1	U-bus Access	11-13
11.8.2	Transaction Size	11-13
11.8.3	L2U Module Configuration Register (L2U_MCR)	11-13
11.8.4	Region Base Address Registers (L2U_RBAX)	11-14
11.8.5	Region Attribute Registers (L2U_RAX)	11-15
11.8.6	Global Region Attribute Register	11-16

Section 12 U-BUS TO IMB3 BUS INTERFACE (UIMB)

12.1	Features	12-1
12.2	UIMB Block Diagram	12-2
12.3	Clock Module	12-2
12.4	Interrupt Operation	12-3
12.4.1	Interrupt Sources and Levels on IMB	12-4
12.4.2	IMB Interrupt Multiplexing	12-4
12.4.3	ILBS Sequencing	12-4
12.4.4	Interrupt Synchronizer	12-6
12.5	Programming Model	12-7
12.5.1	UIMB Module Configuration Register (UMCR)	12-7
12.5.2	Test control register (UTSTCREG)	12-8
12.5.3	Pending Interrupt Request Register (UIPEND)	12-8

Section 13 QUEUED ANALOG-TO-DIGITAL CONVERTER (QADC64E)

13.1	Features, Overview and Quick Reference Diagrams	13-1
13.1.1	Features of the QADC64E (Each Module)	13-1
13.1.2	QADC64E Block Diagrams	13-2
13.1.3	Memory Map	13-4
13.1.4	Using the Queue and Result Word Table	13-6
13.1.5	External Multiplexing	13-7
13.2	Programming the QADC64E Registers	13-9
13.2.1	QADC64E Module Configuration Register	13-10
13.2.1.1	Low Power Stop Mode	13-10
13.2.1.2	Freeze Mode	13-11
13.2.1.3	Supervisor/Unrestricted Address Space	13-12
13.2.1.4	Master/Slave Operation and Multi-Module Synchronous Clocks	13-13
13.2.2	QADC64E Interrupt Register	13-13
13.2.3	Port Data Register	13-15
13.2.4	Port Data Direction Register	13-15
13.2.5	Control Register 0	13-16
13.2.6	Control Register 1	13-18
13.2.7	Control Register 2	13-20

Paragraph Number

Page Number



13.2.8	Status Registers	13-23
13.2.9	Conversion Command Word Table	13-30
13.2.10	Result Word Table	13-36
13.3	Analog Subsystem	13-38
13.3.1	Analog-to-Digital Converter Operation	13-38
13.3.1.1	Conversion Cycle Times	13-39
13.3.2	Channel Decode and Multiplexer	13-40
13.3.3	Sample Buffer Amplifier	13-40
13.3.4	Digital to Analog Converter (DAC) Array	13-40
13.3.5	Comparator	13-41
13.3.6	Bias	13-41
13.3.7	Successive Approximation Register	13-41
13.3.8	State Machine	13-41
13.4	Digital Subsystem	13-41
13.4.1	Queue Priority	13-42
13.4.2	Sub-Queues That are Paused	13-42
13.4.3	Boundary Conditions	13-44
13.4.4	Scan Modes	13-45
13.4.4.1	Disabled Mode	13-45
13.4.4.2	Reserved Mode	13-46
13.4.4.3	Single-Scan Modes	13-46
13.4.4.4	Software Initiated Single-Scan Mode	13-47
13.4.4.5	External Trigger Single-Scan Mode	13-47
13.4.4.6	External Gated Single-Scan Mode	13-48
13.4.4.7	Periodic/Interval Timer Single-Scan Mode	13-48
13.4.4.8	Continuous-Scan Modes	13-49
13.4.4.9	Software Initiated Continuous-Scan Mode	13-50
13.4.4.10	External Trigger Continuous-Scan Mode	13-50
13.4.4.11	External Gated Continuous-Scan Mode	13-51
13.4.4.12	Periodic/Interval Timer Continuous-Scan Mode	13-52
13.4.5	QADC64E Clock (QCLK) Generation	13-52
13.4.6	Periodic/Interval Timer	13-54
13.4.7	Configuration And Control using the IMB Interface	13-55
13.4.7.1	QADC64E Bus Interface Unit	13-55
13.4.7.2	QADC64E Bus Accessing	13-55
13.5	Trigger and Queue Interaction Examples	13-57
13.5.1	Queue Priority Schemes	13-57
13.5.2	Conversion Timing Schemes	13-68
13.6	QADC64E Integration Requirements	13-71
13.6.1	Port Digital Input/Output Pins	13-71
13.6.2	External Trigger Input Pins	13-72
13.6.3	Analog Power Pins	13-72
13.6.3.1	Analog Supply Filtering and Grounding	13-74



13.6.4	Analog Reference Pins	13-76
13.6.5	Analog Input Pins	13-76
13.6.5.1	Analog Input Considerations	13-78
13.6.5.2	Settling Time for the External Circuit	13-80
13.6.5.3	Error Resulting from Leakage.	13-80
13.6.5.4	Accommodating Positive/Negative Stress Conditions	13-81

Section 14

QUEUED SERIAL MULTI-CHANNEL MODULE

14.1	Overview	14-1
14.2	Block Diagram	14-1
14.2.1	MPC565 / MPC566 QSMCM Details	14-2
14.3	Signal Descriptions	14-3
14.4	Memory Maps	14-3
14.5	QSMCM Global Registers	14-6
14.5.1	Low-Power Stop Operation	14-6
14.5.2	Freeze Operation	14-7
14.5.3	Access Protection.	14-7
14.5.4	QSMCM Interrupts	14-7
14.5.5	QSMCM Configuration Register (QSMCMCR)	14-9
14.5.6	QSMCM Test Register (QTEST)	14-9
14.5.7	QSMCM Interrupt Level Registers (QDSCI_IL, QSPI_IL)	14-9
14.6	QSMCM Pin Control Registers	14-10
14.6.1	Port QS Data Register (PORTQS)	14-11
14.6.2	PORTQS Pin Assignment Register (PQSPAR)	14-12
14.6.3	PORTQS Data Direction Register (DDRQS)	14-13
14.7	Queued Serial Peripheral Interface	14-14
14.7.1	QSPI Registers	14-16
14.7.1.1	QSPI Control Register 0	14-17
14.7.1.2	QSPI Control Register 1	14-19
14.7.1.3	QSPI Control Register 2	14-20
14.7.1.4	QSPI Control Register 3	14-20
14.7.1.5	QSPI Status Register	14-21
14.7.2	QSPI RAM	14-22
14.7.2.1	Receive RAM	14-23
14.7.2.2	Transmit RAM.	14-23
14.7.2.3	Command RAM	14-23
14.7.3	QSPI Pins	14-24
14.7.4	QSPI Operation	14-25
14.7.4.1	Enabling, Disabling, and Halting the SPI	14-26
14.7.4.2	QSPI Interrupts	14-27
14.7.4.3	QSPI Flow	14-27
14.7.5	Master Mode Operation	14-34

Paragraph Number

Page Number



14.7.5.1	Clock Phase and Polarity	14-35
14.7.5.2	Baud Rate Selection	14-35
14.7.5.3	Delay Before Transfer	14-36
14.7.5.4	Delay After Transfer	14-36
14.7.5.5	Transfer Length	14-37
14.7.5.6	Peripheral Chip Selects	14-37
14.7.5.7	Master Wraparound Mode	14-38
14.7.6	Slave Mode	14-38
14.7.6.1	Description of Slave Operation	14-39
14.7.7	Slave Wraparound Mode	14-41
14.7.8	Mode Fault	14-42
14.8	Serial Communication Interface	14-42
14.8.1	SCI Registers	14-45
14.8.2	SCI Control Register 0	14-46
14.8.3	SCI Control Register 1	14-46
14.8.4	SCI Status Register (SCxSR)	14-48
14.8.5	SCI Data Register (SCxDR)	14-50
14.8.6	SCI Pins	14-51
14.8.7	SCI Operation	14-51
14.8.7.1	Definition of Terms	14-51
14.8.7.2	Serial Formats	14-52
14.8.7.3	Baud Clock	14-52
14.8.7.4	Parity Checking	14-53
14.8.7.5	Transmitter Operation	14-53
14.8.7.6	Receiver Operation	14-55
14.8.7.7	Receiver Functional Operation	14-57
14.8.7.8	Idle-Line Detection	14-58
14.8.7.9	Receiver Wake-Up	14-59
14.8.7.10	Internal Loop Mode	14-59
14.9	SCI Queue Operation	14-60
14.9.1	Queue Operation of SCI1 for Transmit and Receive	14-60
14.9.2	Queued SCI1 Status and Control Registers	14-60
14.9.2.1	QSCI1 Control Register	14-60
14.9.2.2	QSCI1 Status Register	14-62
14.9.3	QSCI1 Transmitter Block Diagram	14-62
14.9.4	QSCI1 Additional Transmit Operation Features	14-63
14.9.5	QSCI1 Transmit Flow Chart Implementing the Queue	14-65
14.9.6	Example QSCI1 Transmit for 17 Data Bytes	14-67
14.9.7	Example SCI Transmit for 25 Data Bytes	14-68
14.9.8	QSCI1 Receiver Block Diagram	14-69
14.9.9	QSCI1 Additional Receive Operation Features	14-69
14.9.10	QSCI1 Receive Flow Chart Implementing The Queue	14-72
14.9.11	QSCI1 Receive Queue Software Flow Chart	14-73



14.9.12 Example QSCI1 Receive Operation of 17 Data Frames	14-74
---	-------

Section 15

DATA LINK CONTROLLER MODULE (DLCMD2)

15.1 Scope	15-1
15.2 Features	15-1
15.3 1.4 Background	15-2
15.4 1.5 Applicable Documents	15-2
15.5 1.6 General Requirements	15-2
15.6 Logic Description	15-2
15.6.1 Block Diagram	15-2
15.6.2 DLCMD2 Operation	15-3
15.6.2.1 General	15-3
15.6.2.2 Logic Section Description and Relation to Transceiver	15-4
15.6.2.3 DLCMD2 Transmit/Receive Operation	15-4
15.6.2.4 Message Transmission	15-6
15.6.2.5 Message Reception	15-6
15.6.2.6 Sleep Mode	15-7
15.6.2.7 Debug Mode	15-7
15.6.2.8 4X Speed Mode	15-7
15.6.2.9 Block Mode	15-8
15.6.2.10 Error Detection	15-8
15.6.2.11 Arbitration	15-9
15.6.2.12 Timebase Generation	15-9
15.6.2.13 Receive and Transmit Message Buffers	15-10
15.6.2.14 Bus Waveforms Generation	15-11
15.6.2.15 Huntzicker Encoding	15-11
15.6.3 TData Link Controller Module (DLCMD2)	15-13
15.7 Signals Overview	15-13
15.7.1 J1850 Bus Waveforms	15-14
15.7.1.1 Start of Frame (SOF)	15-14
15.7.1.2 Data Bits	15-14
15.7.1.3 "0" bit	15-14
15.7.1.4 "1" bit	15-15
15.7.1.5 End of Data (EOD)	15-15
15.7.1.6 Normalization Bit	15-15
15.7.1.7 End of Frame (EOF)	15-15
15.7.1.8 Break	15-16
15.7.2 General Symbol Transmission	15-16
15.7.3 General Symbol Reception	15-16
15.7.4 Support For External Transceiver	15-17
15.8 Operating Modes	15-17
15.8.1 Power Off	15-18

Paragraph Number

Page Number



15.8.2	Reset	15-18
15.8.3	Run	15-19
15.8.4	DLCMD2 STOP and LPSTOP	15-19
15.8.4.1	DLCMD2 STOP mode	15-19
15.8.4.2	DLCMD2 LPSTOP mode	15-19
15.8.5	DLCMD2 DEBUG	15-19
15.9	CPU Interface	15-22
15.9.1	Parallel Interface Requirements	15-22
15.9.2	Reset Operation	15-23
15.10	Operational Information	15-24
15.10.1	Initialization	15-24
15.10.1.1	Step 1 — Initialize MCR	15-24
15.10.1.2	Step 2 — Initialize ILR and IVR registers if Interrupts Employed	15-24
15.10.1.3	Step 3 — Initialize SCTL and SDATA registers	15-24
15.10.1.4	Step 4 — Enable DLCMD2 by exiting DEBUG mode	15-24
15.10.2	Transmitting a Message	15-24
15.10.3	Receiving a Message	15-25
15.10.4	Receiving a Message in Block Mode	15-26
15.10.5	Transmitting a Message in Block Mode	15-26
15.10.6	Receiving a Message in 4X Mode	15-26
15.10.7	Transmitting a Message in 4x Mode	15-27
15.11	Register Descriptions	15-27
15.11.1	Module Configuration Register (MCR)	15-27
15.11.2	Interrupt Pending Register (IPR)	15-30
15.11.3	Interrupt Level Register (ILR)	15-31
15.11.4	Interrupt Vector Register (IVR)	15-32
15.11.5	Symbol Timing Control and Pre-Scaler Register (SCTL)	15-32
15.11.6	Symbol Timing Data Register (SDATA)	15-34
15.11.7	Transmit Command Register (CMD)	15-35
15.11.8	Transmit Data Register (TDATA)	15-39
15.11.9	TxFIFO Command Load Sequences	15-39
15.11.10	Transmit Data Register (TDATA)	15-40
15.11.11	Receive Status Register (STAT)	15-41
15.11.12	Receive Data Register (RDATA)	15-44
15.11.13	Completion Code	15-44
15.11.14	Bus Errors	15-47
15.11.15	Data Link Controller Module (DLCMD2)	15-49
15.12	Mask Programmable Bus Error (BERR) Functionality	15-50
15.12.1	BERR_PLUG = 0	15-50
15.12.2	BERR_PLUG = 1	15-50
15.13	Interrupt	15-51
15.13.1	DLCMD2 Interrupts	15-51
15.13.2	Interrupt Structure	15-52

Paragraph Number

Page Number



15.14 In-Frame Response	15-54
15.14.1 IFR Operation	15-54
15.14.2 IFR Abort Conditions	15-56
15.14.3 IFR Types	15-56
15.14.3.1 Type 1 IFR	15-57
15.14.3.2 1.Type 2 IFR	15-57
15.14.3.3 Type 3 IFR	15-57
15.15 System Overview	15-58
15.16 Test Operation	15-58
15.16.1 Test Configuration Register (TCR)	15-58
15.17 Module I/O Signals	15-59
15.17.1 Signal Descriptions	15-59
15.17.2 External Connections	15-59
15.17.3 Signal Functions	15-59
15.17.3.1 CL2Tx	15-59
15.17.3.2 CL2Rx	15-60
15.17.3.3 4XEN	15-60

Section 16 CAN 2.0B CONTROLLER MODULE

16.1 Features	16-1
16.2 External Pins	16-2
16.3 TouCAN Architecture	16-3
16.3.1 Tx/Rx Message Buffer Structure	16-3
16.3.1.1 Common Fields for Extended and Standard Format Frames	16-4
16.3.1.2 Fields for Extended Format Frames	16-6
16.3.1.3 Fields for Standard Format Frames	16-6
16.3.1.4 Serial Message Buffers	16-6
16.3.1.5 Message Buffer Activation/Deactivation Mechanism	16-7
16.3.1.6 Message Buffer Lock/Release/Busy Mechanism	16-7
16.3.2 Receive Mask Registers	16-7
16.3.3 Bit Timing	16-8
16.3.3.1 Configuring the TouCAN Bit Timing	16-9
16.3.4 Error Counters	16-9
16.3.5 Time Stamp	16-10
16.4 TouCAN Operation	16-11
16.4.1 TouCAN Reset	16-11
16.4.2 TouCAN Initialization	16-11
16.4.3 Transmit Process	16-12
16.4.3.1 Transmit Message Buffer Deactivation	16-13
16.4.3.2 Reception of Transmitted Frames	16-13
16.4.4 Receive Process	16-13
16.4.4.1 Receive Message Buffer Deactivation	16-14

Paragraph Number

Page Number



16.4.4.2 Locking and Releasing Message Buffers	16-15
16.4.5 Remote Frames	16-15
16.4.6 Overload Frames	16-16
16.5 Special Operating Modes	16-16
16.5.1 Debug Mode	16-16
16.5.2 Low-Power Stop Mode	16-17
16.5.3 Auto Power Save Mode	16-18
16.6 Interrupts	16-18
16.7 Programmer's Model	16-20
16.7.1 TouCAN Module Configuration Register	16-22
16.7.2 TouCAN Test Configuration Register	16-24
16.7.3 TouCAN Interrupt Configuration Register	16-24
16.7.4 Control Register 0	16-25
16.7.5 Control Register 1	16-26
16.7.6 Prescaler Divide Register	16-27
16.7.7 Control Register 2	16-28
16.7.8 Free Running Timer	16-29
16.7.9 Receive Global Mask Registers	16-29
16.7.10 Receive Buffer 14 Mask Registers	16-30
16.7.11 Receive Buffer 15 Mask Registers	16-30
16.7.12 Error and Status Register	16-30
16.7.13 Interrupt Mask Register	16-32
16.7.14 Interrupt Flag Register	16-33
16.7.15 Error Counters	16-33

Section 17 MODULAR I/O SYSTEM (MIOS14)

17.1 Overview	17-1
17.1.1 Documentation Conventions	17-3
17.1.1.1 Terminology Definitions:	17-3
17.1.2 Bit and Byte Ordering	17-3
17.1.2.1 Supported Data Sizes	17-3
17.1.2.2 MIOS14 Port Size:	17-4
17.1.3 Submodule Numbering Convention	17-4
17.1.4 MIOS14 Module/Submodule Addressing	17-4
17.1.4.1 MIOS14 Base Address	17-4
17.1.4.2 Submodule Base Addresses	17-4
17.1.4.3 Bus Error Support	17-4
17.1.4.4 Wait States	17-4
17.1.4.5 Unimplemented Locations	17-5
17.1.4.6 Unimplemented Bits	17-5
17.2 MIOS14 Naming Convention	17-5
17.2.1 Submodule Naming Convention	17-5

Paragraph Number

Page Number



17.2.2 MIOS14 Pin Naming Convention	17-5
17.3 MIOS14 Functional Overview	17-7
17.3.1 MIOS14 Configuration	17-8
17.4 MIOS14 Feature List	17-8
17.5 MIOS14 Pin Count	17-11
17.6 Submodule Overview	17-11
17.6.1 MIOS Bus Interface Submodule (MBISM)	17-11
17.6.2 MIOS Modulus Counter Submodule (MMCSM)	17-11
17.6.3 MIOS Double Action Submodule (MDASM)	17-12
17.6.4 MIOS Pulse Width Modulation Submodule (MPWMSM)	17-13
17.6.5 MIOS 16-bit Parallel Port I/O Submodule (MPIOSM)	17-13
17.6.6 MIOS Real-Time Clock Submodule (MRTCSCM)	17-13
17.6.7 Timing Function Examples	17-13
17.6.7.1 Single-Edge Input Capture	17-14
17.6.7.2 Input Double-Edge Pulse Width Measurement	17-15
17.6.7.3 Input Double-Edge Period Measurement	17-16
17.6.7.4 Single-Edge Output Compare	17-17
17.6.7.5 Double-Edge Single Output Pulse Generation	17-18
17.6.7.6 Output Pulse Width Modulation With MDASM	17-19
17.6.7.7 Input Pulse Accumulation	17-21
17.7 MIOS14 I/O Ports	17-21
17.7.1 Using and Clearing Flag Bits	17-21
17.8 MIOS14 Bus System Description	17-21
17.8.1 Modular I/O Bus Description	17-21
17.8.2 Read/Write and Control Bus Description	17-22
17.8.3 Request Bus Description	17-22
17.8.4 Counter Bus Set Description	17-22
17.9 MIOS14 Address Map	17-22
17.9.1 Interrupts	17-24
17.9.2 MIOS14 Interrupt Structure	17-24
17.9.3 Request Submodule (RQSM)	17-25
17.9.4 MIRSM0 Registers	17-27
17.9.4.1 MIOS14SR0 Interrupt Status Register	17-27
17.9.4.2 MIOS14ER0 Interrupt Enable Registers	17-27
17.9.4.3 MIOS14RPR0 Request Pending Register	17-28
17.9.5 MIRSM1 Registers	17-28
17.9.5.1 MIOS14SR1 Interrupt Status Register	17-28
17.9.5.2 MIOS14ER1 Interrupt Enable Registers	17-29
17.9.5.3 MIOS14RPR1 Request Pending Register	17-29
17.9.6 MBISM Interrupt Registers	17-30
17.9.6.1 MIOS14LVL0 Register	17-30
17.9.6.2 MIOS14LVL1 Register	17-30
17.9.7 Interrupt Control Section (ICS)	17-30

Paragraph Number

Page Number



17.9.7.1 Non-Vectored Interrupt	17-31
17.10 Bus Interface Submodule (MBISM)	17-31
17.10.1 MBISM Overview Description	17-31
17.10.2 MBISM Registers	17-31
17.10.2.1 MBISM Registers Organization	17-31
17.10.2.2 MIOS14 Test and Pin Control Register (MIOS14TPCR)	17-32
17.10.2.3 MIOS14 Vector Register (MIOS14VECT)	17-33
17.10.2.4 MIOS14 Module-Version Number Register (MIOS14VNR)	17-33
17.10.2.5 MIOS14 Module Configuration Register (MIOS14MCR)	17-33
17.11 Counter Prescaler Submodule (MCPSM)	17-34
17.11.1 MCPSM Overview Description	17-34
17.11.1.1 MCPSM features	17-35
17.11.1.2 MCPSM Pin Functions	17-35
17.11.1.3 Modular I/O Bus (MIOB) Interface	17-35
17.11.2 Effect of RESET on MCPSM	17-36
17.11.3 MCPSM Registers	17-36
17.11.3.1 MCPSM Registers Organization.	17-36
17.11.3.2 MCPSMSCR — MCPSM Status/Control Register	17-36
17.12 Modulus Counter Submodule (MMCSM)	17-37
17.12.1 MMCSM Overview Description.	17-37
17.12.2 MMCSM features	17-39
17.12.2.1 MMCSM Pin Functions.	17-39
17.12.3 MMCSM Prescaler	17-40
17.12.4 Modular I/O Bus (MIOB) Interface	17-40
17.12.5 Effect of RESET on MMCSM	17-40
17.12.6 MMCSM Registers	17-41
17.12.7 MMCSM Register Organization	17-41
17.12.8 MMCSM Up-Counter Register (MMCSMCNT)	17-42
17.12.8.1 MMCSM Modulus Latch Register (MMCSMML)	17-42
17.12.8.2 MMCSMSCRD — MMCSM Status/Control Register (Duplicated)	17-43
17.12.8.3 MMCSM Status/Control Register (MMCSMSCR)	17-43
17.12.9 Double Action Submodule (MDASM)	17-45
17.12.10 MDASM Overview Description	17-45
17.12.11 MDASM Features	17-46
17.12.11.1 MDASM Pin Functions	17-47
17.12.12 MDASM Description	17-47
17.12.13 MDASM Modes of Operation	17-48
17.12.13.1 Disable (DIS) Mode	17-49
17.12.13.2 Input Pulse Width Measurement (IPWM) Mode	17-49
17.12.14 Input Period Measurement (IPM) Mode	17-50
17.12.15 Input Capture (IC) Mode.	17-51
17.12.15.1 Output Compare (OCB and OCAB) Modes	17-52
17.12.15.2 Single Shot Output Pulse Operation.	17-53



17.12.15.3	Single Output Compare operation	17-54
17.12.15.4	Output Port Bit operation	17-55
17.12.15.5	Output Pulse Width Modulation (OPWM) mode	17-55
17.12.16	Modular I/O Bus (MIOB) Interface	17-57
17.12.17	Effect of RESET on MDASM	17-58
17.12.18	MDASM Registers	17-58
17.12.18.1	MDASM Registers Organization	17-58
17.12.18.2	MDASM DataA (MDASMAR) Register Bits	17-60
17.12.18.3	MDASM DataB (MDASMBR) Register Bits	17-61
17.12.19	MDASMSCR — MDASM Status/Control Register (Duplicated)	17-62
17.12.20	MDASMSCR — MDASM Status/Control Register	17-62
17.13	Pulse Width Modulation Submodule (MPWMSM)	17-64
17.13.1	MPWMSM Overview Description	17-64
17.13.2	MPWMSM Terminology	17-65
17.13.2.1	MPWMSM Features	17-65
17.13.3	MPWMSM Description	17-66
17.13.3.1	Clock Selection	17-67
17.13.3.2	Counter	17-67
17.13.3.3	Period Register	17-67
17.13.3.4	Pulse Width Registers	17-68
17.13.3.5	0% and 100% Duty Cycles	17-69
17.13.3.6	Tables	17-70
17.13.3.7	MPWMSM Status and Control Register (SCR)	17-70
17.13.3.8	MPWMSM Interrupt	17-71
17.13.3.9	MPWMSM Port Functions	17-71
17.13.3.10	MPWMSM Data Coherency	17-71
17.13.4	MIO Bus (MIOB) Interface	17-72
17.13.5	Effect of RESET on MPWMSM	17-72
17.13.6	MPWMSM Registers	17-72
17.13.6.1	MPWMSM Registers Organization	17-72
17.13.6.2	MPWMPERR — MPWMSM Period Register	17-74
17.13.6.3	MPWMPULR — MPWMSM Pulse Width Register	17-75
17.13.6.4	MPWMCNTR — MPWMSM Counter Register	17-76
17.13.6.5	MPWMSCR — MPWMSM Status/Control Register	17-76
17.14	Parallel Port I/O Submodule (MPIO SM)	17-79
17.14.1	MPIO SM Overview Description	17-79
17.14.2	MPIO SM features	17-80
17.14.3	MPIO SM Pin Functions	17-80
17.14.4	MPIO SM Description	17-80
17.14.4.1	MPIO SM Port function	17-80
17.14.4.2	Non-Bonded MPIO SM Pads	17-81
17.14.5	Modular I/O Bus (MIOB) Interface	17-81
17.14.6	Effect of RESET on MPIO SM	17-81

Paragraph Number

Page Number



17.14.7	MPIOSM Testing	17-81
17.14.8	MPIOSM Registers	17-81
17.14.9	MPIOSM Register Organization	17-82
17.14.9.1	MPIOSMDR — MPIOSM Data Register	17-82
17.14.9.2	MPIOSMDDR — MPIOSM Data Direction Register	17-82
17.15	Real-Time Clock Submodule (MRTCSM)	17-82
17.15.1	MRTCSM Overview Description	17-83
17.15.1.1	MRTCSM Terminology	17-83
17.15.1.2	MRTCSM Features	17-83
17.15.1.3	MRTCSM Pad Functions	17-85
17.15.2	MRTCSM Description	17-85
17.15.2.1	Oscillator	17-85
17.15.2.2	Standby Supply and Power Switch	17-85
17.15.2.3	Counter Chain	17-86
17.15.2.4	15-Bit Prescaler	17-87
17.15.2.5	32-Bit Free-running Counter	17-87
17.15.2.6	15-Bit Prescaler and 32-Bit Free-Running Counter Buffers	17-87
17.15.3	Modes of Operation	17-87
17.15.3.1	Enabling the MRTCSM	17-87
17.15.3.2	15-Bit Prescaler and 32-Bit Free-Running Counter Buffer Updates	17-88
17.15.3.3	Read of 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers	17-88
17.15.3.4	Write to 15-Bit Prescaler and 32-Bit Free-Running Counter Buffers	17-89
17.15.4	MRTCSM Interrupt	17-90
17.15.5	Chip Wake-Up Feature	17-90
17.15.6	Modular I/O Bus (MIOB) Interface	17-90
17.15.6.1	Low Power Mode — Peripheral Bus Clock Running	17-90
17.15.6.2	Low Power Mode — Peripheral Bus Clock Stopped	17-90
17.15.7	Effect of Standby Mode on MRTCSM	17-91
17.15.8	Effect of RESET on MRTCSM	17-91
17.15.9	MRTCSM Registers	17-92
17.15.10	MRTCSM Register Organization	17-92
17.15.10.1	MRTCSM Free-Running Counter High Buffer (MRTCFRCH) Register Bits ..	17-92
17.15.10.2	MRTCSM Free-Running Counter Low Buffer (MRTCFRCL) Register Bits ..	17-93
17.15.10.3	MRTCSM Prescaler Counter Buffer (MRTCPB) Register Bits	17-93
17.15.10.4	MRTCSMSCR — MRTCSM Status/Control Register	17-93

Section 18 TIME PROCESSOR UNIT 3

18.1	Overview	18-1
18.2	TPU3 Components	18-2
18.2.1	Time Bases	18-2
18.2.2	Timer Channels	18-2
18.2.3	Scheduler	18-2

Paragraph Number

Page Number



18.2.4	Microengine	18-2
18.2.5	Host Interface	18-3
18.2.6	Parameter RAM	18-3
18.3	TPU Operation	18-3
18.3.1	Event Timing	18-3
18.3.2	Channel Orthogonality	18-3
18.3.3	Interchannel Communication	18-4
18.3.4	Programmable Channel Service Priority	18-4
18.3.5	Coherency	18-4
18.3.6	Emulation Support	18-4
18.3.7	TPU3 Interrupts	18-5
18.3.8	Prescaler Control for TCR1	18-5
18.3.9	Prescaler Control for TCR2	18-7
18.4	Programming Model	18-8
18.4.1	TPU Module Configuration Register	18-11
18.4.2	TPU3 Test Configuration Register	18-13
18.4.3	Development Support Control Register	18-13
18.4.4	Development Support Status Register	18-15
18.4.5	TPU3 Interrupt Configuration Register	18-15
18.4.6	Channel Interrupt Enable Register	18-16
18.4.7	Channel Function Select Registers	18-16
18.4.8	Host Sequence Registers	18-18
18.4.9	Host Service Request Registers	18-18
18.4.10	Channel Priority Registers	18-19
18.4.11	Channel Interrupt Status Register	18-20
18.4.12	Link Register	18-21
18.4.13	Service Grant Latch Register	18-21
18.4.14	Decoded Channel Number Register	18-21
18.4.15	TPU3 Module Configuration Register 2	18-21
18.4.16	TPU Module Configuration Register 3	18-23
18.4.17	TPU3 Test Registers	18-23
18.4.18	TPU3 Parameter RAM	18-23
18.5	Time Functions	18-24

Section 19 DUAL-PORT TPU RAM (DPTRAM)

19.1	Features	19-2
19.2	DPTRAM Configuration and Block Diagram	19-2
19.3	Programming Model	19-2
19.3.1	DPTRAM Module Configuration Register (DPTMCR)	19-4
19.3.2	DPTRAM Test Register	19-5
19.3.3	Ram Base Address Register (RAMBAR)	19-5
19.3.4	MISR High (MISRH) and MISR Low (MISRL)	19-5



19.3.5 MISC Counter (MISCNT)	19-6
19.4 Operation	19-6
19.4.1 Normal Operation	19-6
19.4.2 Standby Operation	19-7
19.4.3 Reset Operation	19-7
19.4.4 Stop Operation	19-7
19.4.5 Freeze Operation	19-8
19.4.6 TPU3 Emulation Mode Operation	19-8
19.5 Multiple Input Signature Calculator (MISC)	19-8

Section 20

CDR3 FLASH (UC3F) EEPROM

20.1 Introduction	20-1
20.1.1 Features of the CDR3 FLASH EEPROM (UC3F)	20-3
20.1.2 Glossary of Terms Used	20-4
20.2 UC3F Interface	20-5
20.2.1 External Interface	20-5
20.3 Programmer's Model	20-6
20.3.0.1 UC3F EEPROM Module Control Register Addressing	20-6
20.3.1 UC3F EEPROM Control Registers	20-6
20.3.2 UC3F EEPROM Configuration Register (UC3FMCR)	20-7
20.3.3 UC3F EEPROM Extended Configuration Register (UC3FMCRE)	20-10
20.3.4 UC3F EEPROM High Voltage Control Register (UC3FCTL)	20-13
20.3.5 UC3F EEPROM Array Addressing	20-17
20.3.6 UC3F EEPROM Shadow Row	20-17
20.3.6.1 Reset Configuration Word (UC3FCFIG)	20-18
20.3.7 UC3F EEPROM 512-Kbyte Array Configuration	20-21
20.4 Operation	20-22
20.4.1 Reset	20-22
20.4.2 Register Read and Write Operation	20-23
20.4.3 Array Read Operation	20-23
20.4.3.1 Array On-Page Read Operation	20-24
20.4.4 Shadow Row Select Read Operation	20-24
20.4.5 Array Program/Erase Interlock Write Operation	20-24
20.4.6 High Voltage Operations	20-24
20.4.6.1 Overview of Program/Erase Operation	20-24
20.4.7 Programming	20-24
20.4.7.1 Program Sequence	20-25
20.4.7.2 Program Shadow Information	20-28
20.4.7.3 Program Suspend	20-28
20.4.8 Erasing	20-28
20.4.8.1 Erase Sequence	20-29
20.4.8.2 Erasing Shadow Information Words	20-31

Paragraph Number

Page Number



20.4.8.3 Erase Suspend	20-31
20.4.9 Stop Operation	20-32
20.4.10 Disabled	20-32
20.4.11 Censored Accesses and Non-Censored Accesses	20-33
20.4.11.1 Setting and Clearing Censor	20-34
20.4.11.2 Setting Censor	20-35
20.4.11.3 Clearing Censor	20-35
20.4.11.4 Switching The UC3F EEPROM Censorship.	20-36
20.4.12 Background Debug Mode or Freeze Operation	20-37

Section 21 CALRAM OPERATION

21.1 Definitions and Acronyms	21-1
21.1.1 Key Feature List	21-2
21.2 CALRAM Introduction	21-2
21.3 Modes of Operation	21-6
21.3.1 Reset	21-6
21.3.2 One-Cycle Mode.	21-6
21.3.2.1 CALRAM Access/Privilege Violations.	21-6
21.3.3 Two-Cycle Mode.	21-7
21.3.4 Standby Operation / Keep-Alive Power.	21-7
21.3.5 Stop Operation	21-7
21.3.6 Overlay Mode Operation	21-7
21.3.6.1 Overlay Mode Configuration.	21-8
21.3.6.2 Priority of Overlay Regions.	21-13
21.3.6.3 Normal (Non-Overlay) Access to Overlay Regions	21-13
21.3.6.4 Calibration Write Cycle Flow	21-14
21.4 Register Definitions	21-14
21.4.1 CALRAM Module Configuration Register (CRAMMCR)	21-15
21.4.2 CALRAM Region Base Address Registers (CRAM_RBAX)	21-18
21.4.3 CALRAM Overlay Configuration Register (CRAMOVLCR)	21-20
21.4.4 CALRAM Ownership Trace Register (CRAMOTR)	21-21

Section 22 DEVELOPMENT SUPPORT

22.1 Overview	22-1
22.2 Program Flow Tracking	22-1
22.2.1 Program Trace Cycle	22-2
22.2.1.1 Instruction Queue Status Pins — VF [0:2]	22-3
22.2.1.2 History Buffer Flushes Status Pins— VFLS [0..1]	22-4
22.2.1.3 Queue Flush Information Special Case	22-4
22.2.2 Program Trace when in Debug Mode.	22-4
22.2.3 Sequential Instructions Marked as Indirect Branch	22-4
22.2.4 The External Hardware.	22-5



22.2.4.1	Synchronizing the Trace Window to the CPU Internal Events	22-5
22.2.4.2	Detecting the Trace Window Start Address	22-6
22.2.4.3	Detecting the Assertion/Negation of VSYNC	22-6
22.2.4.4	Detecting the Trace Window End Address.	22-7
22.2.4.5	Compress	22-7
22.2.5	Instruction Fetch Show Cycle Control	22-7
22.3	Watchpoints and Breakpoints Support.	22-8
22.3.1	Internal Watchpoints and Breakpoints	22-10
22.3.1.1	Restrictions.	22-12
22.3.1.2	Byte and Half-Word Working Modes	22-12
22.3.1.3	Examples	22-13
22.3.1.4	Context Dependent Filter	22-14
22.3.1.5	Ignore First Match.	22-15
22.3.1.6	Generating Six Compare Types.	22-15
22.3.2	Instruction Support	22-15
22.3.2.1	Load/Store Support	22-16
22.3.3	Watchpoint Counters	22-20
22.3.3.1	Trap Enable Programming	22-20
22.4	Development System Interface	22-20
22.4.1	Debug Mode Support	22-23
22.4.1.1	Debug Mode Enable vs. Debug Mode Disable.	22-25
22.4.1.2	Entering Debug Mode.	22-25
22.4.1.3	The Check Stop State and Debug Mode	22-28
22.4.1.4	Saving Machine State upon Entering Debug Mode	22-28
22.4.1.5	Running in Debug Mode.	22-29
22.4.1.6	Exiting Debug Mode	22-29
22.5	Development Port	22-30
22.5.1	Development Port Pins.	22-30
22.5.2	Development Serial Clock	22-30
22.5.3	Development Serial Data In	22-30
22.5.4	Development Serial Data Out.	22-31
22.5.5	Freeze Signal	22-31
22.5.5.1	SGPIO6/FRZ/ $\overline{\text{PTR}}$ Pin	22-31
22.5.5.2	IWP[0:1]/VFLS[0:1] Pins.	22-31
22.5.5.3	VFLS[0:1]_MPIO32B[3:4] Pins.	22-31
22.5.6	Development Port Registers.	22-31
22.5.6.1	Development Port Shift Register	22-32
22.5.6.2	Trap Enable Control Register.	22-32
22.5.6.3	Development Port Registers Decode	22-32
22.5.6.4	Development Port Serial Communications — Clock Mode Selection	22-32
22.5.6.5	Development Port Serial Communications — Trap Enable Mode	22-37
22.5.6.6	Serial Data into Development Port — Trap Enable Mode	22-37
22.5.6.7	Serial Data Out of Development Port — Trap Enable Mode	22-38



22.5.6.8 Development Port Serial Communications — Debug Mode	22-38
22.5.6.9 Serial Data Into Development Port	22-39
22.5.6.10 Serial Data Out of Development Port	22-40
22.5.6.11 Fast Download Procedure	22-40
22.6 Software Monitor Debugger Support	22-42
22.6.1 Freeze Indication	22-42
22.7 Development Support Registers	22-42
22.7.1 Register Protection	22-43
22.7.2 Comparator A–D Value Registers (CMPA–CMPD)	22-44
22.7.3 Comparator E–F Value Registers	22-45
22.7.4 Breakpoint Address Register (BAR)	22-45
22.7.5 Comparator G–H Value Registers (CMPG–CMPH)	22-45
22.7.6 I-Bus Support Control Register	22-46
22.7.7 L-Bus Support Control Register 1	22-48
22.7.8 L-Bus Support Control Register 2	22-49
22.7.9 Breakpoint Counter A Value and Control Register	22-50
22.7.10 Breakpoint Counter B Value and Control Register	22-51
22.7.11 Exception Cause Register (ECR)	22-51
22.7.12 Debug Enable Register (DER)	22-53
22.7.13 Development Port Data Register (DPDR)	22-55

Section 23 READI MODULE

23.1 Overview	23-1
23.1.1 General Description	23-1
23.1.2 Feature Summary List	23-1
23.1.3 Functional Block Diagram	23-2
23.1.4 Modes of Operation	23-3
23.1.4.1 READI Reset Configuration	23-4
23.1.4.2 Security	23-4
23.1.4.3 Disabled	23-4
23.1.5 Parametrics	23-4
23.1.6 Programmer's Model	23-5
23.1.7 Messages	23-5
23.1.8 Terms and Definitions	23-6
23.2 Programmer's Model	23-8
23.2.1 Register Map	23-8
23.2.1.1 User Mapped Register	23-8
23.2.1.2 Tool Mapped Registers	23-9
23.2.1.3 Device ID (DID) Register	23-9
23.2.1.4 Development Control (DC) Register	23-10
23.2.1.5 RCPD Development Access Modes	23-11
23.2.1.6 User Base Address (UBA) Register	23-11



23.2.1.7	Read/Write Access (RWA) Register	23-13
23.2.1.8	Upload/Download Information (UDI) Register	23-14
23.2.1.9	Data Trace Attributes 1 and 2 (DTA1 and DTA2) Registers	23-16
23.2.2	Accessing Memory Mapped Locations Via the Auxiliary Port	23-17
23.2.3	Accessing READI Tool Mapped Registers Via the Auxiliary Port	23-18
23.2.4	Partial Register Updates	23-19
23.2.5	Programming Considerations	23-19
23.2.5.1	Program Trace Guidelines	23-19
23.2.5.2	Compressed Code Mode Guidelines	23-19
23.2.5.3	Reset Sequence Guidelines	23-21
23.2.5.4	BDM Guidelines	23-21
23.3	Pin Interface	23-21
23.3.1	Functional Description	23-21
23.3.1.1	Pins Implemented	23-21
23.3.2	Functional Block Diagram	23-22
23.3.2.1	Message Priority	23-23
23.3.2.2	Pin Protocol	23-23
23.3.2.3	Messages	23-26
23.3.2.4	Message Formats	23-29
23.3.2.5	Rules of Messages	23-31
23.3.2.6	Examples	23-31
23.3.2.7	Non-Temporal Ordering of Transmitted Messages	23-33
23.3.3	READI Reset Configuration	23-33
23.3.3.1	Reset Configuration for Debug Mode	23-34
23.3.3.2	Reset Configuration for Non-Debug Mode	23-34
23.3.3.3	Secure Mode	23-34
23.3.3.4	Disabled Mode	23-34
23.3.3.5	Guidelines For Transmitting Input Messages	23-35
23.4	Program Trace	23-35
23.4.1	Branch Trace Messaging	23-35
23.4.1.1	RCPU Instructions that Cause BTM Messages	23-36
23.4.2	Review of RCPU Instruction Execution	23-36
23.4.2.1	RCPU Pipeline and Execution Model	23-36
23.4.2.2	RCPU Branch Trace Indicators	23-38
23.4.3	BTM Message Formats	23-40
23.4.3.1	Direct Branch Messages	23-40
23.4.3.2	Indirect Branch Messages	23-40
23.4.3.3	Program Trace Correction Message	23-41
23.4.3.4	Error Message (Queue Overflow)	23-44
23.4.3.5	Program Trace Synchronization Messages	23-45
23.4.3.6	Direct Branch Synchronization Message	23-46
23.4.3.7	Indirect Branch Synchronization Message	23-46
23.4.3.8	Direct Branch Synchronization Message With Compressed Code	23-47

Paragraph Number

Page Number



23.4.3.9 Indirect Branch Synchronization Message with Compressed Code	23-47
23.4.3.10 Relative Addressing	23-47
23.4.4 BTM Operation	23-48
23.4.4.1 BTM Capture and Encoding Algorithm	23-48
23.4.4.2 Instruction Fetch Snooping	23-48
23.4.4.3 Instruction Execution Tracking	23-49
23.4.4.4 Instruction Flush Cases	23-51
23.4.5 BTM Queueing	23-51
23.4.6 Timing Diagram	23-52
23.4.7 Program Trace Guidelines	23-56
23.5 Data Trace	23-56
23.5.1 Data Trace for the Load/Store Bus (L-bus)	23-56
23.5.2 Data Trace Message Formats	23-56
23.5.2.1 Data Write Message	23-57
23.5.2.2 Data Read Message	23-57
23.5.2.3 Data Trace Synchronization Messages	23-57
23.5.2.4 Data Write Synchronization Message	23-58
23.5.2.5 Data Read Synchronization Messaging	23-58
23.5.2.6 Relative Addressing	23-59
23.5.3 Error Message (Queue Overflow)	23-59
23.5.4 Data Trace Operation	23-59
23.5.5 Data Trace Windowing	23-60
23.5.6 Special L-bus Cases	23-61
23.5.7 Data Trace Queueing	23-61
23.5.8 Throughput and Latency	23-62
23.5.8.1 Assumptions for Throughput Analysis	23-62
23.5.8.2 Throughput Calculations	23-62
23.5.9 Timing Diagrams	23-62
23.6 Read/Write Access	23-64
23.6.1 Functional Description	23-64
23.6.2 Write Operation to Memory Mapped Locations and PowerPC Registers	23-66
23.6.2.1 Single Write Operation	23-66
23.6.2.2 Block Write Operation	23-66
23.6.3 Read Operation to Memory Mapped Locations and PowerPC Registers	23-67
23.6.3.1 Single Read Operation	23-67
23.6.3.2 Block Read Operation	23-68
23.6.4 Read/Write Access to Internal READI Registers	23-69
23.6.4.1 Write Operation	23-69
23.6.4.2 Read Operation	23-69
23.6.5 Error Handling	23-69
23.6.5.1 Access Alignment	23-69
23.6.5.2 L-bus Address Error	23-70
23.6.5.3 L-bus Data Error	23-70

Paragraph Number

Page Number



23.6.6	Exception Sequences	23-70
23.6.7	Secure Mode	23-71
23.6.8	Error Messages	23-71
23.6.8.1	Read/Write Access Error	23-71
23.6.8.2	Invalid Message	23-71
23.6.8.3	Invalid Access Opcode	23-72
23.6.9	Faster Read/Write Accesses With Default Attributes	23-72
23.6.10	Throughput and Latency	23-72
23.6.10.1	Assumptions for Throughput Analysis	23-72
23.7	Timing Diagrams	23-74
23.8	Watchpoint Support	23-77
23.8.1	Watchpoint Messaging	23-77
23.8.1.1	Watchpoint Source Field	23-78
23.8.2	Error Message (Watchpoint Overrun)	23-78
23.8.3	Synchronization	23-79
23.8.4	Timing Diagrams	23-79
23.9	Ownership Trace	23-79
23.9.1	Ownership Trace Messaging	23-80
23.9.2	Error Message (Queue Overflow)	23-80
23.9.2.1	OTM Flow	23-80
23.9.2.2	OTM Queueing	23-81
23.9.3	Timing Diagram	23-81
23.10	RCPU Development Access	23-82
23.10.1	RCPU Development Access Messaging	23-83
23.10.1.1	DSDI Message	23-83
23.10.1.2	DSDO Message	23-84
23.10.1.3	BDM Status Message	23-84
23.10.1.4	Error Message (Invalid Message)	23-85
23.10.2	RCPU Development Access Operation	23-85
23.10.2.1	Enabling RCP Development Access Via READI Pins	23-86
23.10.2.2	Enabling Background Debug Mode (BDM) via READI Pins	23-86
23.10.2.3	Entering Background Debug Mode (BDM) Via READI Pins	23-87
23.10.2.4	Non-Debug Mode Access of RCP Development Access	23-87
23.10.2.5	RCPU Development Access Flow Diagram	23-87
23.10.3	Throughput	23-89
23.10.4	Timing Diagrams	23-89
23.11	Power Management	23-92
23.11.1	Functional Description	23-92
23.11.2	Low Power Modes	23-93
23.12	Application Notes	23-93
23.12.1	Automotive Calibration	23-93
23.12.1.1	Calibration Variable Acquisition	23-93
23.12.2	Calibration Variables Located In Contiguous Memory Locations	23-94

Paragraph Number

Page Number



23.12.2.1 Data Read Messaging	23-94
23.12.2.2 Read/Write Access	23-94
23.12.3 Calibration Variables Not Located in Contiguous Memory Locations	23-94
23.12.3.1 Data Write Messaging	23-94
23.12.3.2 Read/Write Access	23-95
23.12.3.3 Calibration Constant Tuning	23-96
23.12.4 UC3F Programming Guideline Flowchart via READI Read/Write Access	23-96

Section 24

IEEE 1149.1-COMPLIANT INTERFACE (JTAG)

24.1 IEEE 1149.1 Test Access Port (TAP) and Joint Test Action Group (JTAG)	24-1
24.2 IEEE 1149.1 Test Access Port	24-1
24.2.1 Overview	24-2
24.2.1.1 TAP CONTROLLER	24-3
24.2.1.2 Boundary Scan Register	24-4
24.2.2 Instruction Register	24-23
24.2.2.1 EXTEST	24-24
24.2.2.2 SAMPLE/PRELOAD	24-24
24.2.2.3 BYPASS	24-24
24.2.2.4 CLAMP	24-25
24.2.3 HI-Z	24-25
24.3 MPC565 / MPC566 Restrictions	24-25
24.3.1 Non-Scan Chain Operation	24-26
24.3.2 Motorola MPC565 / MPC566 BSDL Description	24-27

Appendix A

INTERNAL MEMORY MAP

Appendix B

REGISTER GENERAL INDEX

Appendix C

REGISTER DIAGRAM INDEX

Appendix D

TPU ROM FUNCTIONS

D.1 Overview	D-1
D.2 Programmable Time Accumulator (PTA)	D-4
D.3 Queued Output Match TPU Function (QOM)	D-6
D.4 Table Stepper Motor (TSM)	D-8
D.5 Frequency Measurement (FQM)	D-11
D.6 Universal Asynchronous Receiver/Transmitter (UART)	D-13
D.7 New Input Capture/Transition Counter (NITC)	D-16
D.8 Multiphase Motor Commutation (COMM)	D-18
D.9 Hall Effect Decode (HALLD)	D-20
D.10 Multichannel Pulse-Width Modulation (MCPWM)	D-22
D.11 Fast Quadrature Decode TPU Function (FQD)	D-29

Paragraph Number

Page Number



D.12	Period/Pulse-Width Accumulator (PPWA)	D-32
D.13	Output Compare (OC)	D-34
D.14	Pulse-Width Modulation (PWM)	D-36
D.15	Discrete Input/Output (DIO)	D-38
D.16	Synchronized Pulse-Width Modulation (SPWM)	D-40
D.17	Read / Write Timers and Pin TPU Function (RWTPIN)	D-43
D.18	ID TPU Function (ID)	D-45
D.19	Serial Input/Output Port (SIOP)	D-47
D.19.1	Parameters	D-48
D.19.1.1	CHAN_CONTROL	D-49
D.19.1.2	BIT_D	D-50
D.19.1.3	HALF_PERIOD	D-50
D.19.1.4	BIT_COUNT	D-50
D.19.1.5	XFER_SIZE	D-50
D.19.1.6	SIOP_DATA	D-50
D.19.2	Host CPU Initialization of the SIOP Function	D-51
D.19.3	SIOP Function Performance	D-51
D.19.3.1	XFER_SIZE Greater Than 16	D-52
D.19.3.2	Data Positioning	D-52
D.19.3.3	Data Timing	D-52

Appendix E ELECTRICAL CHARACTERISTICS

E.1	Absolute Maximum Ratings (VSS = 0V)	E-2
E.2	Package	E-3
E.3	EMI Characteristics	E-3
E.3.1	Reference Documents	E-3
E.3.2	Definitions and Acronyms	E-3
E.3.3	EMI Testing Specifications	E-3
E.4	Thermal Characteristics	E-4
E.4.1	Thermal References	E-6
E.5	ESD Protection	E-7
E.6	DC Electrical Characteristics	E-7
E.7	Oscillator and PLL Electrical Characteristics	E-12
E.8	Flash Electrical Characteristic	E-12
E.9	Power-Up/Down Sequencing	E-13
E.9.1	Power-Up/Down Option A	E-14
E.9.2	Power-Up/Down Option B	E-16
E.10	Issues Regarding Power Sequence	E-19
E.10.1	Flash Issue	E-19
E.10.2	Keep-Alive RAM	E-19
E.11	Timing	E-20
E.12	Debug Port Timing	E-45
E.13	Pin Electrical Characteristics	E-46
E.13.1	AC Electrical Characteristics	E-46
E.14	RESET Timing	E-49
E.15	IEEE 1149.1 Electrical Characteristics	E-53
E.16	QADC64E Electrical Characteristics	E-57
E.17	QSMCM Electrical Characteristics	E-58
E.18	GPIO Electrical Characteristics	E-61
E.19	TPU3 Electrical Characteristics	E-62
E.20	TouCAN Electrical Characteristics	E-63
E.21	MIOS Timing Characteristics	E-63

Paragraph Number		Page Number
E.21.1	MPWMSM Timing Characteristics	E-64
E.21.2	MMCSM Timing Characteristics.	E-67
E.21.3	MDASM Timing Characteristics	E-70
E.22	MSASM Timing Characteristics	E-73
E.22.1	MPIO SM Timing Characteristics	E-76



INDEX

Online publishing by JABIS™, <http://www.jabis.com>