



## APPENDIX B REGISTER GENERAL INDEX

### –B–

BAR (ROMBAH, ROMBAL)  
    base address register (BAR — ROMBAH, ROMBAL) 12-5  
BIUMCR (BIUSM module configuration register) 13-51  
BIUSM  
    module configuration register (BIUMCR) 13-51, 13-54  
    time base register (BIUTBR) 13-52  
BIUTBR (BIUSM time base register) 13-52

### –C–

CANCTRL0 (control register 0) 7-26  
CANCTRL1 (control register 1) 7-27  
CANCTRL2 (control register 2) 7-29  
CANICR (TouCAN interrupt configuration register) 7-25  
CANMCR (TouCAN module configuration register) 7-23  
CCW (conversion command word table) 5-48  
CFSR0 (TPU3 channel function select register 0) 8-15  
CFSR1 (TPU3 channel function select register 1) 8-15  
CFSR2 (TPU3 channel function select register 2) 8-15  
CFSR3 (TPU3 channel function select register 3) 8-15  
CIER (TPU3 channel interrupt enable register) 8-14  
CISR (TPU3 channel interrupt status register) 8-18  
CMFI  
    CMFI EEPROM configuration register (CMFIMCR) 10-9  
    CMFI high voltage control register (CMFICTLx) 10-16  
CMFIBAH (CMFI base address high register) 10-15  
CMFIBAL (CMFI base address low register) 10-15  
CMFIBS0 (CMFI bootstrap information words) 10-19  
CMFIBS01 (CMFI bootstrap information words) 10-19  
CMFIBS2 (CMFI bootstrap information words) 10-19  
CMFIBS3 (CMFI bootstrap information words) 10-20  
CMFICTL1 (CMFI high voltage control register 1) 10-16  
CMFICTL2 (CMFI high voltage control register 2) 10-12, 10-17  
CMFIMCR (CMFI EEPROM configuration register) 10-10  
CPCR (CPSM control register) 13-54  
CPR0 (TPU3 channel priority register 0) 8-17  
CPR1 (TPU3 channel priority register 1) 8-17  
CSBAR (SCIM2 chip-select base address register) 4-80  
CSBARBT (SCIM2 chip-select base boot register) 4-79  
CSOR (SCIM2 chip select option register) 4-81  
CSORBT (SCIM2 chip-select option boot register) 4-80  
CSPAR0 (SCIM2 chip-select pin assignment register 0) 4-76  
CSPAR1 (SCIM2 chip-select pin assignment register 1) 4-76

### –D–

DASM  
    data register A (DASMA) 13-37  
    data register B (DASMB) 13-38  
    status/interrupt control register (DASMSIC) 13-35  
DASMA (DASM data register A) 13-37, 13-38



DASMSIC (DASM status/interrupt control register) 13-35  
DDRAB, DDRE (SCIM2 port E data direction registers) 4-89  
DDRAB, PEPAR (SCIM2 port E pin assignment register) 4-89  
DDRF (SCIM2 port F data direction register) 4-92  
DDRG, DDRH (SCIM2 port G,H data direction registers) 4-94  
DDRQA (PORTQA data direction register) 5-37  
DDRQS (PORTQS data direction register) 6-12  
DPTBAR (RAM array base address register) 9-5  
DPTMCR (DPTRAM module configuration register) 9-3  
DPTRAM  
    module configuration register (DPTMCR) 9-3  
    RAMbase address register (DPTBAR) 9-4  
    test register 9-4  
DSCR (TPU3 development support control register) 8-12  
DSSR (TPU3 development support status register) 8-13

–E–

ESTAT (error and status register) 7-31

–F–

FCSM

    status/interrupt control register (FMSMSIC) 13-7  
FCSMCNT (FCSM counter register) 13-9  
FCSMSIC (FCSM status/interrupt control register) 13-7

–H–

HSQR0 (TPU3 host sequence register 0) 8-16  
HSQR1 (TPU3 host sequence register 1) 8-16  
HSSR0 (TPU3 host service request register 0) 8-16  
HSSR1 (TPU3 host service request register 1) 8-16

–I–

IFLAG (interrupt flag register) 7-33  
IMASK (interrupt mask register) 7-33

–L–

LJSRR (left justified, signed result register) 5-51  
LJURR (left justified, unsigned result register) 5-51

–M–

MCSM

    counter register (MCSMCNT) 13-14  
    status/interrupt control register (MCSMSIC) 13-12  
MCSMCNT (MCSM counter register) 13-14  
MCSMML (MCSM modulus latch register) 13-14  
MCSMSIC (MCSM status/interrupt control register) 13-12  
MISCNT (MISC counter) 9-6  
MISRH (multiple input signature register high) 9-5  
MISRL (multiple input signature register low) 9-5

–P–

PFIVR (SCIM2 port F edge-detect interrupt vector register) 4-93  
PFLVR (SCIM2 port F edge-detect interrupt level register) 4-93  
PFPAR (SCIM2 port F pin assignment register) 4-92  
PICR (SCIM2 periodic interrupt control register) 4-31  
PITR (SCIM2 periodic interrupt timer register) 4-31



PORTA-B (SCIM2 port A and B data registers) 4-88  
PORTC (SCIM2 PORTC data register) 4-78  
PORTE (SCIM2 port E data registers) 4-89  
PORTF (SCIM2 port F data registers) 4-91  
PORTFE (SCIM2 port F edge-detect flag register) 4-93  
PORTG, PORTH (SCIM2 port G,H data registers) 4-94  
PORTQA (port QA data register) 5-36  
PORTQB (port QB data register) 5-36  
PORTQS (port QS data register) 6-10  
PQSPAR (PORTQS pin assignment register) 6-11  
PRESDIV (prescaler divide register) 7-28  
PWM  
    counter register (PWMC) 13-49  
    period register (PWMA) 13-48  
    pulse width register (PWMB) 13-49  
PWMA (PWM period register) 13-49  
PWMB (PWM pulse width register) 13-49  
PWMC (PWM counter register) 13-50  
PWMSIC (PWSM status/interrupt control register) 13-45

—Q—

QACR0 (QADC64 control register 0) 5-37  
QACR1 (QADC64 control register 1) 5-38  
QACR2 (QADC64 control register 2) 5-40  
QADC64  
    control register 0 (QACR0) 5-37  
    control register 1 (QACR1) 5-38  
    control register 2 (QACR2) 5-40  
    interrupt register (QADC64INT) 5-35  
    port A/B data register (PORTQA/B) 5-36  
    PORTQA data direction register (DDRQA) 5-37  
    status register 0 (QASR0) 5-42  
    status register 1 (QASR1) 5-44  
    successive approximation register (SAR) 5-14  
QADC64INT (QADC64 interrupt register) 5-36  
QADC64MCR (QADC64 module configuration register) 5-35  
QASR0 (QADC64 status register 0) 5-43, 5-44  
QILR (QSMCM interrupt level register) 6-7  
QIVR (QSMCM interrupt vector register) 6-8  
QSCI1CR (QSCI1 control register) 6-57  
QSCI1SR (QSCI1 status register) 6-58  
QSMCM  
    configuration register (QMCR) 6-6  
    interrupt level registers (QILR, QIVR) 6-7  
    port QS data register (PORTQS) 6-10  
    PORTQS data direction register (DDRQS) 6-12  
    PORTQS pin assignment register (PQSPAR) 6-10  
    QSCI1 control register (QSCI1CR) 6-57  
    QSCI1 status register (QSCI1SR) 6-58  
    QSPI command RAM (CRx) 6-22  
    QSPI control register 0 (SPCR0) 6-16  
    QSPI control register 1 (SPCR1) 6-18  
    QSPI control register 2 (SPCR2) 6-18  
    QSPI control register 3 (SPCR3) 6-19  
    QSPI registers 6-15  
    QSPI status register (SPSR) 6-20  
    queued SCI1 status and control registers 6-57  
    SCI control register 0 (SCCxR0) 6-45  
    SCI control register 1 (SCCxR1) 6-45  
    SCI data register (SCxDR) 6-49



SCI registers 6-44  
SCI status register (SCxSR) 6-47  
test register (QTEST) 6-7  
QSMCMCCR (QSMCM module configuration register) 6-7  
QSPI\_IL (QSMCM queued SPI interrupt level register) 6-8

–R–

RAMMCR (SRAM module configuration register) 11-4  
RAMMCR RAMBAH, RAMBAL (SRAM array base address register) 11-5  
RJURR (right justified, unsigned result register) 5-51  
ROM  
    module configuration register (ROMMCR) 12-3  
ROMBAH (ROM base address high register) 12-5  
ROMBAL (ROM base address low register) 12-5  
ROMBS0–ROMBS3  
    bootstrap information words (ROMBS0–ROMBS3) 12-7  
ROMBS0–ROMBS3 (ROM bootstrap information words) 12-7, 12-8  
ROMMCR (ROM module configuration registers) 12-4  
RSR  
    reset status register (RSR) 4-56  
RSR (SCIM2 reset status register) 4-56  
RXECTR (receive error counter) 7-34  
RXGMSKHI (receive global mask register high) 7-30

–S–

SASM  
    data register A (SDATA) 13-22  
    data register B (SDATB) 13-23  
    status/interrupt control register A (SICA) 13-20  
    status/interrupt control register B (SICB) 13-22  
SCCxR0 (QSMCM SCI control register 0) 6-45  
SCCxR1 (QSMCM SCI control register 1) 6-46  
SCDR (QSMCM SCI data register) 6-49  
SCIM  
    clock synthesizer control register (SYNCR) 4-14  
SCIM2  
    chip-select base address registers (CSBARBT) 4-78  
    module configuration register (SCIMMCR) 4-2  
    periodic interrupt control register (PICR) 4-30  
    periodic interrupt timer register (PITR) 4-31  
    port C data register (PORTC) 4-78  
    port E data direction registers (DDRAB, DDRE) 4-89  
    port E pin assignment register (PEPAR) 4-89  
    port F data direction register (DDRF) 4-92  
    port F edge-detect flag register (PORTFE) 4-93  
    port F edge-detect interrupt level register (PFLVR) 4-93  
    port F edge-detect interrupt vector register (PFIVR) 4-93  
    port F pin assignment register (PFPAR) 4-92  
    port G,H data direction registers ((DDRG, DDRH) 4-94  
    port G,H data registers (PORTG, PORTH) 4-94  
    software watchdog service register (SWSR) 4-28  
    system protection control register (SYPCR) 4-24  
SCIMMCR (SCIM2 module configuration register) 4-2  
SCxSR (QSMCM SCIx status register) 6-47  
SDATA (SASM data register A) 13-22  
SDATB (SASM data register B) 13-23  
SICA (SASM status/interrupt control register A) 13-20  
SICB (SASM status/interrupt control register B) 13-23  
SIGHI



ROM signature register (SIGHI) 12-6  
SIGHI (ROM signature high register) 12-6  
SIGLO  
ROM signature register (SIGLO) 12-6  
SIGLO (ROM signature low register) 12-6  
SPCR0 (QSPI control register 0) 6-16  
SPCR1 (QSPI control register 1) 6-18  
SPCR2 (QSPI control register 2) 6-19  
SPCR3 (QSPI control register 3) 6-19  
SPSR (QSPI status register) 6-20  
SWSR (SWSR software watchdog service register) 4-28  
SYNCR (SYNCR clock synthesizer control register, external clock mode) 4-15  
SYNCR (SYNCR clock synthesizer control register, fast reference model) 4-14  
SYNCR (SYNCR clock synthesizer control register, slow reference model) 4-14  
SYPCR (SCIM2 system protection control register) 4-24

–T–

TICR (TPU3 interrupt configuration register) 8-14  
TIMER (free running timer register) 7-29  
TouCAN  
control register 0 (CANCTRL0) 7-26  
control register 1 (CANCTRL1) 7-27  
control register 2 (CANCTRL2) 7-29  
error and status register (ESTAT) 7-31  
interrupt configuration register (CANICR) 7-25  
interrupt flag register (IFLAG) 7-33  
interrupt mask register (IMASK) 7-33  
module configuration register (CANMCR) 7-23  
prescaler divide register (PRES DIV) 7-28  
receive buffer 14 mask registers 7-30  
receive buffer 15 mask registers 7-31  
receive global mask registers (RXGMSKHI) 7-30  
receive mask registers 7-7  
TPU3  
channel function select registers (CFSRx) 8-15  
channel interrupt enable register (CIER) 8-14  
channel interrupt status register (CISR) 8-18  
channel priority registers (CPRx) 8-17  
decoded channel number register (DCNR) 8-18  
development support control register (DSCR) 8-12  
development support status register (DSSR) 8-13  
host sequence registers (HSQRx) 8-15  
host service request registers (HSSRx) 8-16  
interrupt configuration register (TICR) 8-14  
link register (LR) 8-18  
module configuration register (TPUMCR) 8-10  
module configuration register 2 (TPUMCR2) 8-18  
module configuration register 3 (TPUMCR3) 8-20  
service grant latch register (SGLR) 8-18  
test configuration register (TCR) 8-12  
test registers (ISDR, ISCR) 8-20  
TPUMCR (TPU3 module configuration register) 8-10  
TPUMCR2 (TPU3 module configuration register 2) 8-18  
TPUMCR3 (TPU3 module configuration register 3) 8-20

