



## APPENDIX A ELECTRICAL CHARACTERISTICS

This appendix contains electrical specification tables and reference timing diagrams for MC68336 and MC68376 microcontroller units.

**Table A-1 Maximum Ratings**

Num	Rating	Symbol	Value	Unit
1	Supply Voltage <sup>1, 2, 7</sup>	$V_{DD}$	– 0.3 to + 6.5	V
2	Input Voltage <sup>11, 22, 3, 55, 77</sup>	$V_{in}$	– 0.3 to + 6.5	V
3	Instantaneous Maximum Current Single pin limit (applies to all pins) <sup>11, 55, 66, 77</sup>	$I_D$	25	mA
4	Operating Maximum Current Digital Input Disruptive Current <sup>4, 5, 6, 7, 8</sup> $V_{NEGCLAMP} \cong -0.3 \text{ V}$ $V_{POSCLAMP} \cong V_{DD} + 0.3$	$I_{ID}$	– 500 to 500	$\mu\text{A}$
5	Operating Temperature Range MC68336/376 “C” Suffix MC68336/376 “V” Suffix MC68336/376 “M” Suffix	$T_A$	$T_L$ to $T_H$ – 40 to 85 – 40 to 105 – 40 to 125	°C
6	Storage Temperature Range	$T_{stg}$	– 55 to 150	°C

**NOTES:**

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. All pins except TSTME/TSC.
4. All functional non-supply pins are internally clamped to  $V_{SS}$ . All functional pins except EXTAL and XFC are internally clamped to  $V_{DD}$ . Does not include QADC pins (refer to [Table A-11](#)).
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions.
7. This parameter is periodically sampled rather than 100% tested.
8. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.



**Table A-2 Typical Ratings**

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	$V_{DD}$	5.0	V
2	Operating Temperature	$T_A$	25	°C
3	$V_{DD}$ Supply Current RUN LPSTOP, VCO off LPSTOP, External clock, maxi $f_{sys}$	$I_{DD}$	113 125 3.75	mA $\mu$ A mA
4	Clock Synthesizer Operating Voltage	$V_{DDSYN}$	5.0	V
5	$V_{DDSYN}$ Supply Current VCO on, maximum $f_{sys}$ External Clock, maximum $f_{sys}$ LPSTOP, VCO off $V_{DD}$ powered down	$I_{DDSYN}$	1.0 5.0 100 50	mA mA $\mu$ A $\mu$ A
6	RAM Standby Voltage	$V_{SB}$	3.0	V
7	RAM Standby Current Normal RAM operation Standby operation	$I_{SB}$	7.0 40	$\mu$ A $\mu$ A
8	Power Dissipation	$P_D$	570	mW

**Table A-3 Thermal Characteristics**

Num	Rating	Symbol	Value	Unit
1	Thermal Resistance Plastic 160-Pin Surface Mount	$\theta_{JA}$	37	°C/W

The average chip-junction temperature ( $T_J$ ) in C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

$T_A$  = Ambient Temperature, °C

$\theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D$  =  $P_{INT} + P_{I/O}$

$P_{INT}$  =  $I_{DD} \times V_{DD}$ , Watts — Chip Internal Power

$P_{I/O}$  = Power Dissipation on Input and Output Pins — User Determined

For most applications  $P_{I/O} < P_{INT}$  and can be neglected. An approximate relationship between  $R_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273^\circ\text{C}) + \theta_{JA} \times P_D \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring  $R_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .



**Table A-4 Clock Control Timing**

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ , 4.194 MHz reference)

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range	$f_{ref}$	4.194	5.243	MHz
2	System Frequency <sup>1</sup> On-Chip PLL System Frequency External Clock Operation	$f_{sys}$	dc $f_{ref}/32$ dc	20.97 20.97 20.97	MHz
3	PLL Lock Time <sup>2, 3, 4, 5</sup>	$t_{pll}$	—	20	ms
4	VCO Frequency <sup>6</sup>	$f_{VCO}$	—	2 ( $f_{sys} \text{ max}$ )	MHz
5	Limp Mode Clock Frequency SYNCR X bit = 0 SYNCR X bit = 1	$f_{limp}$	— —	$f_{sys} \text{ max}/2$ $f_{sys} \text{ max}$	MHz
6	CLKOUT Jitter <sup>2, 3, 4, 7</sup> Short term (5 $\mu\text{s}$ interval) Long term (500 $\mu\text{s}$ interval)	$J_{clk}$	-0.625 -0.0625	-0.625 -0.0625	%

**NOTES:**

1. All internal registers retain data at 0 Hz.
2. This parameter is periodically sampled rather than 100% tested.
3. Assumes that a low-leakage external filter network is used to condition clock synthesizer input voltage. Total external resistance from the XFC pin due to external leakage must be greater than 15 M $\Omega$  to guarantee this specification. Filter network geometry can vary depending upon operating environment.
4. Proper layout procedures must be followed to achieve specifications.
5. Assumes that stable  $V_{DDSYN}$  is applied, and that the crystal oscillator is stable. Lock time is measured from the time  $V_{DD}$  and  $V_{DDSYN}$  are valid until  $\overline{\text{RESET}}$  is released. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
6. Internal VCO frequency ( $f_{VCO}$ ) is determined by SYNCR W and Y bit values. The SYNCR X bit controls a divide-by-two circuit that is not in the synthesizer feedback loop. When X = 0, the divider is enabled, and  $f_{sys} = f_{VCO} \div 4$ . When X = 1, the divider is disabled, and  $f_{sys} = f_{VCO} \div 2$ . X must equal one when operating at maximum specified  $f_{sys}$ .
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{sys}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via  $V_{DDSYN}$  and  $V_{SS}$  and variation in crystal oscillator frequency increase the  $J_{clk}$  percentage for a given interval. When jitter is a critical constraint on control system operation, this parameter should be measured during functional testing of the final system.



**Table A-5 DC Characteristics**

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ )

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	$V_{IH}$	$0.7 (V_{DD})$	$V_{DD} + 0.3$	V
2	Input Low Voltage	$V_{IL}$	$V_{SS} - 0.3$	$0.2 (V_{DD})$	V
3	Input Hysteresis <sup>1</sup>	$V_{HYS}$	0.5	—	V
4	Input Leakage Current <sup>2</sup> $V_{in} = V_{DD}$ or $V_{SS}$ Input-only pins	$I_{in}$	-2.5	2.5	$\mu\text{A}$
5	High Impedance (Off-State) Leakage Current <sup>22</sup> $V_{in} = V_{DD}$ or $V_{SS}$ All input/output and output pins	$I_{OZ}$	-2.5	2.5	$\mu\text{A}$
6	CMOS Output High Voltage <sup>22, 3</sup> $I_{OH} = -10.0 \mu\text{A}$ Group 1, 2, 4 input/output and all output pins	$V_{OH}$	$V_{DD} - 0.2$	—	V
7	CMOS Output Low Voltage <sup>22</sup> $I_{OL} = 10.0 \mu\text{A}$ Group 1, 2, 4 input/output and all output pins	$V_{OL}$	—	0.2	V
8	Output High Voltage <sup>22, 33</sup> $I_{OH} = -0.8 \text{ mA}$ Group 1, 2, 4 input/output and all output pins	$V_{OH}$	$V_{DD} - 0.8$	—	V
9	Output Low Voltage <sup>22</sup> $I_{OL} = 1.6 \text{ mA}$ Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, $\overline{IP}$ $\overline{IPE}$ $I_{OL} = 5.3 \text{ mA}$ Group 2 and Group 4 I/O Pins, $\overline{CSBOOT}$ , $\overline{BG/CS}$ $I_{OL} = 12 \text{ mA}$ Group 3	$V_{OL}$	— — —	0.4 0.4 0.4	V
10	Three State Control Input High Voltage	$V_{IHTSC}$	$1.6 (V_{DD})$	9.1	V
11	Data Bus Mode Select Pull-up Current <sup>4</sup> $V_{in} = V_{IL}$ DATA[15:0] $V_{in} = V_{IH}$ DATA[15:0]	$I_{MSP}$	— -15	-120 —	$\mu\text{A}$
12A	MC68336 $V_{DD}$ Supply Current <sup>5</sup> RUN <sup>6</sup> RUN, TPU emulation mode LPSTOP, 4.194 MHz crystal, VCO Off (STSIM = 0) LPSTOP (External clock input frequency = maximum $f_{sys}$ )	$I_{DD}$ $I_{DD}$ $S_{IDD}$ $S_{IDD}$	— — — —	140 150 3 7	mA mA mA mA
12B	MC68376 $V_{DD}$ Supply Current <sup>5</sup> RUN <sup>6</sup> RUN, TPU emulation mode LPSTOP, 4.194 MHz crystal, VCO Off (STSIM = 0) LPSTOP (External clock input frequency = maximum $f_{sys}$ )	$I_{DD}$ $I_{DD}$ $S_{IDD}$ $S_{IDD}$	— — — —	150 160 3 7	mA mA mA mA
13	Clock Synthesizer Operating Voltage	$V_{DDSYN}$	4.75	5.25	V
14	$V_{DDSYN}$ Supply Current <sup>55</sup> 4.194 MHz crystal, VCO on, maximum $f_{sys}$ External Clock, maximum $f_{sys}$ LPSTOP, 4.194 MHz crystal, VCO off (STSIM = 0) 4.194 MHz crystal, $V_{DD}$ powered down	$I_{DDSYN}$ $I_{DDSYN}$ $S_{IDDSYN}$ $I_{IDDSYN}$	— — — —	3 5 3 3	mA mA mA mA

# Table A-5 DC Characteristics (Continued)

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ )



Num	Characteristic	Symbol	Min	Max	Unit
15	RAM Standby Voltage <sup>7</sup> Specified $V_{DD}$ applied $V_{DD} = V_{SS}$	$V_{SB}$	0.0 3.0	5.25 5.25	V
16	RAM Standby Current <sup>55, 77, 8</sup> Normal RAM operation $V_{DD} > V_{SB} - 0.5 \text{ V}$ Transient condition $V_{SB} - 0.5 \text{ V} \geq V_{DD} \geq V_{SS} + 0.5 \text{ V}$ Standby operation $V_{DD} < V_{SS} + 0.5 \text{ V}$	$I_{SB}$	— — —	10 3 100	$\mu\text{A}$ mA $\mu\text{A}$
17A	MC68336 Power Dissipation <sup>9</sup>	$P_D$	—	756	mW
17B	MC68376 Power Dissipation <sup>9</sup>	$P_D$	—	809	mW
18	Input Capacitance <sup>22, 10</sup> All input-only pins All input/output pins	$C_{in}$	— —	10 20	pF
19	Load Capacitance <sup>22</sup> Group 1 I/O Pins and CLKOUT, FREEZE/QUOT, IPIPE Group 2 I/O Pins and CSBOOT, BG/CS Group 3 I/O pins Group 4 I/O pins	$C_L$	— — — —	90 100 130 200	pF

## NOTES:

### 1. Applies to :

Port E[7:4] — SIZ[1:0],  $\overline{AS}$ ,  $\overline{DS}$   
Port F[7:0] —  $\overline{IRQ}$ [7:1], MODCLK  
Port QS[7:0] — TXD, PCS[3:1], PCS0/ $\overline{SS}$ , SCK, MOSI, MISO  
TPUCH[15:0], T2CLK, CPWM[8:5], CTD[4:3], CTD[10:9], CTM2C  
BKPT/DSCLK,  $\overline{IFETCH}$ ,  $\overline{RESET}$ , RXD,  $\overline{TSTME/TSC}$   
EXTAL (when PLL enabled)

### 2. Input-Only Pins: EXTAL, $\overline{TSTME/TSC}$ , $\overline{BKPT}$ , PAI, T2CLK, RXD, CTM2C

Output-Only Pins: CSBOOT, BG/CS, CLKOUT, FREEZE/QUOT, IPIPE

Input/Output Pins:

Group 1: DATA[15:0],  $\overline{IFETCH}$ , TPUCH[15:0], CPWM[8:5], CTD[4:3], CTD[10:9]  
Group 2: Port C[6:0] — ADDR[22:19]/CS[9:6], FC[2:0]/CS[5:3]  
Port E[7:0] — SIZ[1:0],  $\overline{AS}$ ,  $\overline{DS}$ , AVEC, RMC, DSACK[1:0]  
Port F[7:0] —  $\overline{IRQ}$ [7:1], MODCLK  
Port QS[7:3] — TXD, PCS[3:1], PCS0/ $\overline{SS}$   
ADDR23/ $\overline{CS}$ 10/ECLK, ADDR[18:0], R/W,  $\overline{BERR}$ ,  $\overline{BR/CS}$ 0,  $\overline{BGACK/CS}$ 2  
Group 3:  $\overline{HALT}$ ,  $\overline{RESET}$   
Group 4: MISO, MOSI, SCK

Pin groups do not include QADC pins. See **Tables A-11 through A-14** for information concerning the QADC.

### 3. Does not apply to $\overline{HALT}$ and $\overline{RESET}$ because they are open drain pins. Does not apply to port QS[7:0] (TXD, PCS[3:1], PCS0/ $\overline{SS}$ , SCK, MOSI, MISO) in wired-OR mode.

### 4. Use of an active pulldown device is recommended.

### 5. Total operating current is the sum of the appropriate $I_{DD}$ , $I_{DDSYN}$ , and $I_{SB}$ values. $I_{DD}$ values include supply currents for device modules powered by $V_{DDE}$ and $V_{DDI}$ pins.

### 6. Current measured at maximum system clock frequency, all modules active.

### 7. The SRAM module will not switch into standby mode as long as $V_{SB}$ does not exceed $V_{DD}$ by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.

### 8. When $V_{DD}$ is transitioning during power-up or power down sequence, and $V_{SB}$ is applied, current flows between the $V_{STBY}$ and $V_{DD}$ pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the $V_{DD}$ and $V_{STBY}$ pins can contribute to this condition.

### 9. Power dissipation measured at system clock frequency, all modules active. Power dissipation can be calculated using the following expression:

$$P_D = \text{Maximum } V_{DD} (\text{Run } I_{DD} + I_{DDSYN} + I_{SB}) + \text{Maximum } V_{DDA} (I_{DDA})$$

### 10. This parameter is periodically sampled rather than 100% tested.



**Table A-6 AC Timing**

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )<sup>1</sup>

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation <sup>2</sup>	$f_{\text{sys}}$	—	20.97	MHz
1	Clock Period	$t_{\text{cyc}}$	47.7	—	ns
1A	ECLK Period	$t_{\text{Ecyc}}$	381	—	ns
1B	External Clock Input Period <sup>3</sup>	$t_{\text{Xcyc}}$	47.7	—	ns
2, 3	Clock Pulse Width	$t_{\text{CW}}$	18.8	—	ns
2A, 3A	ECLK Pulse Width	$t_{\text{ECW}}$	183	—	ns
2B, 3B	External Clock Input High/Low Time <sup>3</sup>	$t_{\text{XCHL}}$	23.8	—	ns
3, 4	Clock Rise and Fall Time	$t_{\text{Crf}}$	—	5	ns
4A, 5A	Rise and Fall Time — All Outputs except CLKOUT	$t_{\text{rf}}$	—	8	ns
4B, 5B	External Clock Rise and Fall Time <sup>4</sup>	$t_{\text{XCrf}}$	—	5	ns
4	Clock High to Address, FC, SIZE, $\overline{\text{RMC}}$ Valid	$t_{\text{CHAV}}$	0	23	ns
5	Clock High to Address, Data, FC, SIZE, $\overline{\text{RMC}}$ High Impedance	$t_{\text{CHAZx}}$	0	47	ns
6	Clock High to Address, FC, SIZE, $\overline{\text{RMC}}$ Invalid <sup>5</sup>	$t_{\text{CHAZn}}$	0	—	ns
7	Clock Low to $\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Asserted	$t_{\text{CLSA}}$	0	23	ns
8A	$\overline{\text{AS}}$ to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ Asserted (Read) <sup>6</sup>	$t_{\text{STSA}}$	–10	10	ns
8C	Clock Low to $\overline{\text{IFETCH}}$ , $\overline{\text{IPIPE}}$ Asserted	$t_{\text{CLIA}}$	2	22	ns
11	Address, FC, SIZE, $\overline{\text{RMC}}$ Valid to $\overline{\text{AS}}$ , $\overline{\text{CS}}$ Asserted	$t_{\text{AVSA}}$	10	—	ns
12	Clock Low to $\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Negated	$t_{\text{CLSN}}$	2	23	ns
12A	Clock Low to $\overline{\text{IFETCH}}$ , $\overline{\text{IPIPE}}$ Negated	$t_{\text{CLIN}}$	2	22	ns
13	$\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Negated to Address, FC, SIZE Invalid (Address Hold)	$t_{\text{SNAI}}$	10	—	ns
14	$\overline{\text{AS}}$ , $\overline{\text{CS}}$ Width Asserted	$t_{\text{SWA}}$	80	—	ns
14A	$\overline{\text{DS}}$ , $\overline{\text{CS}}$ Width Asserted (Write)	$t_{\text{SWAW}}$	36	—	ns
14B	$\overline{\text{AS}}$ , $\overline{\text{CS}}$ Width Asserted (Fast Write Cycle)	$t_{\text{SWDW}}$	32	—	ns
15	$\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Width Negated <sup>7</sup>	$t_{\text{SN}}$	32	—	ns
16	Clock High to $\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\text{R}/\overline{\text{W}}$ High Impedance	$t_{\text{CHSZ}}$	—	47	ns
17	$\overline{\text{AS}}$ , $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Negated to $\text{R}/\overline{\text{W}}$ Negated	$t_{\text{SNRN}}$	10	—	ns
18	Clock High to $\text{R}/\overline{\text{W}}$ High	$t_{\text{CHRH}}$	0	23	ns
20	Clock High to $\text{R}/\overline{\text{W}}$ Low	$t_{\text{CHRL}}$	0	23	ns
21	$\text{R}/\overline{\text{W}}$ Asserted to $\overline{\text{AS}}$ , $\overline{\text{CS}}$ Asserted	$t_{\text{RAAA}}$	10	—	ns
22	$\text{R}/\overline{\text{W}}$ Low to $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Asserted (Write)	$t_{\text{RASA}}$	54	—	ns
23	Clock High to Data Out Valid	$t_{\text{CHDO}}$	—	23	ns
24	Data Out Valid to Negating Edge of $\overline{\text{AS}}$ , $\overline{\text{CS}}$	$t_{\text{DVASN}}$	10	—	ns
25	$\overline{\text{DS}}$ , $\overline{\text{CS}}$ Negated to Data Out Invalid (Data Out Hold)	$t_{\text{SNDOI}}$	10	—	ns
26	Data Out Valid to $\overline{\text{DS}}$ , $\overline{\text{CS}}$ Asserted (Write)	$t_{\text{DVSA}}$	10	—	ns
27	Data In Valid to Clock Low (Data Setup) <sup>5</sup>	$t_{\text{DICL}}$	5	—	ns
27A	Late $\overline{\text{BERR}}$ , $\overline{\text{HALT}}$ Asserted to Clock Low (Setup Time)	$t_{\text{BELCL}}$	15	—	ns
28	$\overline{\text{AS}}$ , $\overline{\text{DS}}$ Negated to $\overline{\text{DSACK}}[1:0]$ , $\overline{\text{BERR}}$ , $\overline{\text{HALT}}$ , $\overline{\text{AVEC}}$ Negated	$t_{\text{SNDN}}$	0	60	ns
29	$\overline{\text{DS}}$ , $\overline{\text{CS}}$ Negated to Data In Invalid (Data In Hold) <sup>8</sup>	$t_{\text{SNDI}}$	0	—	ns

# Table A-6 AC Timing (Continued)

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )<sup>1</sup>

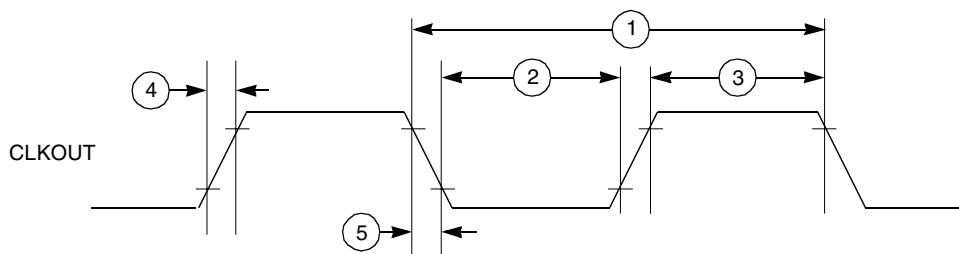


Num	Characteristic	Symbol	Min	Max	Unit
29A	$\overline{DS}$ , $\overline{CS}$ Negated to Data In High Impedance <sup>88, 9</sup>	$t_{SHDI}$	—	48	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold) <sup>88</sup>	$t_{CLDI}$	10	—	ns
30A	CLKOUT Low to Data In High Impedance <sup>88</sup>	$t_{CLDH}$	—	72	ns
31	$\overline{DSACK}[1:0]$ Asserted to Data In Valid <sup>10</sup>	$t_{DADI}$	—	46	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	$t_{CLBAN}$	—	23	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ( $\overline{RMC}$ Not Asserted) <sup>11</sup>	$t_{BRAGA}$	1	—	$t_{cyc}$
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	$t_{GAGN}$	1	2	$t_{cyc}$
39	$\overline{BG}$ Width Negated	$t_{GH}$	2	—	$t_{cyc}$
39A	$\overline{BG}$ Width Asserted	$t_{GA}$	1	—	$t_{cyc}$
46	$R/\overline{W}$ Width Asserted (Write or Read)	$t_{RWA}$	115	—	ns
46A	$R/\overline{W}$ Width Asserted (Fast Write or Read Cycle)	$t_{RWAS}$	70	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$ , $\overline{BGACK}$ , $\overline{DSACK}[1:0]$ , $\overline{BERR}$ , $\overline{AVEC}$ , $\overline{HALT}$	$t_{AIST}$	5	—	ns
47B	Asynchronous Input Hold Time	$t_{AIHT}$	12	—	ns
48	$\overline{DSACK}[1:0]$ Asserted to $\overline{BERR}$ , $\overline{HALT}$ Asserted <sup>12</sup>	$t_{DABA}$	—	30	ns
53	Data Out Hold from Clock High	$t_{DOCH}$	0	—	ns
54	Clock High to Data Out High Impedance	$t_{CHDH}$	—	23	ns
55	$R/\overline{W}$ Asserted to Data Bus Impedance Change	$t_{RADC}$	32	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	$t_{HRPW}$	512	—	$t_{cyc}$
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	$t_{BNHN}$	0	—	ns
70	Clock Low to Data Bus Driven (Show)	$t_{SCLDD}$	0	23	ns
71	Data Setup Time to Clock Low (Show)	$t_{SCLDS}$	10	—	ns
72	Data Hold from Clock Low (Show)	$t_{SCLDH}$	10	—	ns
73	$\overline{BKPT}$ Input Setup Time	$t_{BKST}$	10	—	ns
74	$\overline{BKPT}$ Input Hold Time	$t_{BKHT}$	10	—	ns
75	Mode Select Setup Time	$t_{MSS}$	20	—	$t_{cyc}$
76	Mode Select Hold Time	$t_{MSH}$	0	—	ns
77	$\overline{RESET}$ Assertion Time <sup>13</sup>	$t_{RSTA}$	4	—	$t_{cyc}$
78	$\overline{RESET}$ Rise Time <sup>14, 15</sup>	$t_{RSTR}$	—	10	$t_{cyc}$

## NOTES:

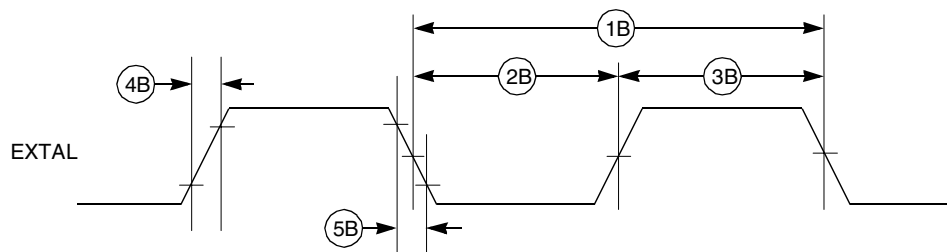
- All AC timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$  levels unless otherwise noted.
- The base configuration of the MC68336/376 requires a 20.97 MHz crystal reference.
- When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable  $t_{xcyc}$  period is reduced when the duty cycle of the external clock signal varies. The relationship between external clock input duty cycle and minimum  $t_{xcyc}$  is expressed:  
Minimum  $t_{xcyc}$  period = minimum  $t_{xchl} / (50\% - \text{external clock input duty cycle tolerance})$ .
- Parameters for an external clock signal applied while the internal PLL is disabled (MODCLK pin held low during reset). Does not pertain to an external VCO reference applied while the PLL is enabled (MODCLK pin held high during reset). When the PLL is enabled, the clock synthesizer detects successive transitions of the reference signal. If transitions occur within the correct clock period, rise/fall times and duty cycle are not critical.
- Address access time =  $(2.5 + WS) t_{cyc} - t_{CHAV} - t_{DIDL}$   
Chip select access time =  $(2 + WS) t_{cyc} - t_{LSA} - t_{DIDL}$   
Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = -1.

6. Specification 9A is the worst-case skew between  $\overline{AS}$  and  $\overline{DS}$  or  $\overline{CS}$ . The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause  $\overline{AS}$  and  $\overline{DS}$  to fall outside the limits shown in specification 9.
7. If multiple chip selects are used,  $\overline{CS}$  width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The  $\overline{CS}$  width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
8. Hold times are specified with respect to  $\overline{DS}$  or  $\overline{CS}$  on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
9. Maximum value is equal to  $(t_{cyc} / 2) + 25$  ns.
10. If the asynchronous setup time (specification 47A) requirements are satisfied, the  $\overline{DSACK}[1:0]$  low to data setup time (specification 31) and  $\overline{DSACK}[1:0]$  low to  $\overline{BERR}$  low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle.  $\overline{BERR}$  must satisfy only the late  $\overline{BERR}$  low to clock low setup time (specification 27A) for the following clock cycle.
11. To ensure coherency during every operand transfer,  $\overline{BG}$  will not be asserted in response to  $\overline{BR}$  until after all cycles of the current operand transfer are complete and RMC is negated.
12. In the absence of  $\overline{DSACK}[1:0]$ ,  $\overline{BERR}$  is an asynchronous input using the asynchronous setup time (specification 47A).
13. After external  $\overline{RESET}$  negation is detected, a short transition period (approximately  $2 t_{cyc}$ ) elapses, then the SIM drives  $\overline{RESET}$  low for  $512 t_{cyc}$ .
14. External assertion of the  $\overline{RESET}$  input can overlap internally-generated resets. To insure that an external reset is recognized in all cases,  $\overline{RESET}$  must be asserted for at least 590 CLKOUT cycles.
15. External logic must pull  $\overline{RESET}$  high during this period in order for normal MCU operation to begin.



68300 CLKOUT TIM

**Figure A-1 CLKOUT Output Timing Diagram**

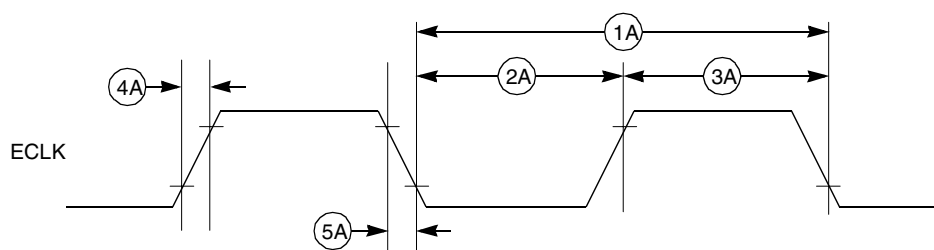


NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70%  $V_{DD}$ .  
PULSE WIDTH SHOWN WITH RESPECT TO 50%  $V_{DD}$ .

68300 EXT CLK INPUT T

**Figure A-2 External Clock Input Timing Diagram**

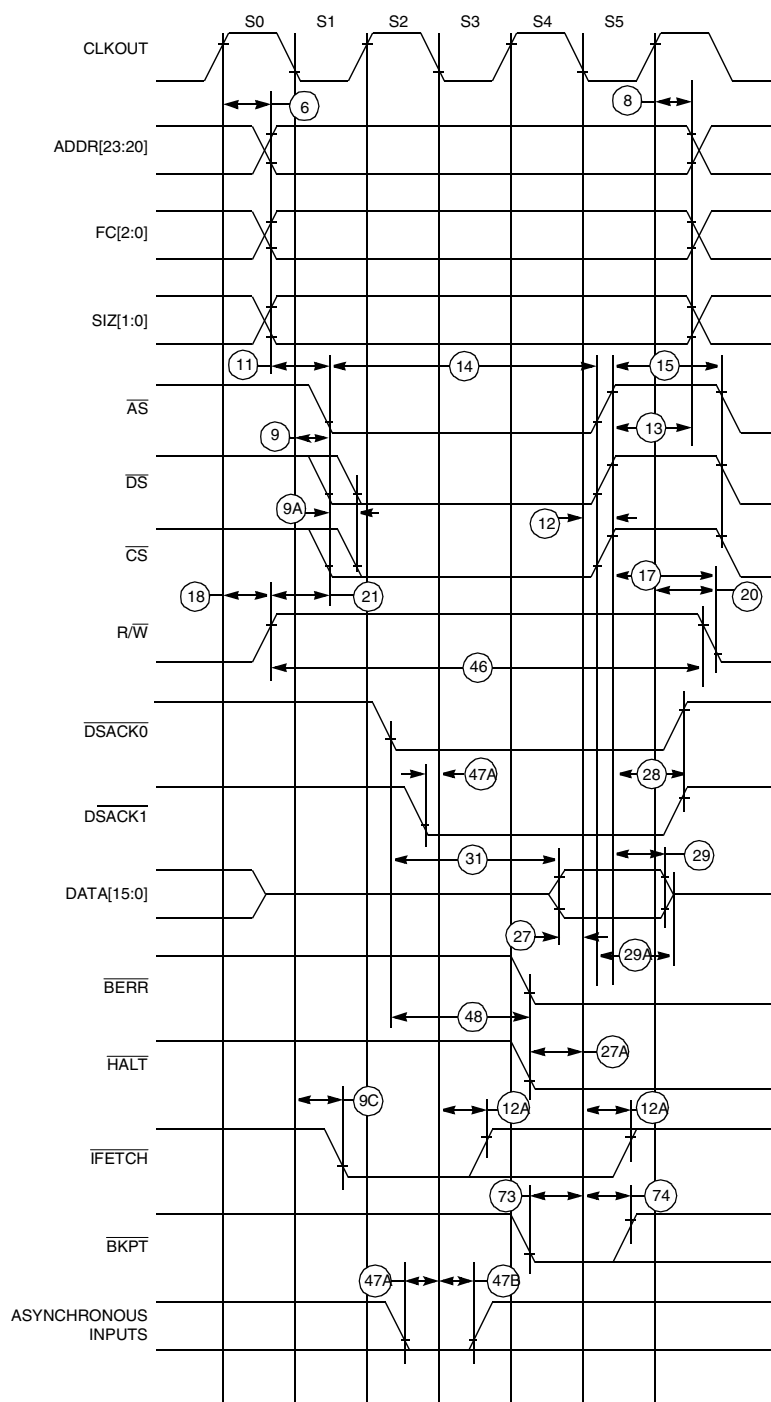




NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70%  $V_{DD}$ .

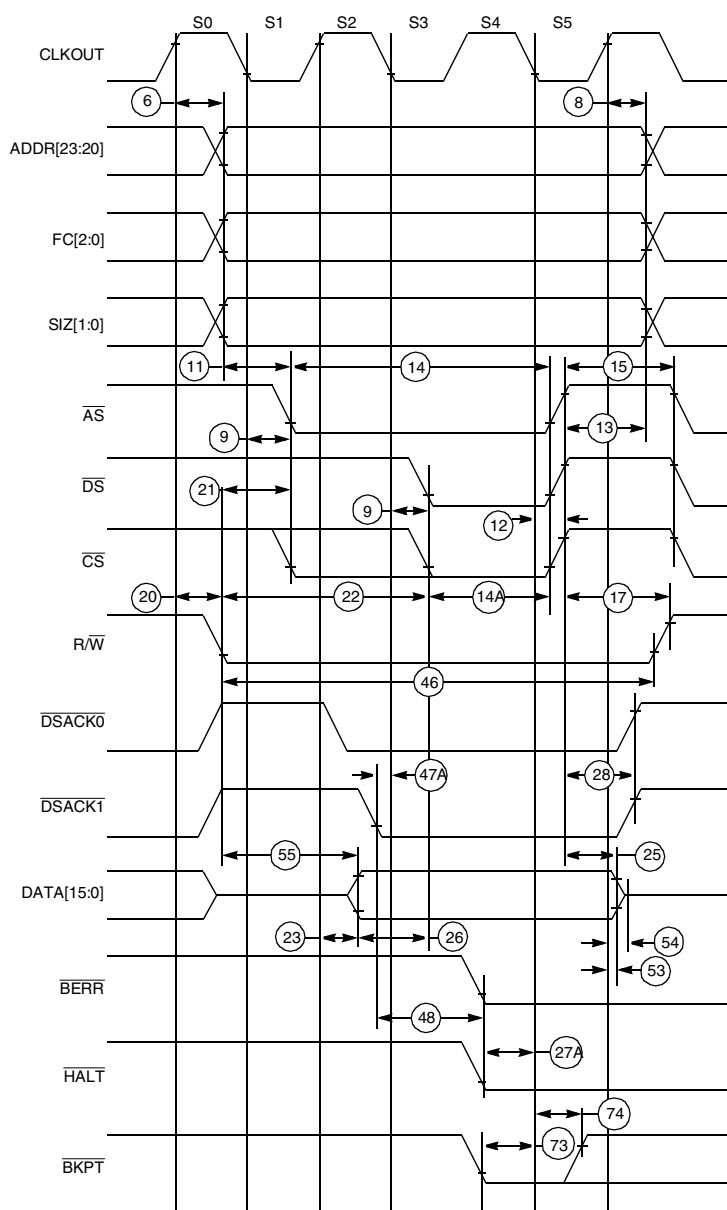
68300 ECLK OUTPUT T1

**Figure A-3 ECLK Output Timing Diagram**



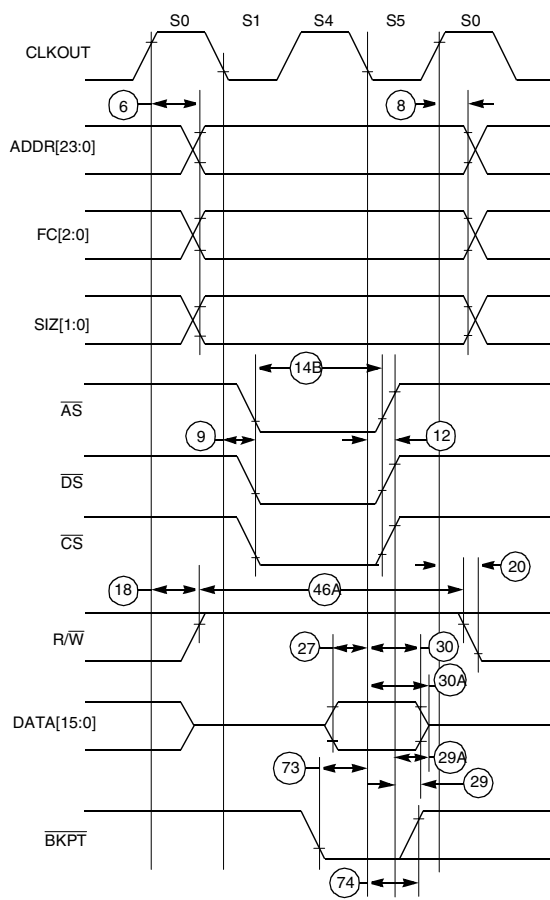
68300 RD CYC TIM

**Figure A-4 Read Cycle Timing Diagram**



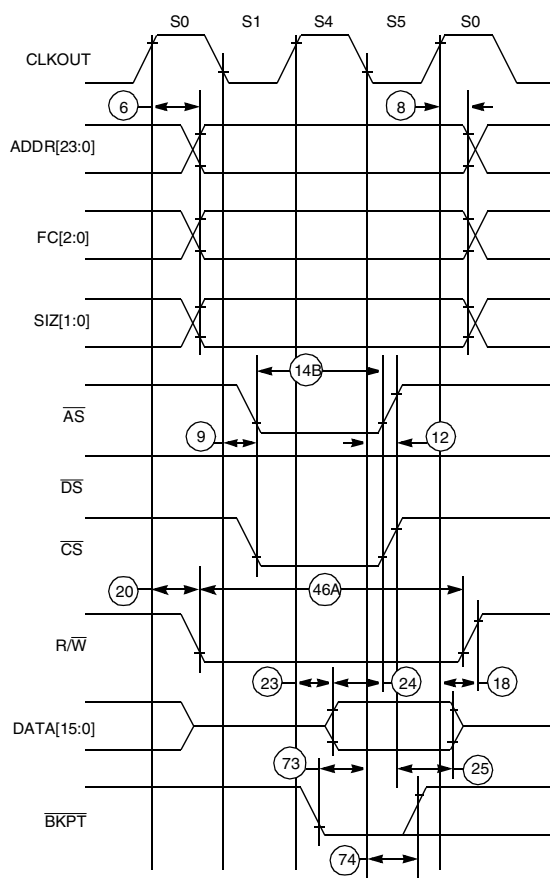
68300 WR CYC TIM

**Figure A-5 Write Cycle Timing Diagram**



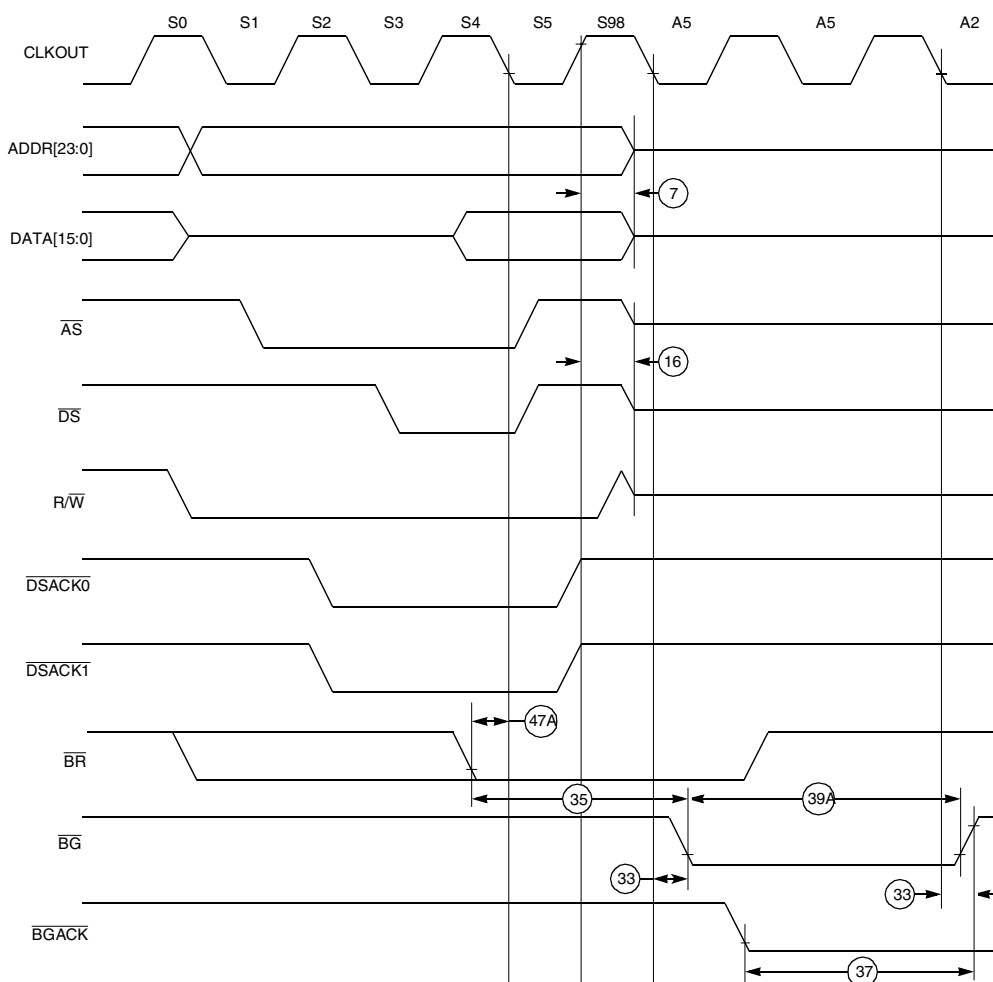
68300 FAST RD CYC TIM

**Figure A-6 Fast Termination Read Cycle Timing Diagram**



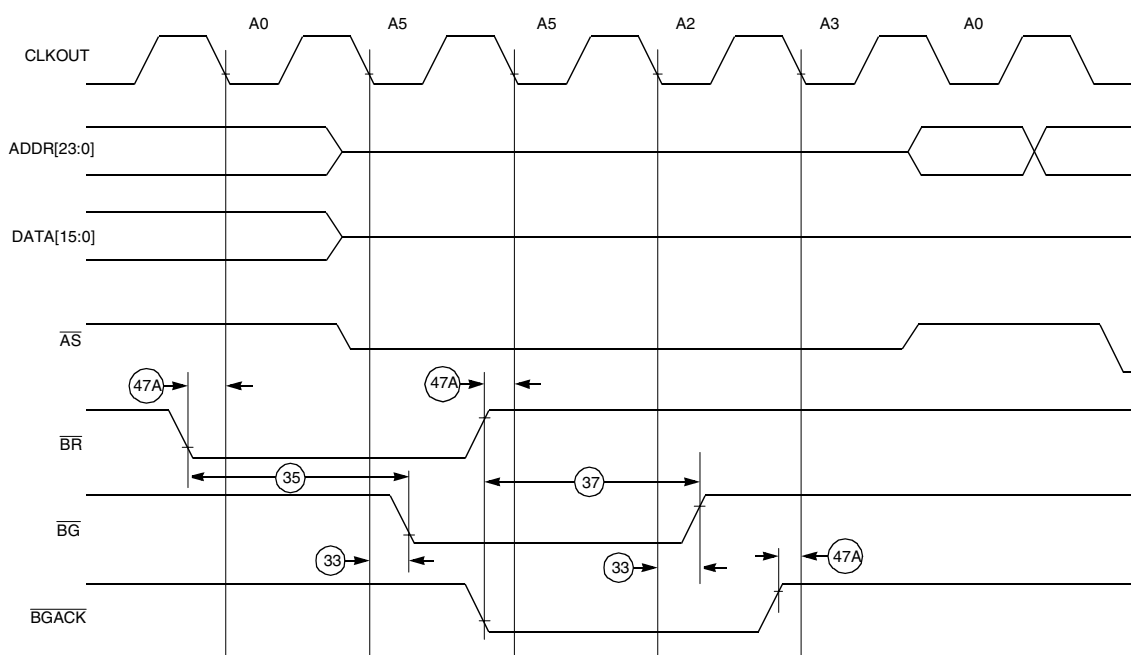
68300 FAST WR CYC TIM

**Figure A-7 Fast Termination Write Cycle Timing Diagram**



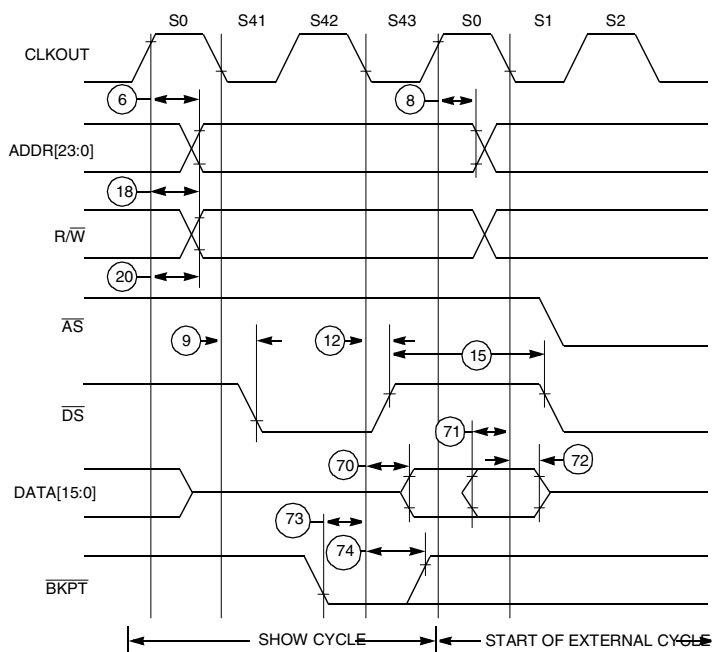
68300 BUS ARB TIM

**Figure A-8 Bus Arbitration Timing Diagram — Active Bus Case**



68300 BUS ARB TIM IDL

**Figure A-9 Bus Arbitration Timing Diagram — Idle Bus Case**

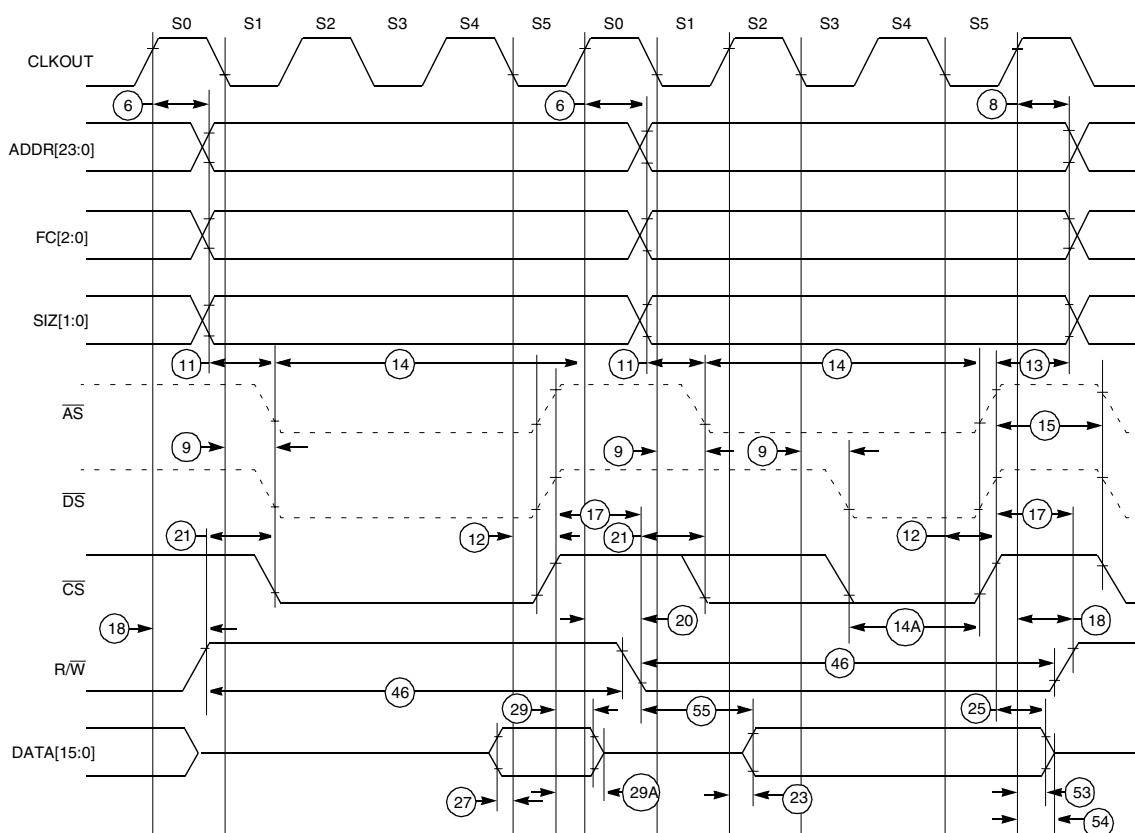


**NOTE:**  
 Show cycles can stretch during clock phase S42 when bus accesses take longer than two cycles due to IMB module wait-state insertion.

68300 SHW CYC TIM

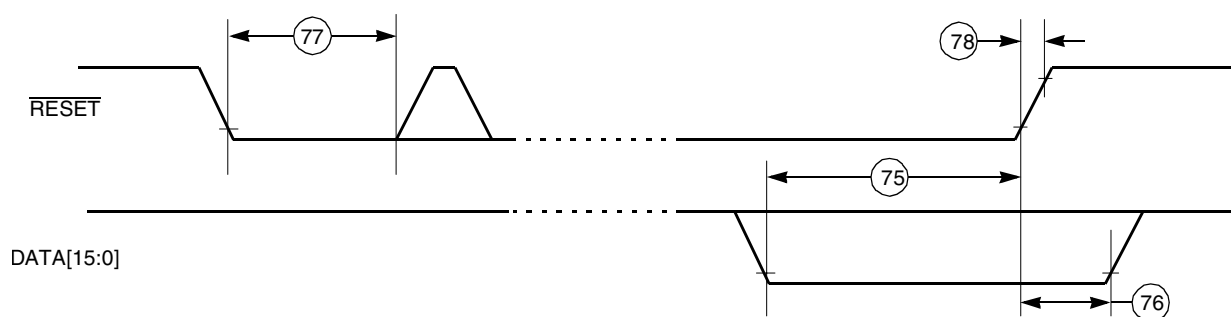
**Figure A-10 Show Cycle Timing Diagram**





68300 CHIP SEL TIM

**Figure A-11 Chip-Select Timing Diagram**



68300 RST/MODE SEL T

**Figure A-12 Reset and Mode Select Timing Diagram**



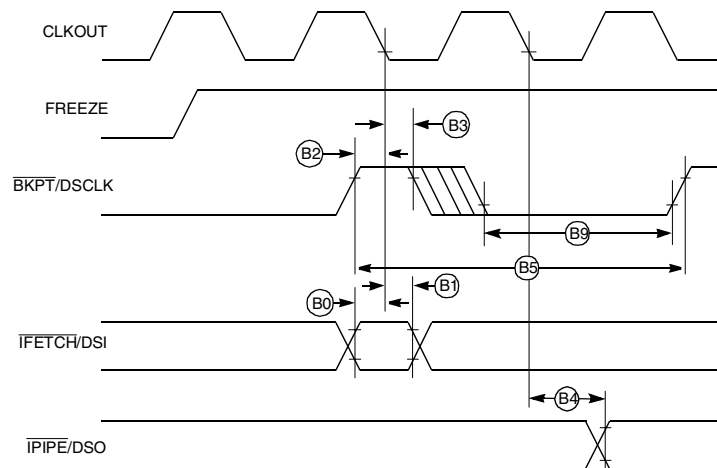
**Table A-7 Background Debug Mode Timing**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )<sup>1</sup>

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	$t_{DSISU}$	15	—	ns
B1	DSI Input Hold Time	$t_{DSIH}$	10	—	ns
B2	DSCLK Setup Time	$t_{DSCSU}$	15	—	ns
B3	DSCLK Hold Time	$t_{DSCCH}$	10	—	ns
B4	DSO Delay Time	$t_{DSOD}$	—	25	ns
B5	DSCLK Cycle Time	$t_{DSCCYC}$	2	—	$t_{cyc}$
B6	CLKOUT Low to FREEZE Asserted/Negated	$t_{FRZAN}$	—	50	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	$t_{IPZ}$	—	TBD	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	$t_{IP}$	—	TBD	ns
B9	DSCLK Low Time	$t_{DSCLO}$	1	—	$t_{cyc}$

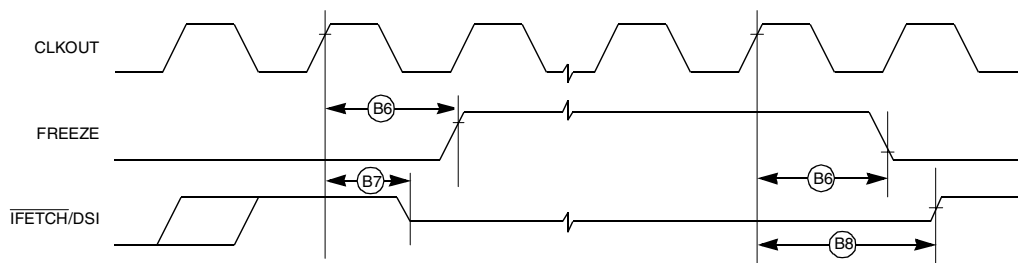
**NOTES:**

1. All AC timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$  levels unless otherwise noted.



68300 BKGD DBM SER COM T

**Figure A-13 Background Debug Mode Timing — Serial Communication**



68300 BDM FRZ TIM

**Figure A-14 Background Debug Mode Timing — Freeze Assertion**



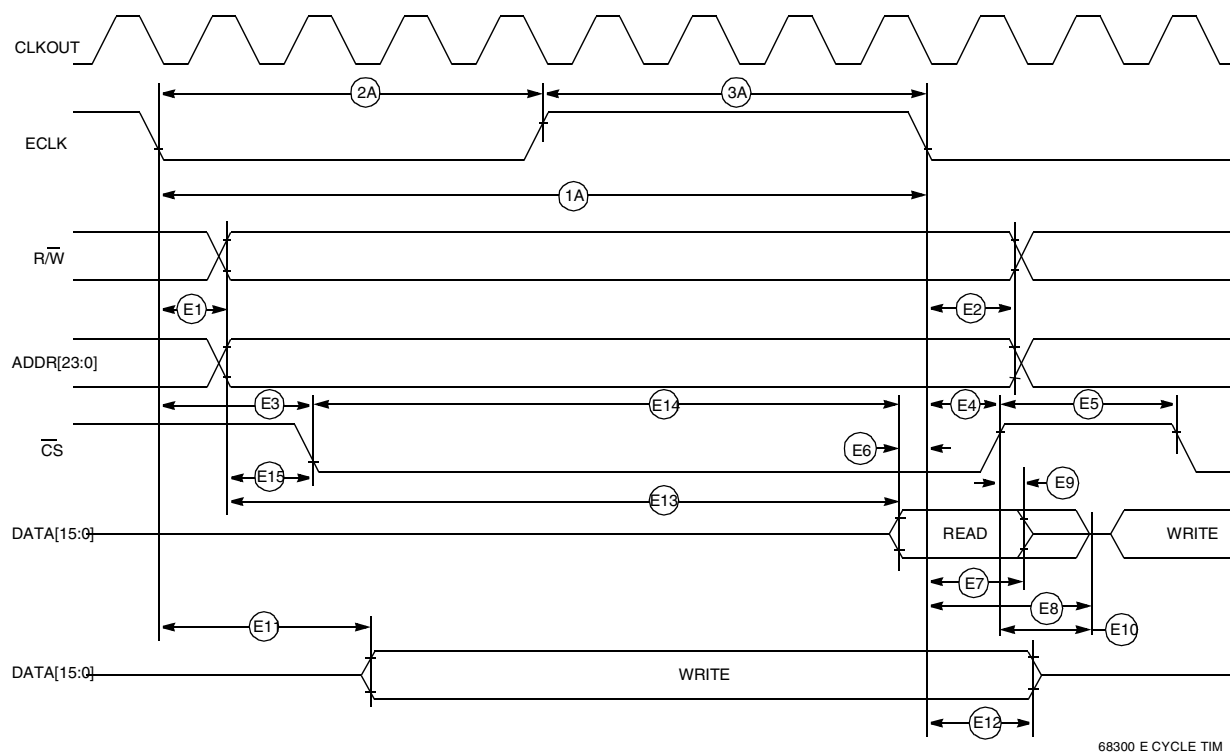
**Table A-8 ECLK Bus Timing**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )<sup>1</sup>

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid <sup>2</sup>	$t_{EAD}$	—	48	ns
E2	ECLK Low to Address Hold	$t_{EAH}$	10	—	ns
E3	ECLK Low to $\overline{CS}$ Valid ( $\overline{CS}$ delay)	$t_{ECSD}$	—	120	ns
E4	ECLK Low to $\overline{CS}$ Hold	$t_{ECSH}$	10	—	ns
E5	$\overline{CS}$ Negated Width	$t_{ECSN}$	25	—	ns
E6	Read Data Setup Time	$t_{EDSR}$	25	—	ns
E7	Read Data Hold Time	$t_{EDHR}$	5	—	ns
E8	ECLK Low to Data High Impedance	$t_{EDHZ}$	—	48	ns
E9	$\overline{CS}$ Negated to Data Hold (Read)	$t_{ECDH}$	0	—	ns
E10	$\overline{CS}$ Negated to Data High Impedance	$t_{ECDZ}$	—	1	$t_{cyc}$
E11	ECLK Low to Data Valid (Write)	$t_{EDDW}$	—	2	$t_{cyc}$
E12	ECLK Low to Data Hold (Write)	$t_{EDHW}$	10	—	ns
E13	Address Access Time (Read) <sup>3</sup>	$t_{EACC}$	308	—	ns
E14	Chip Select Access Time (Read) <sup>4</sup>	$t_{EACS}$	236	—	ns
E15	Address Setup Time	$t_{EAS}$	1/2	—	$t_{cyc}$

**NOTES:**

1. All AC timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$  levels unless otherwise noted.
2. When the previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time =  $t_{EACC} = t_{EAD} + t_{EDSR}$ .
4. Chip select access time =  $t_{EACS} = t_{ECSD} + t_{EDSR}$ .



**Figure A-15 ECLK Timing Diagram**



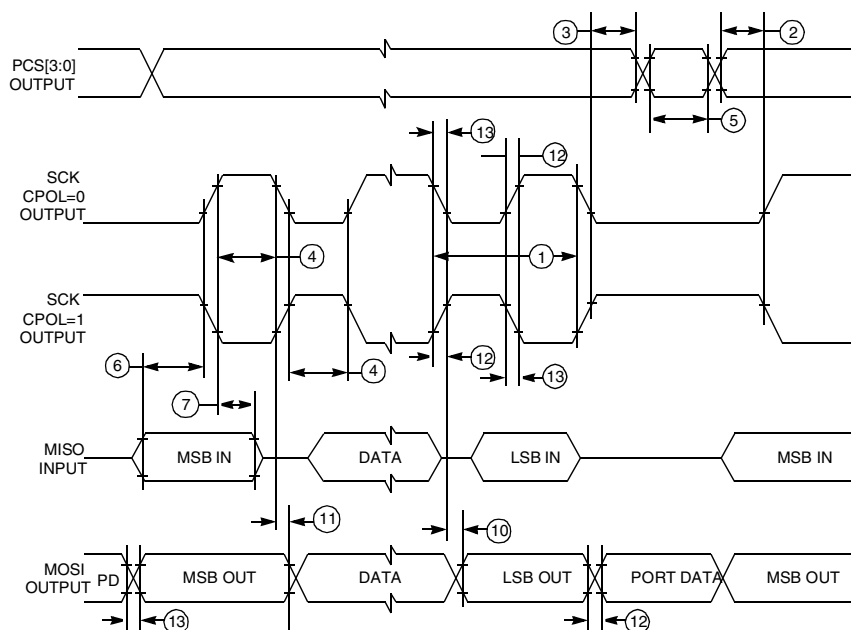
**Table A-9 QSPI Timing**

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$  200 pF load on all QSPI pins)<sup>1</sup>

Num	Function	Symbol	Min	Max	Unit
1	Operating Frequency Master Slave	$f_{QSPI}$	DC DC	1/4 1/4	$f_{sys}$ $f_{sys}$
2	Cycle Time Master Slave	$t_{qcyc}$	4 4	510 —	$t_{cyc}$ $t_{cyc}$
3	Enable Lead Time Master Slave	$t_{lead}$	2 2	128 —	$t_{cyc}$ $t_{cyc}$
4	Enable Lag Time Master Slave	$t_{lag}$	— 2	1/2 —	SCK $t_{cyc}$
5	Clock (SCK) High or Low Time Master Slave <sup>2</sup>	$t_{sw}$	$2 t_{cyc} - 60$ $2 t_{cyc} - n$	$255 t_{cyc}$ —	ns ns
6	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	$t_{td}$	17 13	8192 —	$t_{cyc}$ $t_{cyc}$
7	Data Setup Time (Inputs) Master Slave	$t_{su}$	30 20	— —	ns ns
8	Data Hold Time (Inputs) Master Slave	$t_{hi}$	0 20	— —	ns ns
9	Slave Access Time	$t_a$	—	1	$t_{cyc}$
10	Slave MISO Disable Time	$t_{dis}$	—	2	$t_{cyc}$
11	Data Valid (after SCK Edge) Master Slave	$t_v$	— —	50 50	ns ns
12	Data Hold Time (Outputs) Master Slave	$t_{ho}$	0 0	— —	ns ns
13	Rise Time Input Output	$t_{ri}$ $t_{ro}$	— —	2 30	$\mu s$ ns
14	Fall Time Input Output	$t_{fi}$ $t_{fo}$	— —	2 30	$\mu s$ ns

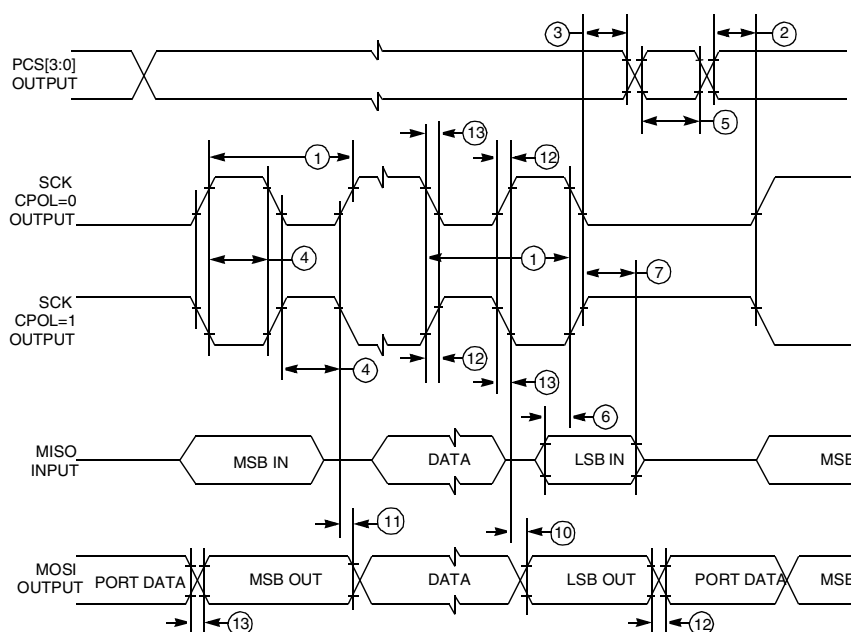
**NOTES:**

1. All AC timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$  levels unless otherwise noted.
2. For high time,  $n$  = External SCK rise time; for low time,  $n$  = External SCK fall time.



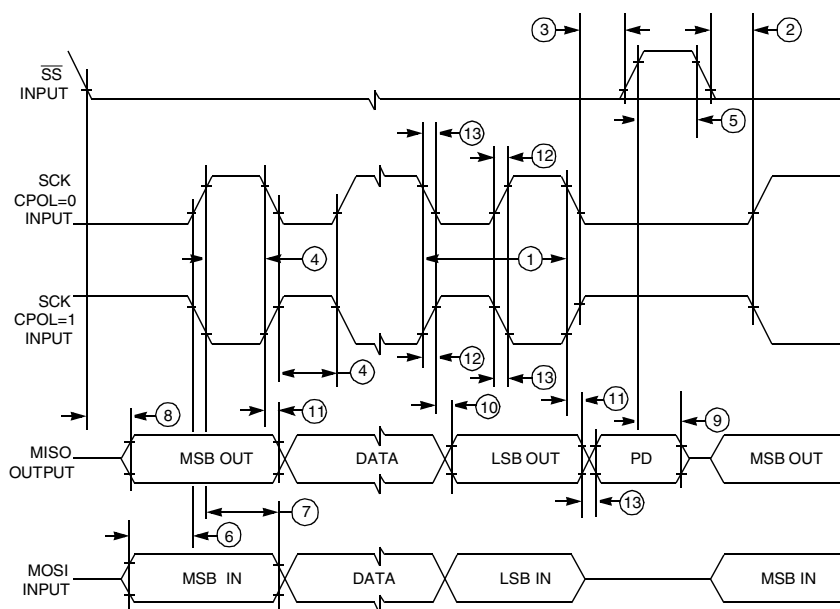
QSPI MAST CPHA0

**Figure A-16 QSPI Timing — Master, CPHA = 0**



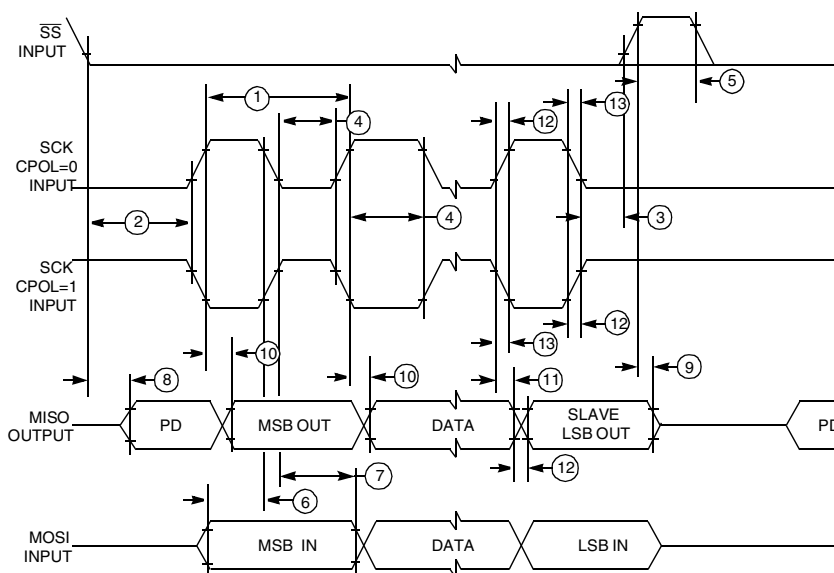
QSPI MAST CPHA1

**Figure A-17 QSPI Timing — Master, CPHA = 1**



QSPI SLV CPHA0

**Figure A-18 QSPI Timing — Slave, CPHA = 0**



QSPI SLV CPHA1

**Figure A-19 QSPI Timing — Slave, CPHA = 1**



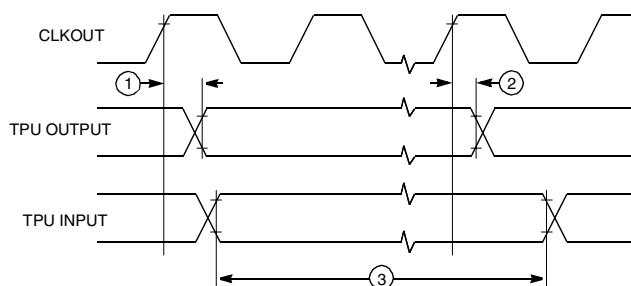
**Table A-10 Time Processor Unit Timing**

( $V_{DD}$  and  $V_{DDSYN} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ ,  $f_{sys} = 20.97 \text{ MHz}$ )<sup>1, 2</sup>

Num	Rating	Symbol	Min	Max	Unit
1	CLKOUT High to TPU Output Channel Valid <sup>3, 4</sup>	$t_{CHTOV}$	2	18	ns
2	CLKOUT High to TPU Output Channel Hold	$t_{CHTOH}$	0	15	ns
3	TPU Input Channel Pulse Width	$t_{TIPW}$	4	—	$t_{cyc}$

**NOTES:**

1. AC timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$  levels.
2. Timing not valid for external T2CLK input.
3. Maximum load capacitance for CLKOUT pin is 90 pF.
4. Maximum load capacitance for TPU output pins is 100 pF.



TPU I/O TIM

**Figure A-20 TPU Timing Diagram**





**Table A-11 QADC Maximum Ratings**

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply, with reference to $V_{SSA}$	$V_{DDA}$	- 0.3	6.5	V
2	Internal Digital Supply, with reference to $V_{SSI}$	$V_{DDI}$	- 0.3	6.5	V
3	Reference Supply, with reference to $V_{RL}$	$V_{RH}$	- 0.3	6.5	V
4	$V_{SS}$ Differential Voltage	$V_{SSI} - V_{SSA}$	- 0.1	0.1	V
5	$V_{DD}$ Differential Voltage	$V_{DDI} - V_{DDA}$	- 6.5	6.5	V
6	$V_{REF}$ Differential Voltage	$V_{RH} - V_{RL}$	- 6.5	6.5	V
7	$V_{RH}$ to $V_{DDA}$ Differential Voltage	$V_{RH} - V_{DDA}$	- 6.5	6.5	V
8	$V_{RL}$ to $V_{SSA}$ Differential Voltage	$V_{RL} - V_{SSA}$	- 6.5	6.5	V
9	Disruptive Input Current <sup>1, 2, 3, 4, 5, 6, 7</sup> $V_{NEGCLAMP} = -0.3$ V $V_{POSCLAMP} = 8$ V	$I_{NA}$	- 500	500	$\mu$ A
10	Positive Overvoltage Current Coupling Ratio <sup>1, 5, 6, 8</sup> PQA PQB	$K_P$	2000 2000	—	—
11	Negative Overvoltage Current Coupling Ratio <sup>1, 5, 6, 8</sup> PQA PQB	$K_N$	125 500	—	—
12	Maximum Input Current <sup>3, 4, 6</sup> $V_{NEGCLAMP} = -0.3$ V $V_{POSCLAMP} = 8$ V	$I_{MA}$	- 25	25	mA

**NOTES:**

- Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than  $V_{RH}$  and \$000 for values less than  $V_{RL}$ . This assumes that  $V_{RH} \leq V_{DDA}$  and  $V_{RL} \geq V_{SSA}$  due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
- Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also affect the conversion accuracy of other channels.
- Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
- This parameter is periodically sampled rather than 100% tested.
- Condition applies to one pin at a time.
- Determination of actual maximum disruptive input current, which can affect operation, is related to external system component values.
- Current coupling is the ratio of the current induced from overvoltage (positive or negative, through an external series coupling resistor), divided by the current induced on adjacent pins. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins.



**Table A-12 QADC DC Electrical Characteristics (Operating)**

( $V_{SSI}$  and  $V_{SSA} = 0V_{dc}$ ,  $f_{QCLK} = 2.1 \text{ MHz}$ ,  $T_A = T_L$  to  $T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply <sup>1</sup>	$V_{DDA}$	4.5	5.5	V
2	Internal Digital Supply <sup>1</sup>	$V_{DDI}$	4.5	5.5	V
3	$V_{SS}$ Differential Voltage	$V_{SSI} - V_{SSA}$	-1.0	1.0	mV
4	$V_{DD}$ Differential Voltage	$V_{DDI} - V_{DDA}$	-1.0	1.0	V
5	Reference Voltage Low <sup>2</sup>	$V_{RL}$	$V_{SSA}$	—	V
6	Reference Voltage High <sup>2</sup>	$V_{RH}$	—	$V_{DDA}$	V
7	$V_{REF}$ Differential Voltage <sup>3</sup>	$V_{RH} - V_{RL}$	4.5	5.5	V
8	Mid-Analog Supply Voltage	$V_{DDA}/2$	2.25	2.75	V
9	Input Voltage	$V_{INDC}$	$V_{SSA}$	$V_{DDA}$	V
10	Input High Voltage, PQA and PQB	$V_{IH}$	$0.7 (V_{DDA})$	$V_{DDA} + 0.3$	V
11	Input Low Voltage, PQA and PQB	$V_{IL}$	$V_{SSA} - 0.3$	$0.2 (V_{DDA})$	V
12	Input Hysteresis <sup>4</sup>	$V_{HYS}$	0.5	—	V
13	Output Low Voltage, PQA <sup>5</sup> $I_{OL} = 5.3 \text{ mA}$ $I_{OL} = 10.0 \mu\text{A}$	$V_{OL}$	— —	0.4 0.2	V
14	Analog Supply Current Normal Operation <sup>6</sup> Low-Power Stop	$I_{DDA}$	— —	1.0 10.0	mA $\mu\text{A}$
15	Reference Supply Current	$I_{REF}$	—	150	$\mu\text{A}$
16	Load Capacitance, PQA	$C_L$	—	90	pF
17	Input Current, Channel Off <sup>7</sup> PQA PQB	$I_{OFF}$	— —	250 150	nA
18	Total Input Capacitance <sup>8</sup> PQA Not Sampling PQA Sampling PQB Not Sampling PQB Sampling	$C_{IN}$	— — — —	15 20 10 15	pF

**NOTES:**

- Refers to operation over full temperature and frequency range.
- To obtain full-scale, full-range results,  $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$ .
- Accuracy tested and guaranteed at  $V_{RH} - V_{RL} = 5.0V \pm 10\%$ .
- Parameter applies to the following pins:  
Port A: PQA[7:0]/AN[59:58]/ETRIG[2:1]  
Port B: PQB[7:0]/AN[3:0]/AN[51:48]/AN[Z:W]
- Open drain only.
- Current measured at maximum system clock frequency with QADC active.
- Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each  $10^\circ \text{C}$  decrease from maximum temperature.
- This parameter is periodically sampled rather than 100% tested.



**Table A-13 QADC AC Electrical Characteristics (Operating)**

( $V_{DDI}$  and  $V_{DDA} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SSI}$  and  $V_{SSA} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	QADC Clock (QCLK) Frequency <sup>1</sup>	$f_{QCLK}$	0.5	2.1	MHz
2	QADC Clock Duty Cycle <sup>2, 3</sup> High Phase Time ( $t_{PSL} \leq t_{PSH}$ )	$t_{PSH}$	500	—	ns
3	Conversion Cycles <sup>4</sup>	CC	18	32	QCLK cycles
4	Conversion Time <sup>2,4,5</sup> $f_{QCLK} = 0.999 \text{ MHz}^6$ Min = CCW/IST = %00 Max = CCW/IST = %11 $f_{QCLK} = 2.097 \text{ MHz}^{1, 7}$ Min = CCW/IST = %00 Max = CCW/IST = %11	$t_{CONV}$	18.0  8.58	32  15.24	$\mu\text{s}$
5	Stop Mode Recovery Time	$t_{SR}$	—	10	$\mu\text{s}$

**NOTES:**

1. Conversion characteristics vary with  $f_{QCLK}$  rate. Reduced conversion accuracy occurs at max  $f_{QCLK}$  rate.
2. Duty cycle must be as close as possible to 75% to achieve optimum performance.
3. Minimum applies to 1.0 MHz operation.
4. Assumes that short input sample time has been selected (IST = 0).
5. Assumes that  $f_{sys} = 20.97 \text{ MHz}$ .
6. Assumes  $f_{QCLK} = 0.999 \text{ MHz}$ , with clock prescaler values of:  
QACR0: PSH = %01111, PSA = %1, PSL = 100)  
CCW: BYP = %0
7. Assumes  $f_{QCLK} = 2.097 \text{ MHz}$ , with clock prescaler values of:  
QACR0: PSH = %00110, PSA = %1, PSL = 010)  
CCW: BYP = %0



**Table A-14 QADC Conversion Characteristics (Operating)**

( $V_{DDI}$  and  $V_{DDA} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SSI}$  and  $V_{SSA} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ ,  
 $0.5 \text{ MHz} \leq f_{QCLK} \leq 2.1 \text{ MHz}$ , 2 clock input sample time)

Num	Parameter	Symbol	Min	Typ	Max	Unit
1	Resolution <sup>1</sup>	1 Count	—	5	—	mV
2	Differential nonlinearity <sup>2</sup>	DNL	—	—	$\pm 0.5$	Counts
3	Integral nonlinearity	INL	—	—	$\pm 2.0$	Counts
4	Absolute error <sup>2, 3, 4</sup> $f_{QCLK} = 0.999 \text{ MHz}^5$ PQA PQB $f_{QCLK} = 2.097 \text{ MHz}^6$ PQA PQB	AE	— — — —	— — — —	$\pm 2.5$ $\pm 2.5$ $\pm 4.0$ $\pm 4.0$	Counts
5	Source impedance at input <sup>7</sup>	$R_S$	—	20	—	$k^{\frac{3}{4}}$

**NOTES:**

- At  $V_{RH} - V_{RL} = 5.12 \text{ V}$ , one count = 5 mV.
- This parameter is periodically sampled rather than 100% tested.
- Absolute error includes 1/2 count (2.5 mV) of inherent quantization error and circuit (differential, integral, and offset) error. Specification assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  capacitor between analog input and analog ground, typical source isolation impedance of 20 k $\Omega$ .
- Assumes  $f_{sys} = 20.97 \text{ MHz}$ .
- Assumes clock prescaler values of:  
QACR0: PSH = %01111, PSA = %1, PSL = 100)  
CCW: BYP = %0
- Assumes clock prescaler values of:  
QACR0: PSH = %00110, PSA = %1, PSL = 010)  
CCW: BYP = %0
- Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.  
Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage ( $V_{errj}$ ):  

$$V_{errj} = R_S \times I_{OFF}$$
where  $I_{OFF}$  is a function of operating temperature. Refer to [Table A-12](#).  
Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the decoupling capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.



**Table A-15 FCSM Timing Characteristics**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin frequency <sup>1</sup>	$f_{PCNTR}$	0	$f_{sys}/4$	MHz
2	Input pin low time <sup>1</sup>	$t_{PINL}$	$2.0/f_{sys}$	—	$\mu\text{s}$
3	Input pin high time <sup>1</sup>	$t_{PINH}$	$2.0/f_{sys}$	—	$\mu\text{s}$
4	Clock pin to counter increment	$t_{PINC}$	$4.5/f_{sys}$	$6.5/f_{sys}$	$\mu\text{s}$
5	Clock pin to new TBB value	$t_{PTBB}$	$5.0/f_{sys}$	$7.0/f_{sys}$	$\mu\text{s}$
6	Clock pin to COF set (\$FFFF)	$t_{PCOF}$	$4.5/f_{sys}$	$6.5/f_{sys}$	$\mu\text{s}$
7	Pin to IN bit delay	$t_{PINB}$	$1.5/f_{sys}$	$2.5/f_{sys}$	$\mu\text{s}$
8	Flag to IMB interrupt request	$t_{FIRQ}$	$1.0/f_{sys}$	$1.0/f_{sys}$	$\mu\text{s}$
9	Counter resolution <sup>2</sup>	$t_{CRES}$	—	$2.0/f_{sys}$	$\mu\text{s}$

**NOTES:**

1. Value applies when using external clock.
2. Value applies when using internal clock. Minimum counter resolution depends on prescaler divide ratio selection.

**Table A-16 MCSM Timing Characteristics**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin frequency <sup>1</sup>	$f_{PCNTR}$	0	$f_{sys}/4$	MHz
2	Input pin low time <sup>1</sup>	$t_{PINL}$	$2.0/f_{sys}$	—	$\mu\text{s}$
3	Input pin high time <sup>1</sup>	$t_{PINH}$	$2.0/f_{sys}$	—	$\mu\text{s}$
4	Clock pin to counter increment	$t_{PINC}$	$4.5/f_{sys}$	$6.5/f_{sys}$	$\mu\text{s}$
5	Clock pin to new TBB value	$t_{PTBB}$	$5.0/f_{sys}$	$7.0/f_{sys}$	$\mu\text{s}$
6	Clock pin to COF set (\$FFFF)	$t_{PCOF}$	$4.5/f_{sys}$	$6.5/f_{sys}$	$\mu\text{s}$
7	Load pin to new counter value	$t_{PLOAD}$	$2.5/f_{sys}$	$3.5/f_{sys}$	$\mu\text{s}$
8	Pin to IN bit delay	$t_{PINB}$	$1.5/f_{sys}$	$2.5/f_{sys}$	$\mu\text{s}$
9	Flag to IMB interrupt request	$t_{FIRQ}$	$1.0/f_{sys}$	$1.0/f_{sys}$	$\mu\text{s}$
10	Counter resolution <sup>2</sup>	$t_{CRES}$	—	$2.0/f_{sys}$	$\mu\text{s}$

**NOTES:**

1. Value applies when using external clock.
2. Value applies when using internal clock. Minimum counter resolution depends on prescaler divide ratio selection.



**Table A-17 SASM Timing Characteristics**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0\text{Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	$t_{PINL}$	$2.0/f_{sys}$	—	$\mu\text{s}$
2	Input pin high time	$t_{PINH}$	$2.0/f_{sys}$	—	$\mu\text{s}$
3	Input capture resolution <sup>1</sup>	$t_{RESCA}$	—	$2.0/f_{sys}$	$\mu\text{s}$
4	Pin to input capture delay	$t_{PCAPT}$	$2.5/f_{sys}$	$4.5/f_{sys}$	$\mu\text{s}$
5	Pin to FLAG set	$t_{PFLAG}$	$2.5/f_{sys}$	$4.5/f_{sys}$	$\mu\text{s}$
6	Pin to IN bit delay	$t_{PINB}$	$1.5/f_{sys}$	$2.5/f_{sys}$	$\mu\text{s}$
7	OCT output pulse	$t_{OCT}$	$2.0/f_{sys}$	—	$\mu\text{s}$
8	Compare resolution <sup>1</sup>	$t_{RESCM}$	—	$2.0/f_{sys}$	$\mu\text{s}$
9	TBB change to FLAG set	$t_{CFLAG}$	$1.5/f_{sys}$	$1.5/f_{sys}$	$\mu\text{s}$
10	TBB change to pin change <sup>2</sup>	$t_{CPIN}$	$1.5/f_{sys}$	$1.5/f_{sys}$	$\mu\text{s}$
11	FLAG to IMB interrupt request <sup>2</sup>	$t_{FIRQ}$	$1.0/f_{sys}$	$1.0/f_{sys}$	$\mu\text{s}$

NOTES:

1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.

**Table A-18 DASM Timing Characteristics**

( $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	$t_{PINL}$	$2.0/f_{sys}$	—	$\mu\text{s}$
2	Input pin high time	$t_{PINH}$	$2.0/f_{sys}$	—	$\mu\text{s}$
3	Input capture resolution <sup>1</sup>	$t_{RESCA}$	—	$2.0/f_{sys}$	$\mu\text{s}$
4	Pin to input capture delay	$t_{PCAPT}$	$2.5/f_{sys}$	$4.5/f_{sys}$	$\mu\text{s}$
5	Pin to FLAG set	$t_{PFLAG}$	$2.5/f_{sys}$	$4.5/f_{sys}$	$\mu\text{s}$
6	Pin to IN bit delay	$t_{PINB}$	$1.5/f_{sys}$	$2.5/f_{sys}$	$\mu\text{s}$
7	OCT output pulse	$t_{OCT}$	$2.0/f_{sys}$	—	$\mu\text{s}$
8	Compare resolution <sup>1</sup>	$t_{RESCM}$	—	$2.0/f_{sys}$	$\mu\text{s}$
9	TBB change to FLAG set	$t_{CFLAG}$	$1.5/f_{sys}$	$1.5/f_{sys}$	$\mu\text{s}$
10	TBB change to pin change <sup>2</sup>	$t_{CPIN}$	$1.5/f_{sys}$	$1.5/f_{sys}$	$\mu\text{s}$
11	FLAG to IMB interrupt request <sup>2</sup>	$t_{FIRQ}$	$1.0/f_{sys}$	$1.0/f_{sys}$	$\mu\text{s}$

NOTES:

1. Minimum resolution depends on counter and prescaler divide ratio selection.
2. Time given from when new value is stable on time base bus.



**Table A-19 PWMSM Timing Characteristics**

( $V_{DD} = 5.0\text{Vdc} \pm 5\%$ ,  $V_{SS} = 0\text{Vdc}$ ,  $T_A = T_L$  to  $T_H$ )

Num	Parameter	Symbol	Min	Max	Unit
1	PWMSM output resolution <sup>1</sup>	$t_{PWMR}$	—	—	$\mu\text{s}$
2	PWMSM output pulse <sup>2</sup>	$t_{PWMO}$	$2.0/f_{\text{sys}}$	—	$\mu\text{s}$
3	PWMSM output pulse <sup>3</sup>	$t_{PWMO}$	$2.0/f_{\text{sys}}$	$2.0/f_{\text{sys}}$	$\mu\text{s}$
4	CPSM enable to output set PWMSM enabled before CPSM , DIV23 = 0 PWMSM enabled before CPSM , DIV23 = 1	$t_{PWMP}$	$3.5/f_{\text{sys}}$ $6.5/f_{\text{sys}}$	—	$\mu\text{s}$
5	PWM enable to output set PWMSM enabled before CPSM , DIV23 = 0 PWMSM enabled before CPSM , DIV23 = 1	$t_{PWME}$	$3.5/f_{\text{sys}}$ $5.5/f_{\text{sys}}$	$4.5/f_{\text{sys}}$ $6.5/f_{\text{sys}}$	$\mu\text{s}$
6	FLAG to IMB interrupt request	$t_{FIRQ}$	$1.5/f_{\text{sys}}$	$2.5/f_{\text{sys}}$	$\mu\text{s}$

**NOTES:**

1. Minimum output resolution depends on counter and prescaler divide ratio selection.
2. Excluding the case where the output is always zero.
3. Excluding the case where the output is always zero.

