Freescale Semiconductor
Technical Data

Document Number: MHE1003N
Rev. 0, 7/2016

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 220 W CW high efficiency RF power transistor is designed for consumer and commercial cooking applications operating in the 2450 MHz ISM band.

Typical Performance: V_{DD} = 26 Vdc, I_{DQ} = 50 mA

Frequency (MHz)	Signal Type	G_{ps} (dB)	PAE (%)	P_{out} (W)
2400	CW	14.0	61.5	230
2450		13.9	62.0	224
2500		11.5	61.8	214

Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage	Result
2450	CW	> 10:1 at all Phase Angles	20 (3 dB Overdrive)	28	No Device Degradation

Features

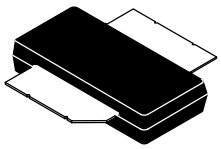
- Characterized with series equivalent large-signal impedance parameters and common source S-parameters
- Internally pre-matched for ease of use
- Qualified for operation up to 28 Vdc
- Integrated ESD protection
- 150°C case operating temperature
- 225°C die temperature capability

Target Applications

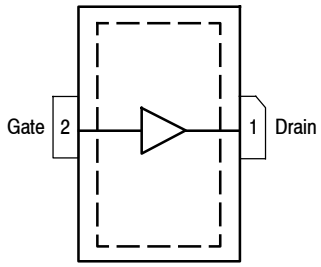
- Consumer cooking
- Commercial cooking

MHE1003N

**2450 MHz, 220 W CW, 26 V
RF POWER LDMOS TRANSISTOR
FOR CONSUMER AND
COMMERCIAL COOKING**



**OM-780-2L
PLASTIC**



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	28, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	833 4.17	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 88°C, 220 W CW, 26 Vdc, I_{DQ} = 100 mA, 2450 MHz	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 2000 V

Table 4. Moisture Sensitivity Level (MSL)

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 303 μAdc)	$V_{GS(th)}$	1.6	2.0	2.4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 100 mAdc)	$V_{GS(Q)}$	—	2.48	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.7 Adc)	$V_{DS(on)}$	—	0.15	—	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	5.8	—	pF

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 6. Typical Performance

In Freescale Reference Circuit, 50 ohm system, V_{DD} = 26 Vdc, I_{DQ} = 50 mA, P_{out} = 220 W, f = 2450 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	—	14.1	—	dB
Power Added Efficiency	PAE	—	63.5	—	%
P_{out} @ 1 dB Compression Point	P1dB	—	206	—	W
P_{out} @ 3 dB Compression Point	P3dB	—	245	—	W
Gain Variation over Temperature (+25°C to +125°C)	ΔG	—	–0.035	—	dB/°C
Output Power Variation over Temperature (+25°C to +125°C)	ΔP1dB	—	0.0046	—	dB/°C

Table 7. Load Mismatch/Ruggedness

In Freescale Reference Circuit, 50 ohm system, I_{DQ} = 50 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
2450	CW	> 10:1 at all Phase Angles	20 (3 dB Overdrive)	28	No Device Degradation

Table 8. Ordering Information

Device	Tape and Reel Information	Package
MHE1003NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-2L

TYPICAL CHARACTERISTICS

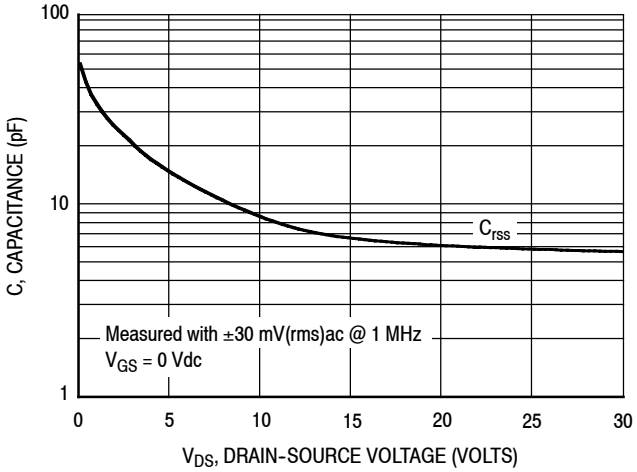
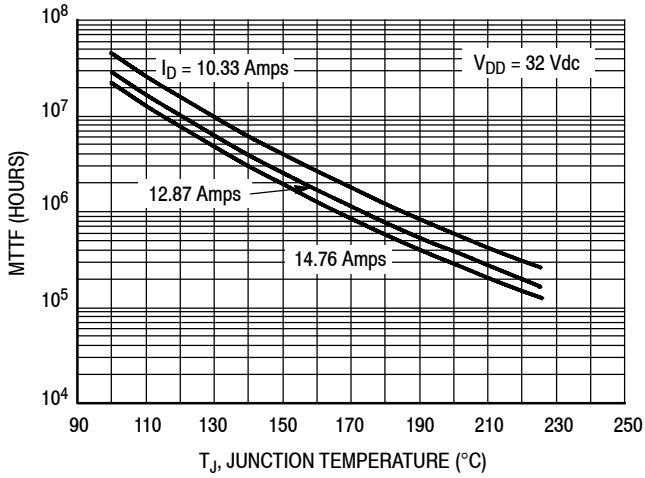


Figure 2. Capacitance versus Drain-Source Voltage



Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http:/www.nxp.com/RF/calculators.

Figure 3. MTTF versus Junction Temperature - CW

Table 9. Load Pull Performance — Maximum Power Tuning

V_{DD} = 26 Vdc, I_{DQ} = 53 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	3.93 – j8.86	4.27 + j8.95	1.14 – j4.72	14.5	54.6	289	51.6	50.7
2450	8.57 – j10.3	8.96 + j10.0	1.16 – j4.84	14.5	54.7	297	52.0	51.0
2500	15.1 – j4.11	15.9 + j3.48	1.25 – j4.99	14.5	54.4	278	49.9	49.0

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	3.93 – j8.86	4.55 + j9.34	1.16 – j4.82	12.4	55.5	353	55.1	53.4
2450	8.57 – j10.3	9.94 + j10.2	1.22 – j4.98	12.3	55.5	358	55.3	53.5
2500	15.1 – j4.11	16.5 + j1.87	1.29 – j5.21	12.2	55.3	337	51.9	50.4

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

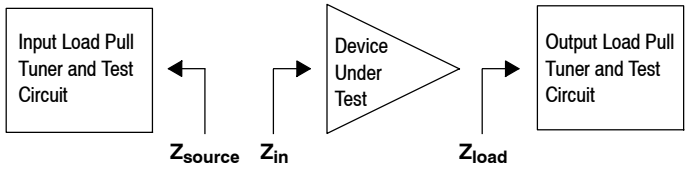
Table 10. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 26 Vdc, I_{DQ} = 53 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	3.93 – j8.86	4.67 + j9.21	2.48 – j3.31	16.4	52.5	178	63.7	62.8
2450	8.57 – j10.3	9.99 + j9.85	2.22 – j3.22	16.5	52.5	179	65.3	64.4
2500	15.1 – j4.11	16.0 + j1.96	2.08 – j3.34	16.5	52.4	174	62.9	62.1

			Max Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	3.93 – j8.86	4.98 + j9.55	2.31 – j3.37	14.5	53.4	218	65.6	64.1
2450	8.57 – j10.3	11.0 + j9.96	2.06 – j3.26	14.6	53.3	216	67.0	65.4
2500	15.1 – j4.11	16.1 + j0.27	2.00 – j3.38	14.5	53.2	209	64.5	63.1

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P3dB – TYPICAL LOAD PULL CONTOURS — 2450 MHz

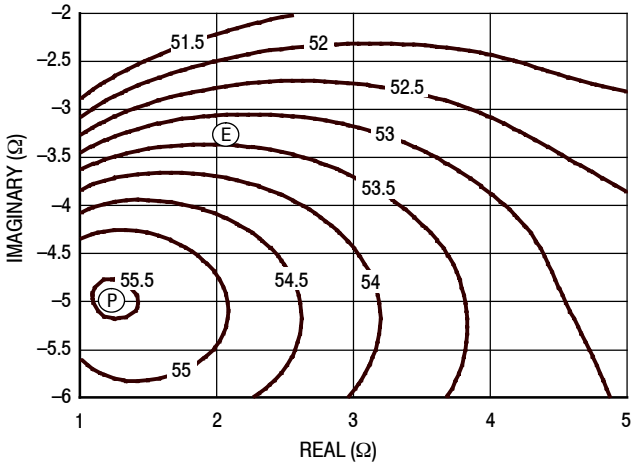


Figure 4. P3dB Load Pull Output Power Contours (dBm)

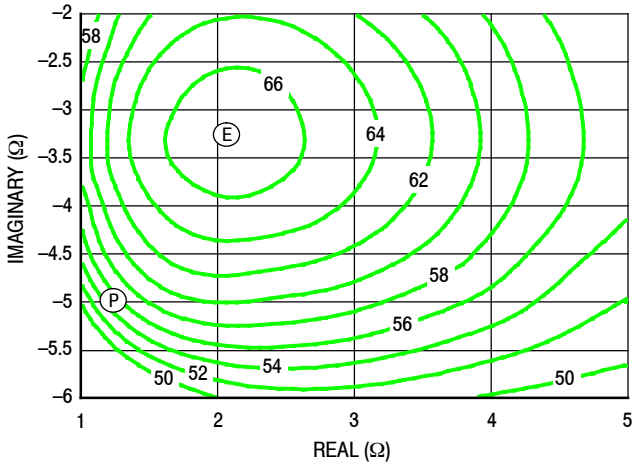


Figure 5. P3dB Load Pull PAE Contours (%)

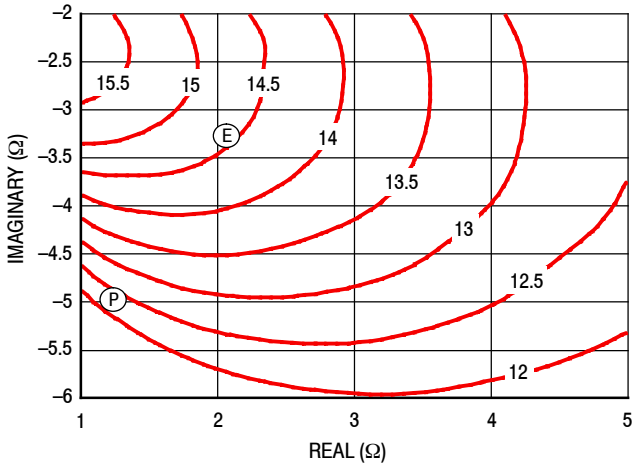


Figure 6. P3dB Load Pull Gain Contours (dB)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Linearity

Output Power

2450 MHz REFERENCE CIRCUIT — 2″ × 3″ (5.1 cm × 7.6 cm)

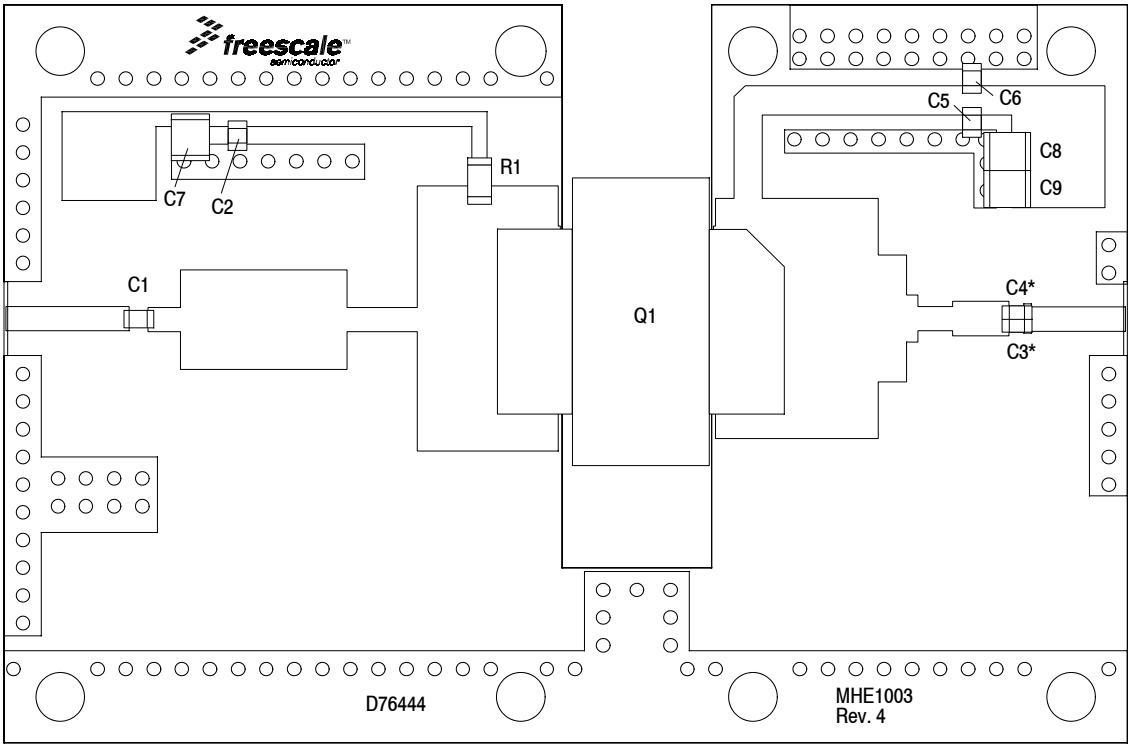
Table 11. 2450 MHz Performance (In Freescale Reference Circuit, 50 ohm system)
V_{DD} = 26 Vdc, I_{DQ} = 50 mA, T_A = 25°C

Frequency (MHz)	P_{in} (W)	G_{ps} (dB)	PAE (%)	P_{out} (W)
2400	9	14.0	61.5	230
2450	9	13.9	62.0	224
2500	15	11.5	61.8	214

Table 12. Load Mismatch/Ruggedness (In Freescale Reference Circuit)

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
2450	CW	> 10:1 at all Phase Angles	20 (3 dB Overdrive)	28	No Device Degradation

2450 MHz REFERENCE CIRCUIT — 2″ × 3″ (5.1 cm × 7.6 cm)



*C3 and C4 are mounted vertically.

Figure 7. MHE1003N Reference Circuit Component Layout — 2450 MHz

Table 13. MHE1003N Reference Circuit Component Designations and Values — 2450 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	27 pF Chip Capacitors	ATC600F270JT250XT	ATC
C7, C8, C9	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF Power LDMOS Transistor	MHE1003N	NXP
R1	10 Ω, 1/4 W Chip Resistor	CRCW120610R0JNEA	Vishay
PCB	Rogers RO4350B, 0.030″, ε_r = 3.66	D76444	MTL

TYPICAL CHARACTERISTICS — 2450 MHz REFERENCE CIRCUIT

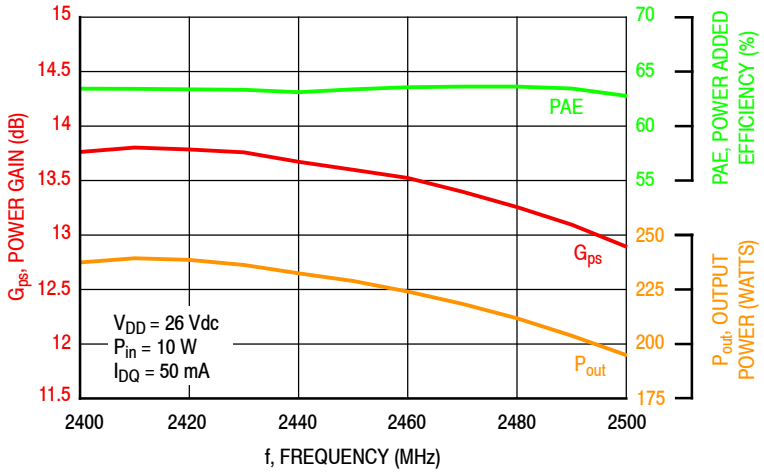


Figure 8. Power Gain, Power Added Efficiency and Output Power versus Frequency at a Constant Input Power

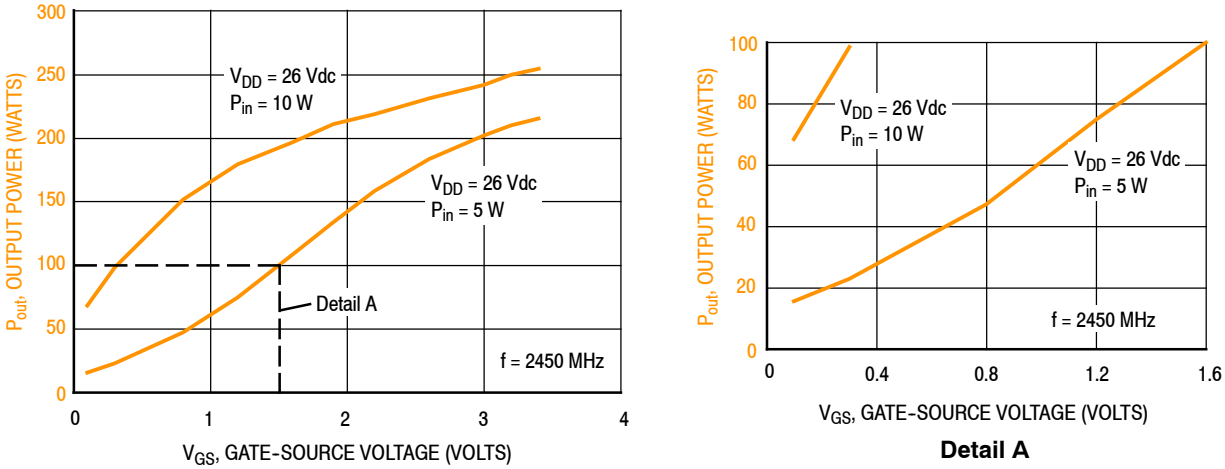


Figure 9. Output Power versus Gate-Source Voltage

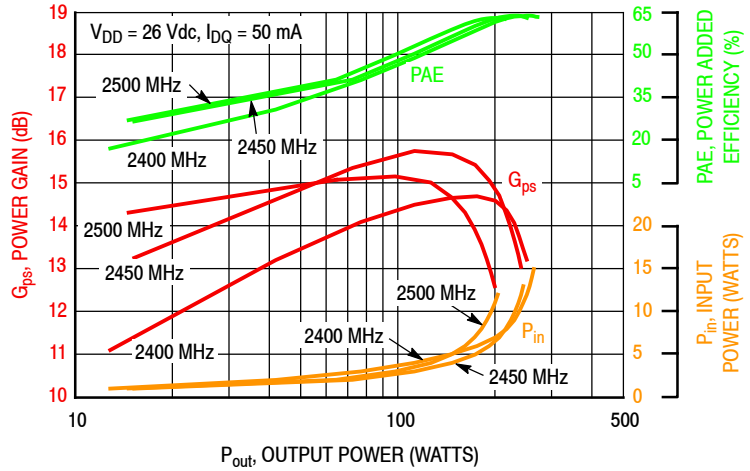


Figure 10. Power Gain, Power Added Efficiency and Input Power versus Output Power and Frequency

TYPICAL CHARACTERISTICS — 2450 MHz REFERENCE CIRCUIT

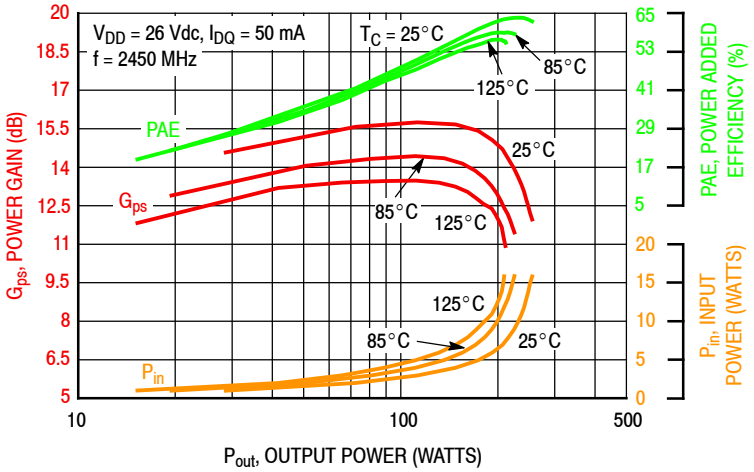
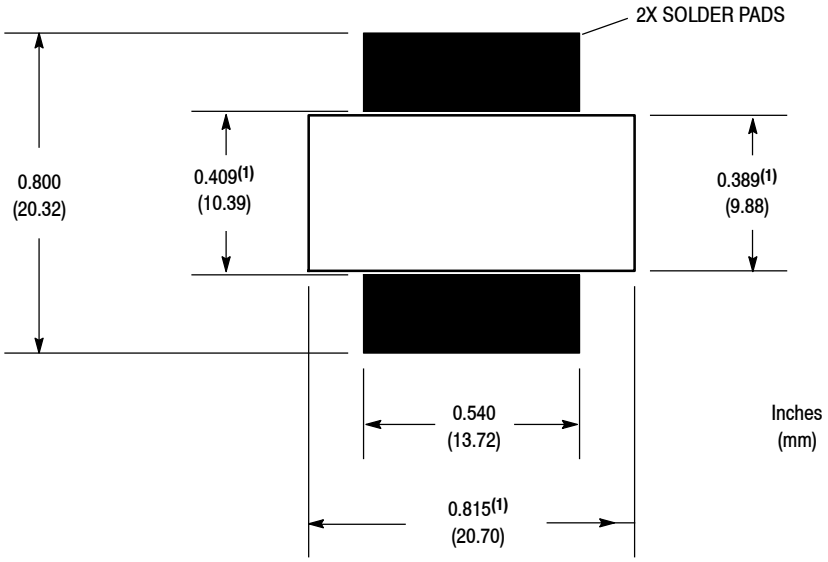


Figure 11. Power Gain, Power Added Efficiency and Input Power versus Output Power and Temperature

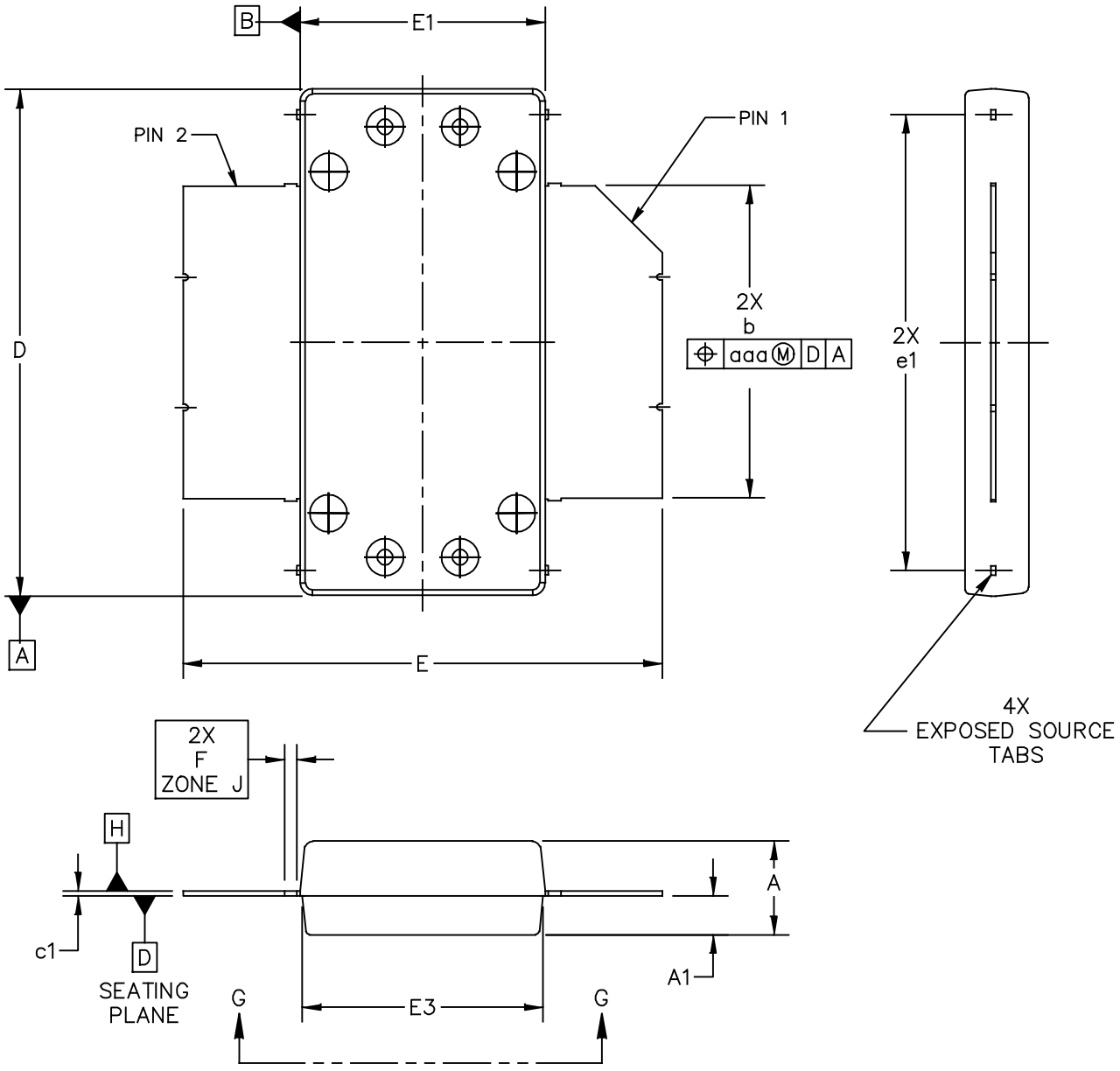


1. Slot dimensions are minimum dimensions and exclude milling tolerances

Figure 12. PCB Pad Layout for OM-780-2L

Figure 13. Product Marking

PACKAGE DIMENSIONS



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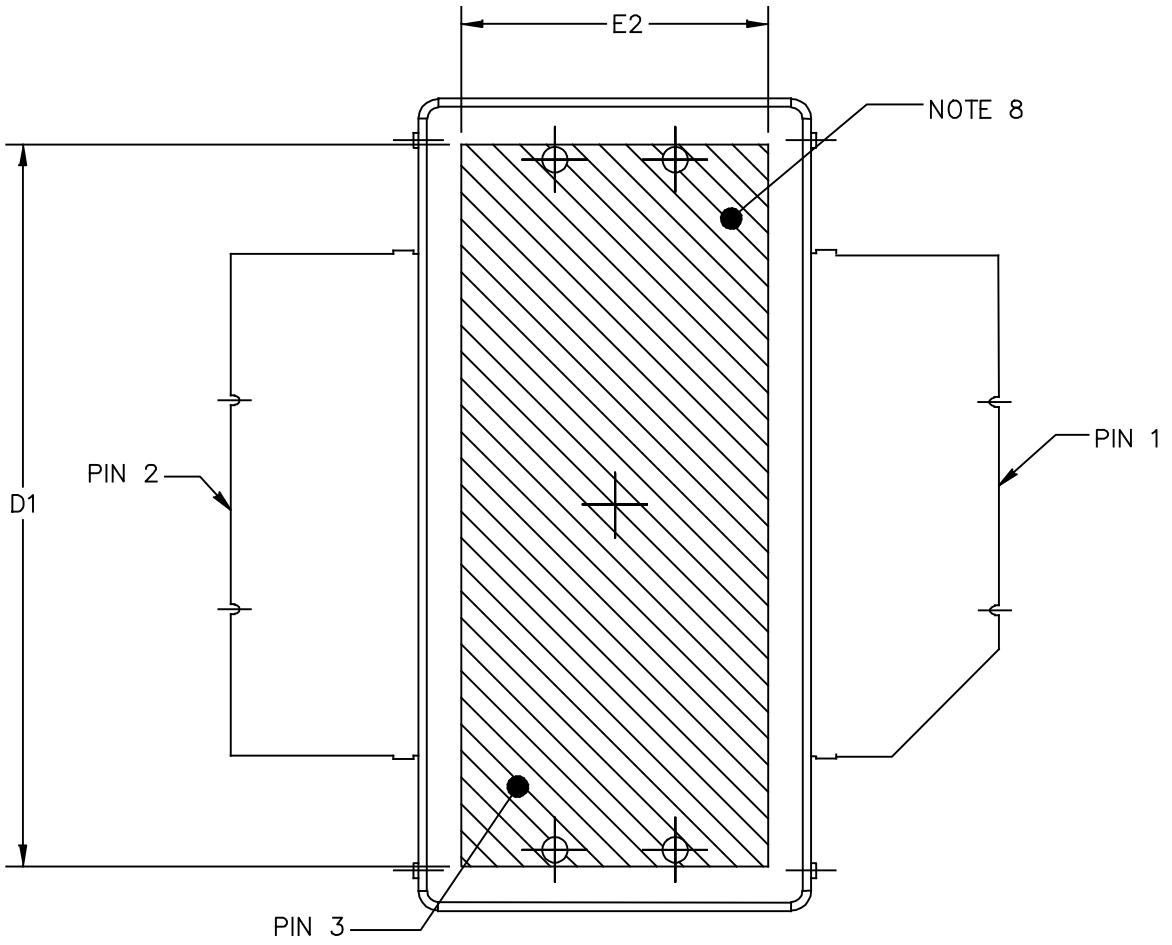
	STANDARD: NON–JEDEC	
	SOT1693–1	22 JAN 2016



BOTTOM VIEW
VIEW G–G

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	STANDARD: NON–JEDEC	
	SOT1693–1	22 JAN 2016

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: OM780–2
STRAIGHT LEAD

DOCUMENT NO: 98ASA10831D REV: C
STANDARD: NON–JEDEC
SOT1693–1 22 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2016	• Initial Release of Data Sheet

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Document Number: MHE1003N
Rev. 0, 7/2016