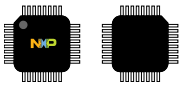
MCXAP100M180F41

Baseline Arm Cortex M33 MCU with 180 MHz, up to 256 KB Flash

Rev. 2 — 30 November 2025 Product data sheet

180 MHz Arm® Cortex®-M33 microcontroller for Industrial and Consumer IoT Applications.



LQFP100

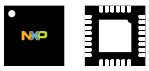
14 x 14 x 1.4 mm, 0.5 mm

LQFP64

10 x 10 x 1.4 mm, 0.5 mm

LQFP48

7 x 7 x 1.4 mm, 0.5 mm



H-PQFN32

5 x 5 x 0.9 mm, 0.5 mm

Features

- Arm Cortex-M33 180 MHz with 738 CoreMark® (4.10 CoreMark®/MHz)
- Up to 256 KB Flash, up to 64 KB SRAM, up to 8 KB RAM with ECC
- All RAM can be retained down to Deep Power Down mode
- Internal free running oscillator (FRO180M) with ±1% precision at junction temperature across the full temperature range
- Temperature range: -40 °C to 125 °C
- Down to 66 µA/MHz Active current, 52 µA Deep Sleep current, 17 µA Power Down current, 408 nA Deep Power Down current

Core

- Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set and MPU, no Trust Zone

Processing Accelerators

- SmartDMA, co-processor for applications such as parallel camera interface and keypad scanning

Memories

- Single-bank Flash: Up to 256 KB FLASH with ECC (support one bit correction and two bits detection, 8 KB shared with CMPA)
- Cache Engine with 8 KB RAM
- Up to 64 KB RAM of which 8 KB is shared with cache, configurable as up to 8 KB RAM with ECC (support single bit correction, two bits detection)
- All RAM can be retained down to deep power down mode
- ROM

Security

- 128-bit Universal Unique Identifier (UUID) per device in accordance with IETF's RFC4122 version 5 specification
- Device lifecycle management
- Flash read/write execute permission protect by MBC and lockable
- Implicit-protected Flash Region (IFR)
- Security Monitoring
  - Code Watchdog for code flow integrity checking
  - GLIKEY enhances protection against attacks to gain unauthorized access to sensitive registers

Low-Power Performance

- **Active**

  - 66 µA/MHz in Active Mode (executing while(1) from flash, 3.3 V at 25 °C)
- **Deep Sleep**
  - 52 µA, 9.18 µs wake-up (3.3 V at 25 °C)
- **Power Down**
  - 17 µA, 19.36 µs wake-up (full SRAM retention, 3.3 V at 25 ℃)
- **Deep Power Down**
  - 408 nA, 0.81 ms wake-up (wakeup timer enabled, reset pin enabled, all SRAM off, 3.3 V at 25 °C)

System and Clocks

- 180 MHz free-running oscillator (FRO180M)
- 12 MHz free-running oscillator (FRO12M)
- 16 kHz free-running oscillator (FRO16K)
- Up to 50 MHz crystal oscillator
- Hardware and Software Watchdogs
- Asynchronous DMA modules (8-channels)

Communication interfaces for Connectivity

- 2x LPSPI, 2x LPI2C, 4x LPUART
- 1x FlexCAN with FD

Advanced Motor Control Subsys

- Up to 2x FlexPWM each with 4 submodules, providing 16 complementary outputs of PWM (no Nanoedge module)
- Up to 2x Quadrature Encoder/Decoder (eQDC)
- 2x AOI (AND/OR/Invert) module support up to 4 output trigger

Analog modules

- 2x 16-bit ADC
  - Up to 3 Msps in 16-bit mode, and 3.75 Msps in 12-bit mode
  - Up to 39 ADC Input channels total (depending on the package)
  - 1x Integrated temperature sensor
- 2x High-speed Comparators with 8 input pins and 8-bit DAC as internal reference
  - 1x LPCMP is functional down to Deep Power Down mode
- 1x OPAMP without PGA

Timers

- 3x 32-bit standard general-purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
- Low power timer
- Frequency measurement timer
- Windowed Watchdog Timer
- Waketimer
- Micro-Tick Timer(UTICK)
- OS Event Timer

- RTC timer without external 32KHz input

General-purpose input/output

- Up to 86 GPIOs
- Up to eight 20 mA IO
- 50 MHz IO on P1, P3 and P4
- Up to 25-pin wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V IO supply range
- Up to two 5V tolerant IO (P3_27, P3_28)

Power Management

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating voltage: 1.71 V to 3.6 V
- IOs: 1.71 V - 3.6 V full-performance

Target Applications Industrial

- Energy Storage and Management System
- Smart Metering
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor(PMSM) Control

Smart Home

- Home Control Panel
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Table 1. Ordering Information

Part Number [1][2]	Marking	Core Speed (MHz)	Flash (KB)	SRAM (K)	GPIOs	Pin Count	Package
MCXA174VLL	MCXA174VLL	180	256	64	86	100	LQFP
MCXA174VLH	MCXA174VLH	180	256	64	55	64	LQFP

Table continues on the next page...

Table 1. Ordering Information *...continued*

Part Number [1][2]	Marking	Core Speed (MHz)	Flash (KB)	SRAM (K)	GPIOs	Pin Count	Package
MCXA174VLF	MA174F	180	256	64	41	48	LQFP
MCXA174VFM	MA174M	180	256	64	29	32	HPQFN
MCXA173VLL	MCXA173VLL	180	128	32	86	100	LQFP
MCXA173VLH	MCXA173VLH	180	128	32	55	64	LQFP
MCXA173VLF	MA173F	180	128	32	41	48	LQFP
MCXA173VFM	MA173M	180	128	32	29	32	HPQFN

[1] As marked on package
[2] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Table 2. Device Revision Number

Device Mask Set Number	JTAG ID Register[PRN]
0P25N	0x0726902B

Table 3. Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	MCXA1xxFS
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXAP100M180F41RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXA174VLL_P25N
Package drawing	Package dimensions are provided in package drawings.	• LQFP100:98ASS23308W • LQFP64: 98ASS23234W • LQFP48: 98AH00962A • H-PQFN32:98ASA02110D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

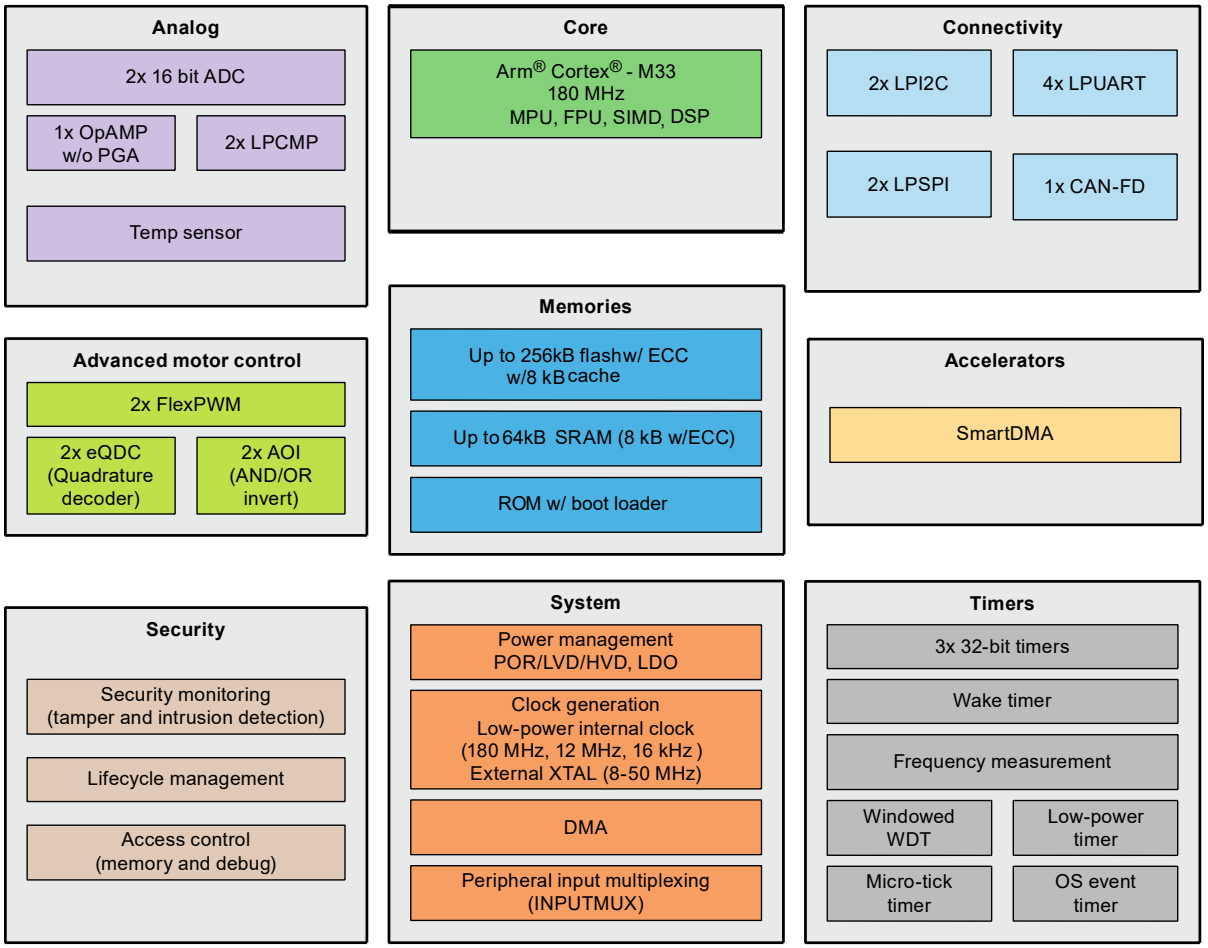


Figure 1. Block Diagram

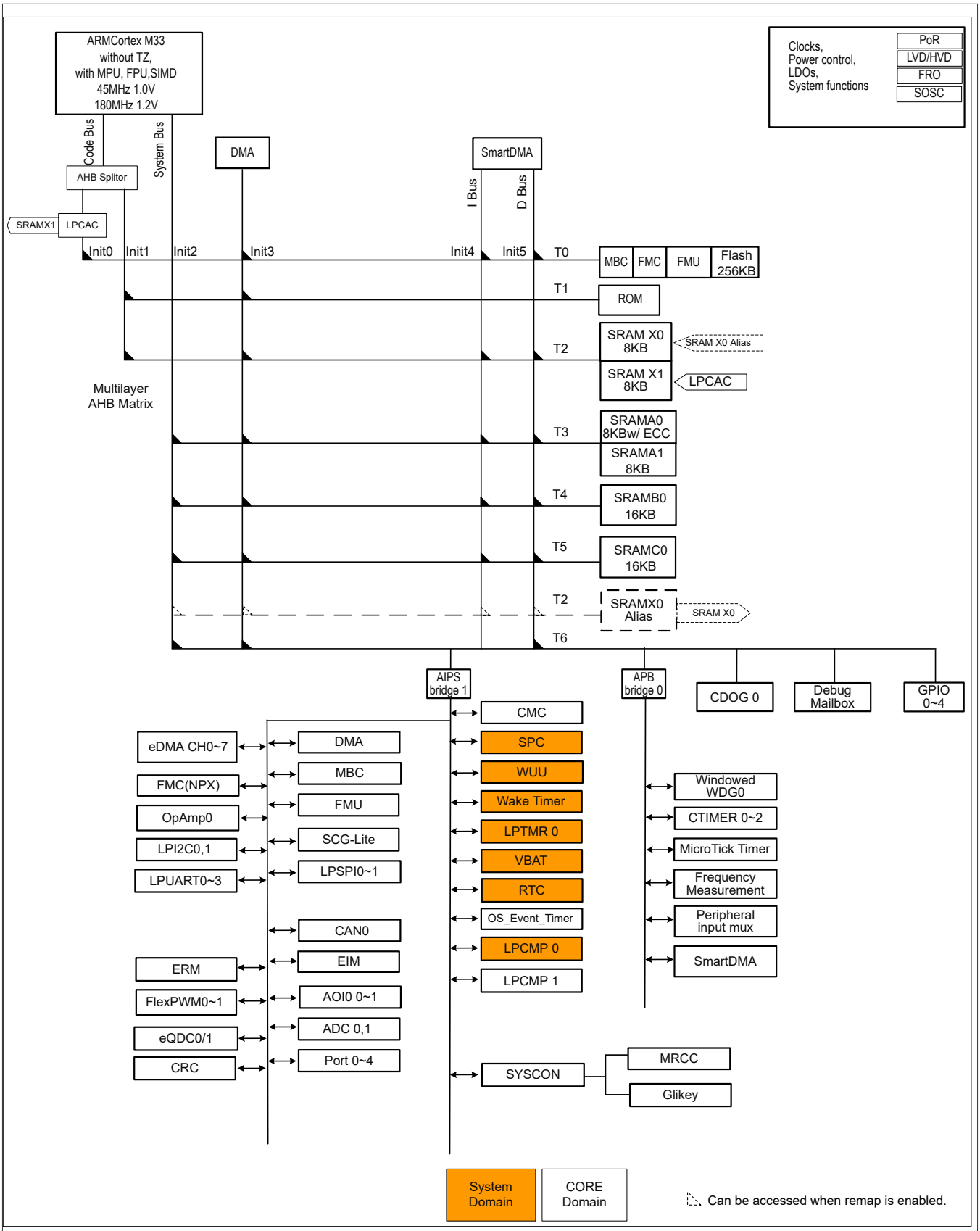


Figure 2. Bus Architecture diagram

1 Feature Comparison

Table 4. Feature comparision

		MCX A173	MCX A174
Core Platform	Core Cortex-M33	180 MHz	
	Cache	8 KB	
	DMA	8 Channels	
	Wakeup unit (WUU)	Yes	
	Pheripheral input multiplexing (INPUTMUX)	Yes	
Processing Accelerators	MAU	No	
	SmartDMA	Yes	
Clock	Fast internal reference clock FRO180M	180 MHz	
	Slow internal reference clock FRO12M	12 MHz	
	Low power internal reference clock FRO16K	16.384 KHz	
	System oscillator with external crystal (SOSC)	8 - 50 MHz	
	PLL	No	
Memory	Flash	128 KB w/ECC w/ 8 KB CMPA	256 KB w/ECC w/ 8KB CMPA
	SRAM	32 KB including 8 kB with ECC	64 KB including 8 KB with ECC and include 8KB SRAM shared with Cache
	Error injection module (EIM)	Yes	
	Error recording module (ERM)	Yes	
Security	Lifecycle management (LC)	Yes	
	Read out protection (ROP)	Yes	
	Memory block checker (MBC)	Yes	
	GLIKEY	Yes	
	UUID	128-bit	
	Code watchdog (CDOG)	1	
	Cyclic redundancy check (CRC)	1	
Communication Interfaces	LPUART	4	
	LPSPI	2	
	LPI2C	2	
	FlexCAN	1x CAN FD	
Analog	ADC	2	

Table continues on the next page...

Table 4. Feature comparision...*continued*

			MCX A173	MCX A174
	ADC input pin	LQFP100(LL)	39	
		LQFP64(LH)	31	
		LQFP48(LF)	21	
		HPQFN32(FM)	13	
	Low power comparator(LPCMP)		2	
	DAC		No	
	OpAmp(w/o PGA)	LQFP100(LL)	1	
		LQFP64(LH)	1	
		LQFP48(LF)	1	
		H-PQFN32(FM)	1	
Motor Control	FlexPWM [1]		2	
	AND/OR INVERT (AOI)		2	
	Quadrature decoder (eQDC)		2	
Timer	32-bit timer (Ctimer)		3	
	Low power timer (LPTMR)		1	
	Micro-tick timer (UTICK)		1	
	OS event timer		1	
	Windowed watchdog timer (WWDT)		1	
	Frequency measurement (FREQME)		1	
	Wake timer		1	
	RTC [2]		1	
IO	Independent IO supply [3]		No	
	5V tolerant IO [4]		2	
	High drive IO (20 mA) [5]		Up to 8	
	50MHz IO [6]		Up to 20	
Packages [7]	GPIO/Wakeup Pin	LQFP100(LL)	86/25	
		LQFP64(LH)	55/19	
		LQFP48(LF)	41/14	
		H-PQFN32(FM)	29/12	
Temperature range			-40 ℃ to 125 ℃	

[1] There are 4 sub-modules for each FlexPWM module.
[2] RTC only supports counter mode, no dedicate VBAT and not support external 32.768KHz crystal.
[3] MCX A173/A174 does not support 1.2V independent IO power supply.
[4] P3_27, P3_28 are 5V tolerant IOs.
[5] P1_8,P1_9,P1_30,P1_31,P3_1,P3_0,P0_16,P0_17 are High Drive IOs.
[6] 50 MHz IOs are located on P1, P3, P4 ports.
[7] Show the package types and GPIO numbers and Wakeup pin numbers.

2 Ratings

2.1 Thermal handling ratings

Table 5. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
TSTG	Storage temperature [1]	–55	—	150	°C	—
TSDR	Solder temperature, lead-free [2]	—	—	260	°C	—

[1] Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
[2] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.2 Moisture handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level [1]	—	—	3	—	—

[1] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.3 ESD handling ratings

Table 7. ESD handling ratings

Description	Rating	Unit	Notes
Electrostatic discharge voltage, human body model	+/-2000	V	[1]
Electrostatic discharge voltage, charged-device model	+/-500	V	[2]
Electrostatic discharge voltage, charged device model (corner pins)	+/-750	V	[2]
Latch-up immunity level (Class II at 110 °C junction temperature)	Immunity Level A	—	[3]

[1] Determined according to ANSI/ESDA/JEDEC Standard JS-001-2017, Human Body Model (HBM) - Component Level.
[2] Determined according to ANSI/ESDA/JEDEC JS-002-2022, Charged Device Model (CDM) - Device Level.
[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

2.4 Voltage and current maximum ratings

Table 8. Voltage and current maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage for Port 0, Port 1, Port 2, Port 3 and Port 4	-0.3	—	3.63	V	—
VDD_ANA	Supply voltage for ADC	-0.3	—	3.63	V	—
VDIO	Digital input voltage	-0.3	—	VDD + 0.3	V	—

Table continues on the next page...

Table 8. Voltage and current maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDIO_5VTOL	Digital input voltage for 5V tolerant I/O pins	-0.3	—	min(VDD + 3.6V, 5.5V)	V	—
VAIO	Analog input voltageAnalog pins are defined as pins that do not have an associated general-purpose I/O port function. [1]	-0.3	—	VDD_ ANA + 0. 3	V	—
IDD	Digital supply current [2]	—	—	100	mA	—
ID	Maximum current single pin limit (digital output pins)	-25	—	25	mA	—

[1] Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
[2] This limit is per supply pin. It includes all power pins, including VDD, VDD_ANA.

2.5 Required Power-On-Reset (POR) Sequencing

- VDD and VDD_ANA must be same voltage

3 General

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

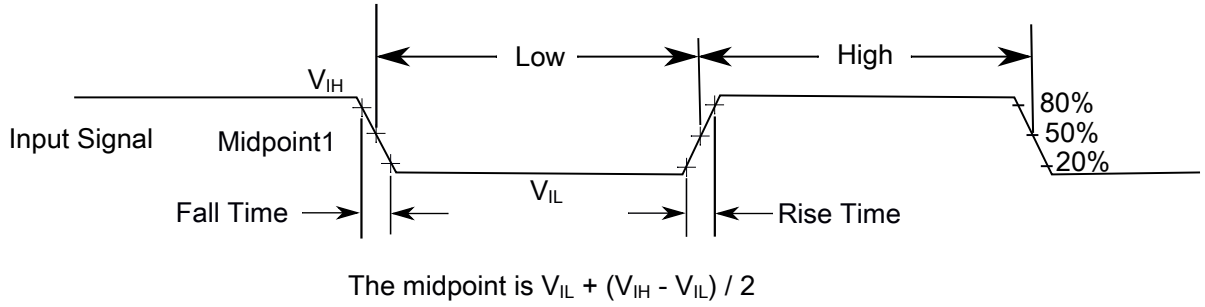


Figure 3. Input signal measurement reference

3.2 Nonswitching electrical specifications

3.2.1 Voltage and current operating requirement

Table 9. Voltage and current operating requirement

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply Voltage for IO, LDO, Flash, and LPCMP	1.71	—	3.6	V	—

Table continues on the next page...

Table 9. Voltage and current operating requirement*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ANA	Supply voltage for ADC	VDD - 0.1	—	VDD + 0.1	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1	—	0.1	V	—
VIH	Input high voltage	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIH_5VTOL	Input high voltage of 5V tolerant IO	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIL	Input low voltage	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VIL_5VTOL	Input low voltage of 5 V tolerant IO	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VHYS	Input hysteresis	0.1 × VDD	—	—	V	—
VHYS_5VTOL	Input hysteresis of 5 V tolerant IO	0.1 × VDD	—	—	V	—
IICIO	IO pin DC injection current — per pin [1]	-3	—	—	mA	VIN < VSS-0.3 V (negative current injection)
IICIO	IO pin DC injection current — per pin [1]	—	—	3	mA	VIN > VDD+0.3 V (positive current injection)
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	Negative current injection
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	—	—	25	mA	Positive current injection
VODPU	Open drain pullup voltage level [2]	VDD	—	VDD	V	—

[1] All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD_MIN(=VSS-0.3 V) or is less than VDD_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-IICIOmin). The positive injection current limiting resistor is calculated as R=(VIN-VDD_MAX)/IICIOmax. The actual resistor should be an order of magnitude higher to tolerate transient voltages

[2] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

3.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD
- VDD_CORE

3.2.2.1 VDD supply HVD, LVD, and POR Operating Requirements

Table 10. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VHVDH_VDD	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	—
VHVDH_HYS_VDD	VDD High-voltage inhibit reset/ recover hysteresis	—	38	—	mV	—
VLVDH_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - high range	2.567	2.619	2.673	V	—
VLVDH_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - high range	—	27	—	mV	—
VLVDL_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - low range	1.618	1.651	1.684	V	—
VLVDL_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - low range	—	16	—	mV	—

3.2.3 Voltage and current operating behaviors

Table 11. Voltage and current operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA
IOHT	Output high current total for all ports	—	—	100	mA	—
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA
IOLT	Output low current total for all ports	—	—	100	mA	—

Table continues on the next page...

Table 11. Voltage and current operating behaviors...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IIN	Input leakage current (per pin) for full temperature range [4]	—	0.02	1	µA	—
IIN	Input leakage current (per pin) at 25 °C [4]	—	0.001	0.025	µA	—
IOZ	Hi-Z (off-state) leakage current (per pin)	—	0.02	1	µA	—
RPU	Internal pullup resistors	33	50	75	kΩ	—
RPD	Internal pulldown resistors	33	50	75	kΩ	—
RHPU	High-resistance pullup option (PCRx[PV] = 1) [5]	0.67	—	1.5	MΩ	—
RHPD	High-resistance pulldown option (PCRx[PV] = 1) [5]	0.67	—	1.5	MΩ	—
VBG	Bandgap voltage reference voltage	0.98	1.0	1.02	V	—

[1] For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.
[2] RESET_B pins are always configured in high drive mode
[3] Open drain outputs must be pulled to VDD
[4] Measured at VDD = 3.6 V.
[5] Only RESET_B pins support this option.

3.2.4 On-chip regulator electrical specifications

3.2.4.1 LDO_CORE electrical specifications

Table 12. LDO_CORE electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	LDO_CORE input supply voltage	1.71	—	3.6	V	—
ILOAD	LDO_CORE max load current	—	—	96	mA	Over drive strength
ILOAD	LDO_CORE max load current	—	—	2	mA	Low drive strength
IDD	LDO_CORE current consumption	—	—	250	µA	Over drive strength
IDD	LDO_CORE current consumption	—	—	500	nA	Low drive strength
IINRUSH	LDO_CORE inrush current	—	—	10	mA	—

3.2.5 Power mode transition operating behaviours

All specifications in the following table assume this clock configuration:

- CPU clock = 45 MHz
- AHB clock = 45 MHz
- Clock source = FRO180M

3.2.5.1 Power mode transition operating behaviors

Table 13. Power mode transition operating behaviors

Symbol	Description	Min	Typ	Max	Unit
tPOR	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD reach 1.8 V) across the operating temperature range of the chip.[1],[2]	—	2.1	2.13	ms
tSLEEP	SLEEP → ACTIVE [1],[2],[3],[4]	—	0.24	0.29	µs
tDSLEEP	DEEP SLEEP → ACTIVE [1],[2],[3],[4]	—	9.18	10.33	µs
tPWDN	Power DOWN → ACTIVE [1],[2],[3],[5]	—	19.36	22.4	µs
tDPWDN	Deep Power DOWN → ACTIVE [1],[2],[3],[4]	—	0.81	0.83	ms

[1] Max value is mean+3 × sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production.
[2] Typical value is the average of values tested at Temperature=25 ℃ and VDD=3.3 V
[3] WFE used for Low Power mode entry
[4] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured for the same level in Active and Low Power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL]=SPC->LP_CFG[CORELDO_VDD_LVL]= 01b).
[5] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x5B and the Core voltage level is configured as different level for Active mode, (SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = 01b for Active mode, SPC->LP_CFG[CORELDO_VDD_LVL] = 00b for Low Power mode)

3.2.6 Power consumption operating behaviors

The maximum values stated in the following sections represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

3.2.6.1 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD_ANA.
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

Table 14. Power consumption operating behaviors

Symbol	Description	Condition [1]	Typ	Unit
IDD_ACT_MD_1 [2]	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	2.67	mA
		105 °C	3.78	mA
		125 °C	4.83	mA
IDD_ACT_MD_2	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	2.82	mA
		105 °C	3.95	mA
		125 °C	5.00	mA

Table continues on the next page...

Table 14. Power consumption operating behaviors*...continued*

IDD_ACT_MD_CM_1	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.	25 °C	3.17	mA
		105 °C	4.28	mA
		125 °C	5.32	mA
IDD_ACT_MD_CM_2	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	3.31	mA
		105 °C	4.46	mA
		125 °C	5.49	mA
IDD_ACT_OD_1	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	10.85	mA
		105 °C	12.54	mA
		125 °C	14.00	mA
IDD_ACT_OD_2	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	11.28	mA
		105 °C	13.00	mA
		125 °C	14.45	mA
IDD_ACT_OD_CM_1	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.	25 °C	13.22	mA
		105 °C	14.98	mA
		125 °C	16.46	mA
IDD_ACT_OD_CM_2	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	13.65	mA
		105 °C	15.42	mA
		125 °C	16.87	mA
IDD_SLEEP_OD_1	1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	5.67	mA
		105 °C	7.33	mA
		125 °C	8.76	mA
IDD_SLEEP_OD_2	1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.	25 °C	5.87	mA
		105 °C	7.53	mA
		125 °C	8.96	mA
IDD_SLEEP_MD_1	1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	1.61	mA
		105 °C	2.74	mA
		125 °C	3.78	mA
IDD_SLEEP_MD_2	1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.	25 °C	1.67	mA
		105 °C	2.81	mA
		125 °C	3.85	mA
IDD_SLEEP_MD_3	1. CPU_CLK = OFF; SYSTEM_CLK = 12 MHz from FRO12M. VDD_CORE = 1.0 V from LDO_CORE Low Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	0.383	mA
		105 °C	1.52	mA
		125 °C	2.59	mA

Table continues on the next page...

Table 14. Power consumption operating behaviors*...continued*

IDD_DEEP_SLEEP_OD_1	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.2 V from LDO_CORE Normal Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	460.17	µA
		105 °C	1880	µA
		125 °C	2980	µA
IDD_DEEP_SLEEP_MD_1	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	51.62	µA
		105 °C	1010	µA
		125 °C	1920	µA
IDD_DEEP_SLEEP_MD_2	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M enabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	97.92	µA
		105 °C	1060	µA
		125 °C	1970	µA
IDD_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 0.6V retention voltage from LDO_CORE Low Drive 2. All RAM retained; FRO16K disabled. 3. Core in WFI.	25 °C	16.55	µA
		105 °C	507.22	µA
		125 °C	1010	µA
IDD_DEEP_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer disabled, FRO16K disabled. 3. Core in WFI.	25 °C	0.408	µA
		105 °C	5.05	µA
		125 °C	11.34	µA
IDD_DEEP_POWER_DOWN_2	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.566	µA
		105 °C	5.18	µA
		125 °C	11.50	µA
IDD_DEEP_POWER_DOWN_3	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	1.36	µA
		105 °C	25.06	µA
		125 °C	55.18	µA
IDD_DEEP_POWER_DOWN_4	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/A0/A1 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	1.20	µA
		105 °C	20.61	µA
		125 °C	45.40	µA
IDD_DEEP_POWER_DOWN_5	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	1.08	µA
		105 °C	16.93	µA
		125 °C	37.16	µA
IDD_DEEP_POWER_DOWN_6	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.743	µA
		105 °C	7.93	µA
		125 °C	17.40	µA
IDD_DEEP_POWER_DOWN_7	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.978	µA
		105 °C	14.40	µA
		125 °C	31.54	µA

Table continues on the next page...

Table 14. Power consumption operating behaviors...*continued*

IDD_DEEP_POWER_DOWN_8	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.741	µA
		105 °C	7.92	µA
		125 °C	17.41	µA
IDD_DEEP_POWER_DOWN_9	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.753	µA
		105 °C	7.93	µA
		125 °C	17.40	µA
IDD_DEEP_POWER_DOWN_10	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.564	µA
		105 °C	5.16	µA
		125 °C	11.50	µA

[1] Ambient temperature
[2] MD middle drive, core voltage is 1.0V. OD over drive, core voltage is 1.2V.

3.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

3.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

3.2.9 Capacitance attributes

Table 15. Capacitance attributes

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN_A	Input capacitance: analog pins	—	—	7	pF	—
CIN_D	Input capacitance: digital pins	—	—	7	pF	—

3.3 Switching specifications

3.3.1 Device clock specs

Table 16. Device clock specs

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)	—	—	180	MHz	Over drive (OD) mode VDD_CORE = 1.2 V
fSYSTEM	CPU clock (CPU_CLK)	—	—	180	MHz	Over drive (OD) mode VDD_CORE = 1.2 V
fSLOW	Slow clock (SLOW_CLK)	—	—	30	MHz	Over drive (OD) mode VDD_CORE = 1.2 V

Table continues on the next page...

Table 16. Device clock specs...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)	—	—	45	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	45	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSLOW	Slow clock (SLOW_CLK)	—	—	7.5	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V

3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPSPI functions.

3.3.2.1 General switching specifications

Note: *Refer to attached pinout spreadsheet.*

Table 17. General switching specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	GPIO pin interrupt pulse width — Synchronous path [1]	1.5	—	—	SYSTEM clock cycles	The synchronous and asynchronous timing must be met.
—	GPIO pin interrupt pulse width — Asynchronous path	150	—	—	ns	—
—	GPIO pin interrupt pulse width — Asynchronous path	50	—	—	ns	—
—	External RST pin interrupt pulse width — Asynchronous path [2]	330	—	—	ns	This is the shortest pulse that is guaranteed to be recognized.
—	GPIO pin interrupt pulse width — Asynchronous path [2]	16	—	—	ns	—
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)

Table continues on the next page...

Table 17. General switching specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	HD pins [7]	2.2	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive, fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive (DSE = 0), fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	15	ns	2.7 ≤ VDD ≤ 3.6 V, Normal drive (DSE =0), slow slew rate (SRE = 1)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE=1), Fast slew rate (SRE = 0)

Table continues on the next page...

Table 17. General switching specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Port rise/fall time for HD pins [7]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE =1), Slow slew rate (SRE=1)
—	RST pins [4]	3	—	8	ns	2.7 ≤ VDD ≤ 3.6 V
—	RST pins [4]	3.6	—	20	ns	1.71 ≤ VDD < 2.7 V

[1] The synchronous and asynchronous timing must be met.
[2] This is the shortest pulse that is guaranteed to be recognized
[3] For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance. For the 5VTOL I/O pins, setting DSE1=1 will support the same fall time at 2x the load capacitance, but the rise time will increase due to the increased loading
[4] Load is 25 pF.
[5] Assumes default values in CALIB1 and CALIB0 in PORTS
[6] 25 pF lumped load
[7] Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].

3.4 Thermal specifications

3.4.1 Thermal operating requirements

Table 18. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TA	Ambient temperature [1]	-40	25	125	°C	—
TJ	Die junction temperature [2][3][4]	—	—	125	°C	—

[1] The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is: TJ = TA + RθJA*chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C TJ.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)

3.4.2 Thermal attributes

Table 19. Thermal attributes

Rating	Board Type [1]	Symbol	HPQFN32	LQFP48	LQFP64	LQFP100	Unit
Junction to Ambient Thermal Resistance [2]	2s2p	$R_{\theta JA}$	34.6	56.4	58.9	47.4	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	2s2p	Ψ_{JT}	0.8	3.3	3.7	2.7	°C/W
Junction to Case Top Thermal Resistance [3]	1s	$R_{\theta JC}$	3.8	30	30.5	21.2	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9 for non-leaded package(BGA) while JESD 51-7 is for leaded package(QFN,QFP,SOIC)
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the
[3] Junction-to-Case top thermal resistance determined using an isothermal cold plate. For QFN package, case temperature refers to the exposed pad surface temperature at the package bottom side dead centre. For QFP/BGA packages, case temperature refers to the mold surface temperature at the package top side dead centre.

4 Peripheral operating requirements and behaviors

4.1 Core modules

4.1.1 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 20. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
J1	TCLK frequency of operation	—	—	25	MHz	Boundary Scan (OD mode)
J1	TCLK frequency of operation	—	—	12.5	MHz	Boundary Scan (MD mode)
J1	TCLK frequency of operation	—	—	25	—	JTAG-DP/TAP (OD mode)
J1	TCLK frequency of operation	—	—	12.5	—	JTAG-DP/TAP (MD mode)
J2	TCLK cycle period	1000/J1	—	—	ns	—
J3	TCLK clock pulse width	J2/2	—	—	ns	—
J4	TCLK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCLK rise	—	—	8	ns	OD mode
J5	Boundary scan input data setup time to TCLK rise	—	—	16	ns	MD mode
J6	Boundary scan input data hold time after TCLK rise	1	—	—	ns	OD mode
J6	Boundary scan input data hold time after TCLK rise	1	—	—	ns	MD mode
J7	TCLK low to boundary scan output data valid	—	—	18	ns	OD mode
J7	TCLK low to boundary scan output data valid	—	—	38	—	MD mode
J8	TCLK low to boundary scan output high-Z	—	—	18	ns	OD mode
J8	TCLK low to boundary scan output high-Z	—	—	38	—	MD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	—	—	8	ns	OD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	—	—	16	—	MD mode

Table continues on the next page...

Table 20. JTAG Debug Interface Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	ns	OD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	—	MD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	18	—	OD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	38	ns	MD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	18	ns	OD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	38	—	MD mode

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

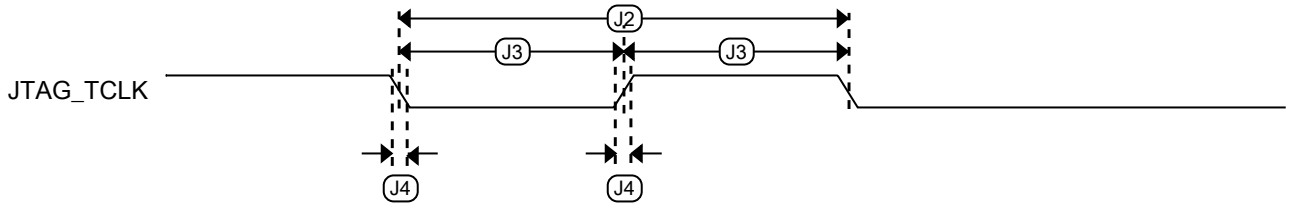


Figure 4. Test clock input timing

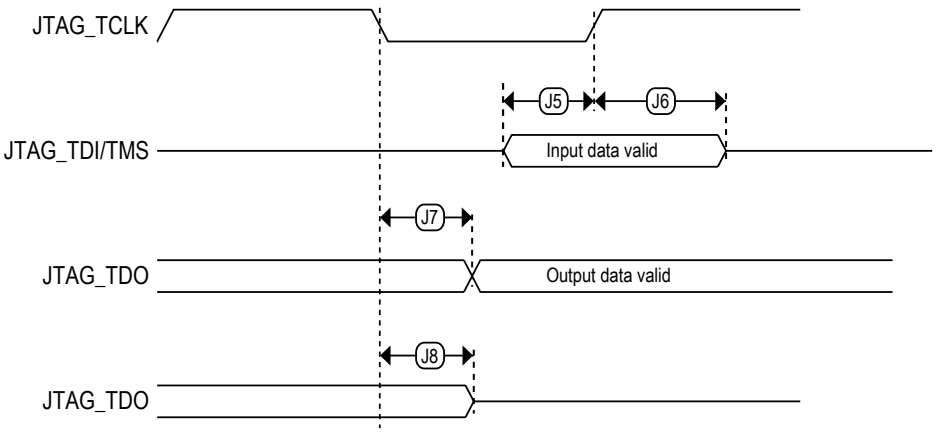


Figure 5. Boundary scan (JTAG) timing

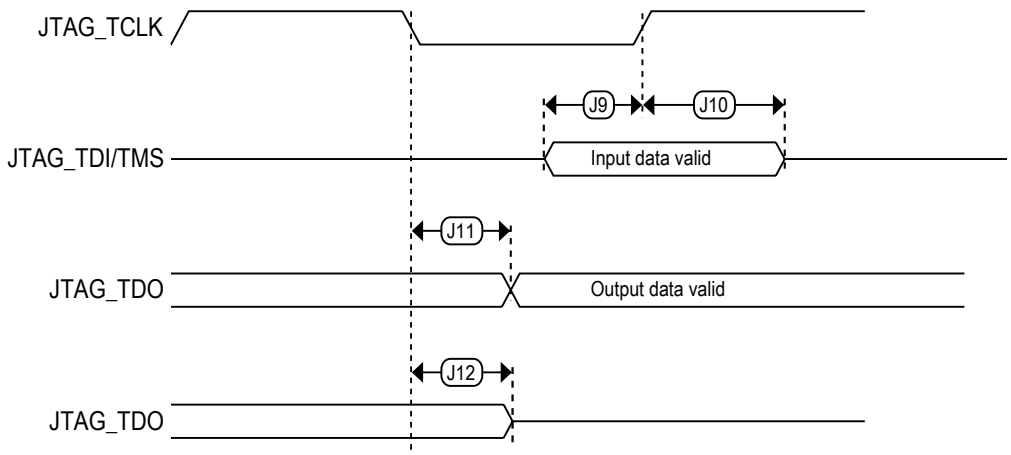


Figure 6. JTAG-DP/TAP timing

4.1.2 Serial Wire Debug (SWD) Timing

The following table gives the Serial Wire Debug specifications for the device.

Table 21. Serial Wire Debug (SWD) Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
S1	SWD_CLK frequency of operation	—	—	25	MHz	OD mode
S1	SWD_CLK frequency of operation	—	—	20	MHz	MD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	OD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	MD mode
S3	SWD_CLK clock pulse width	20	—	—	ns	OD mode
S3	SWD_CLK clock pulse width	25	—	—	ns	MD mode
S4	SWD_CLK rise and fall times	—	—	3	ns	—
S5	SWD_DIO input data setup time to SWD_CLK rise	—	—	10	ns	OD mode
S5	SWD_DIO input data setup time to SWD_CLK rise	—	—	12.5	ns	MD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	OD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	MD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	25	ns	OD mode

Table continues on the next page...

Table 21. Serial Wire Debug (SWD) Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
S7	SWD_CLK high to SWD_DIO data valid	—	—	30	ns	MD mode
S8	SWD_CLK high to SWD_DIO high-Z	—	—	25	ns	OD mode
S8	SWD_CLK high to SWD_DIO high-Z	—	—	30	ns	MD mode

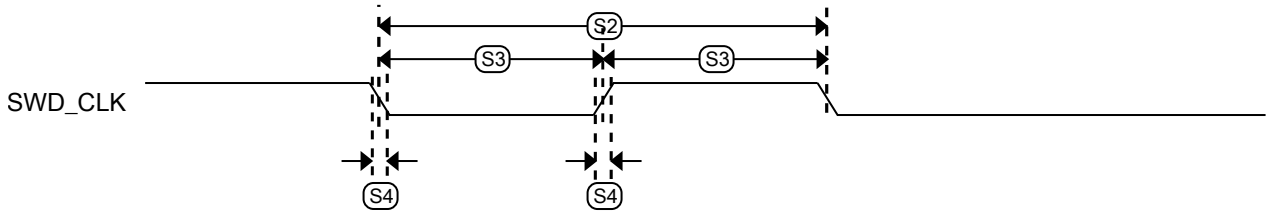


Figure 7. Serial Wire clock input timing

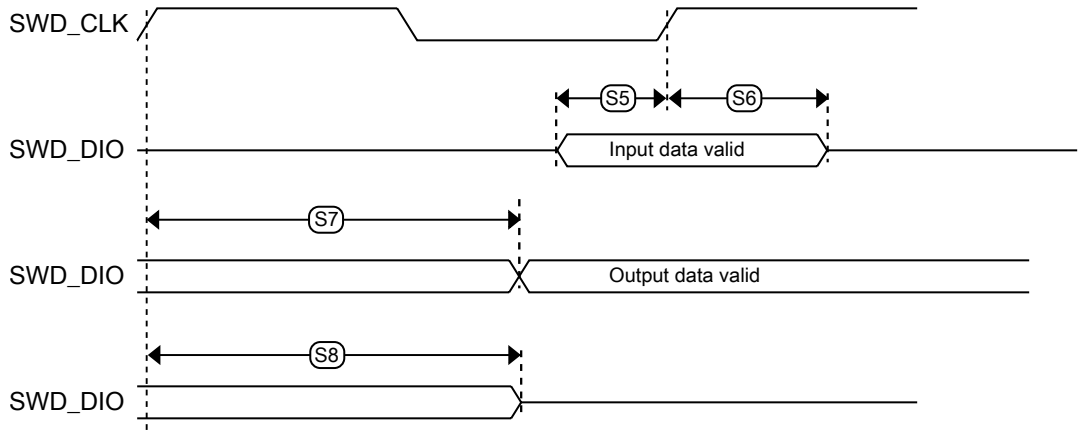


Figure 8. Serial Wire data timing

4.2 Clock modules

4.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

4.2.1.1 System Crystal Oscillator Specification

Table 22. System Crystal Oscillator Specification

Symbol	Description	Min	Typ	Max	Unit	Condition
fosc	Crystal Frequency	8	—	50	MHz	—

Table continues on the next page...

Table 22. System Crystal Oscillator Specification*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Tol	Frequency tolerance	—	±10	±40	ppm	—
Jitosc	Jitter	—	70	—	—	Period jitter (RMS)
Vpp	Peak-to-peak amplitude of oscillation [1]	—	0.6	—	V	—
fec	Externally provided input clock frequency [2]	0	—	50	MHz	—
tDC_EXTAL	External clock duty cycle	45	50	55	%	—
Vec	Externally provided input clock amplitude [2]	Refer to VIH and VIL specification	—	—	—	—

[1] When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
[2] This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

4.2.1.2 System Oscillator Crystal Specifications.

Table 23. System Oscillator Crystal Specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
CP	Shunt Capacitance	—	1	2	pF	—
ESR	Crystal equivalent series resistance [1]	—	20	50	Ω	—
Cpara	Parasitic capacitance of EXTAL	—	—	8	pF	—
Cpara	Parasitic capacitance of XTAL	—	—	10	pF	—
Cm	Motional capacitance Cm	2.05	2.05	2.665	fF	—
Lm	Motional inductance Lm	7.7	—	—	mH	—
Tstart	Crystal start-up time [2]	—	350	—	µs	—
IOSC	Current consumption	—	270	—	µA	Normal mode
IOSC	Current consumption	—	1	465	—	Sleep mode

[1] Maximum crystal equivalent series resistance for 16 MHz is 80 ohms with 2 pF shunt capacitance.
[2] Dependent on crystal specifications, proper PC board layout procedures must be followed to achieve specifications

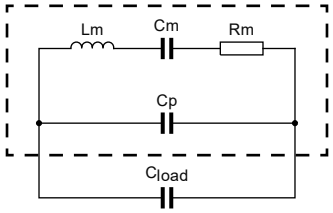


Figure 9. Crystal Electrical Block Diagram

4.2.2 FRO180M specifications

Table 24. FRO180M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
jitper	Period jitter RMS [1]	—	70	—	ps	—
jitper	Accumulated jitter over 10K cycles [1]	—	800	—	ps	—
TJ	Operation temperature	-40	27	125	°C	—
Vvdda	Analog supply voltage	1.71	3.3	3.63	V	—
Vvdd	Digital supply voltage	0.9	1.1	1.21	V	—
Ivdda	3.3v analog supply current	—	50	—	µA	—
Ivdd	1.1v analog supply current	—	58	—	µA	—
Ivdda_dis	3.3v leakage current	—	5	—	nA	—
Ivdd_dis	1.1v leakage current	—	40	—	nA	—
Fclkout	Clock frequency [2]	—	45/45	—	MHz	freq_sel[2:0]=3'b001
Fclkout	Clock frequency [2]	—	60/45	—	MHz	freq_sel[2:0]=3'b011
Fclkout	Clock frequency [2]	—	90/45	—	MHz	freq_sel[2:0]=3'b101
Fclkout	Clock frequency [2]	—	180/45	—	MHz	freq_sel[2:0]=3'b111
Δfclkout	Frequency variation for packages [3]	-1	—	1	%	-40 °C ≤ TJ ≤ 125 °C
Fclkout_closeloop	Close loop accuracy with autotrim from an accurate clock source	-0.25	—	0.25	%	—
Tstartup	Start-up time from disable to 20% accuracy	—	2	—	µs	—
Tsettle	Settling time from disable to 1% accuracy	—	—	50	µs	—
Fovershoot	frequency overshoot during start-up and settling	—	—	2	%	—
DC	Duty cycle of the clock	45	—	55	%	—

[1] Tested at 80 MHz
[2] Frequency in left of slash is fro-hf, and frequency in right of slash is clk_45m in reference manual clocking chapter
[3] Guaranteed by characterization

4.2.3 FRO12M specifications

Table 25. FRO12M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro12m	FRO12M frequency (nominal)	—	12	—	MHz	—
Δffro12m	Frequency deviation	—	—	±3	%	open loop

Table continues on the next page...

Table 25. FRO12M specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Δffro12m	Frequency deviation	—	—	±0.6	%	closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	5	—	µs	—
fos	Frequency overshoot during startup	—	10	20	%	—
Ifro12m	Current consumption	—	7	—	µA	—

4.2.4 FRO16K specifications

Table 26. FRO16K specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro16k	FRO16K frequency (nominal)	—	16.384	—	kHz	—
Δffro16k	Frequency deviation over –40 °C to 125 °C Ta	—	—	±6	%	open loop
TRIMstep	Trimming step	—	1.5	—	%	—
tstartup	Start-up time	—	310	—	µs	—
Ifro16k	Current consumption	—	50	—	nA	—

4.3 Memories and memory interfaces

4.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

4.3.1.1.1 Flash command time specifications

Table 27. Flash command time specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all256k	Read 1s All execution time (256 KB)	—	—	1700	µs	—
trd1all512k	Read 1s All execution time (512 KB)	—	—	3200	µs	—
trd1all1MB	Read 1s All execution time (1 MB)	—	—	6200	µs	—

Table continues on the next page...

Table 27. Flash command time specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1blk256k	Read 1s Block execution time (256 KB)	—	—	1500	µs	—
trd1blk512k	Read 1s Block execution time (512KB)	—	—	3050	µs	—
trd1blk1MB	Read 1s Block execution time (1MB)	—	—	6000	µs	—
trd1scr	Read 1s Sector execution time (8 KB) [1]	—	—	50	µs	—
trd1pg	Read 1s Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1pglv	Read 1s Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1phr	Read 1s Phrase execution time (16B) [1]	—	—	3.8	µs	—
trd1phrlv	Read 1s Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdmisr8k	Read into MISR (8 KB) [1]	—	—	50	µs	—
trdmisr256k	Read into MISR (256 KB)	—	—	1500	µs	—
trdmisr512k	Read into MISR (512 KB)	—	—	3050	µs	—
trdmisr1M	Read into MISR (1 MB) [1]	—	—	6000	µs	—
trd1ipg	Read 1s IFR Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1ipglv	Read 1s IFR Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1iphr	Read 1s IFR Phrase execution time (16 B) [1]	—	—	3.8	µs	—
trd1iphrlv	Read 1s IFR Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdimisr8k	Read IFR into MISR (8 KB) [1]	—	—	50	µs	—
trdimisrk32k	Read IFR into MISR (32 KB) [1]	—	—	190	µs	—
tpgmpg_initial	Program Page execution time at < 1k cycles (128 B) [2]	—	450	600	µs	—
tpgmpg_lifetime	Program Page execution time at > 1k cycles (128 B)	—	450	750	µs	—
tpgmphr_initial	Program Phrase execution time at < 1k cycles (16 B) [2]	—	135	180	µs	—
tpgmphr_lifetime	Program Phrase execution time at > 1k cycles (16 B)	—	135	225	µs	—

Table continues on the next page...

Table 27. Flash command time specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tersall256k	Erase All execution time (256 KB)	—	—	800	ms	—
tersall512k	Erase All execution time (512 KB)	—	—	1500	ms	—
tersall1M	Erase All execution time (1 MB)	—	—	2800	ms	—
tmasers256k	Mass Erase execution time (via sideband) (256 KB)	—	—	800	ms	—
tmasers512k	Mass Erase execution time (via sideband) (512 KB)	—	—	1500	ms	—
tmasers1M	Mass Erase execution time (via sideband) (1 MB)	—	—	2800	ms	—
terrscr	Erase Sector execution time (8 KB) [2]	—	2	22	ms	—

[1] Time to abort the command may significantly impact the time to execute the command.
[2] Measured from the time FSTAT[PERDY] is cleared.

4.3.1.2 Flash high voltage current behavior

Table 28. Flash high voltage current behavior

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_IO_PGM	Average current adder to VDD during flash programming operation [1]	—	—	6	mA	—
IDD_IO_ERS	Average current adder to VDD during flash erase operation [1]	—	—	4	mA	—

[1] See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

4.3.1.3 Flash reliability specifications.

Table 29. Flash reliability specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
Tnvmretp10k	tnvmretp10k	10	50	—	years	Program Flash
Nnvmcycscr	Sector cycling endurance [1]	10 K	500 K	—	cycles	Program Flash
Tnvmretp1k	Data retention after up to 1 K cycles	20	100	—	years	Program Flash
Tnvmretp100k	Data retention after up to 100 K cycles	5	50	—	years	Program Flash
Nnvmcyc256k	Sector cycling endurance for 256 KB [2]	100 K	500 K	—	cycles	Program Flash

[1] Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40°C ≤ Tj ≤ 125°C.
[2] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

Note: *Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.*

4.4 Analog

4.4.1 ADC electrical specifications

ADC operating conditions apply when the ADC is used in differential mode.

All other ADC channels meet the 12-bit single-ended accuracy specifications.

4.4.1.1 ADC operating conditions

Table 30. ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDAD	Supply voltage	1.71	—	3.6	V	—
VSSAD	Ground voltage	-0.1	0	0.1	V	—
ΔVDD	— [1]	-0.1	0	0.1	V	—
ΔVSS	— [1]	-0.1	0	0.1	V	—
VREFH	Reference Voltage High [2]	0.99	VDDAD	VDDAD	V	—
VREFL	Reference Voltage Low [3]	VSSAD	VSSAD	VSSAD	V	—
VADIN	Input Voltage [3][4][5]	VREFL	—	VREFH	V	—
FADCK	ADC conversion clock frequency	6	—	24	MHz	Low-power mode, PWRSEL=0
FADCK	ADC conversion clock frequency	6	—	60	MHz	Normal Mode, 16b, PWRSEL=1
FADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 12b , PWRSEL=1
RAS	Analog source resistance (external) [6]	—	—	5	kΩ	—
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.65	kΩ	VDDAD ≥ 1.71 V
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.525	kΩ	VDDAD ≥ 2.1 V
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	0.925	1.35	kΩ	VDDAD ≥ 2.5 V
CADIN	Input Capacitance	—	1.92	2.4	pF	—

[1] DC potential difference
[2] Minimum VDDAD/VREFH is 2.4 V in high-speed mode (when HS =1)
[3] For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
[4] If VREFH is less than VDD_ANA, then voltage inputs greater than VREFH but less than VDD_ANA are allowed but result in a full-scale conversion result
[5] ADC selected inputs and unselected dedicated inputs must not exceed VDD_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual
[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

4.4.1.2 ADC electrical characteristics

Table 31. ADC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Supply current [1]	—	7	—	—	PWREN = 0, Conversions triggered at 10 kS/s
IDDAD	Supply current [1]	—	60	—	µA	PWREN = 1, No Conversions
IDDAD	Supply current [1]	—	200	—	µA	Low-power mode, 6 MHz Clock, PWRSEL = 0
IDDAD	Supply current [1]	—	257	—	µA	Low-power mode, 22.5 MHz clock, PWRSEL = 0
IDDAD	Supply current [1]	—	645	—	µA	Normal Mode, 60 MHz clock, PWRSEL = 1
IDDAD	Supply cuurent [1]	—	715	—	µA	High Speed Mode, 60 MHz Clock, PWRSEL = 1, HS = 1
IDDTS	Temp Sensor Supply Current	—	50	—	µA	Temperature Sensor Adder
CSMP	ADC Sample cycles [2]	3.5	—	131.5	cycles	Low-power mode and High speed mode
Fconv	ADC conversion rate [3]	—	—	3.75	MS/s	12b mode, (HS = 1)
Fconv	ADC conversion rate [3]	—	—	3.0	MS/s	16b mode, (HS = 1)
TSMP_REQ	Required Sample Time [4]	—	—	—	ns	Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B)
TSMP	Sample Time [5]	145.8	TSMP_REQ	—	ns	Low-power mode
TSMP	Sample Time [6]	58.30	TSMP_REQ	—	ns	High-speed 16b mode
TSMP	Sample Time [6]	58.30	TSMP_REQ	—	ns	High-speed 12b mode
TSMPINT	Internal channel sample time inputs [7]	2.0	—	—	µs	—
DNL	Differential non-linearity [8][9][10]	—	±1	—	LSB	12b mode
INL	Integral non-linearity [8][9][10]	—	±1	—	LSB	12b mode
ZSE	Zero-scale error (V_ADIN = V_REFL) [8][9]	—	±1	—	LSB	12b mode

Table continues on the next page...

Table 31. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
FSE	Full-scale error (V_ADIN = V_REFH) [8][9]	—	±2	—	LSB	12b mode
TUE	Total Unadjusted Error [8][9]	—	±3	—	LSB	12b mode
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][11]	—	15.0	—	bits	23.4 kS/s (FADCK = 60 MHz, HS = 1, AVGS = 0111)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][11]	—	13.4	—	bits	187 kS/s (FADCK = 60 MHz, HS = 1, AVGS = 0100)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][11]	—	12.6	—	bits	750 kS/s (FADCK = 60 MHz, HS = 1, AVGS = 0010)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][11]	—	11.7	—	bits	3.0 MS/s (FADCK = 60 MHz, HS = 1, AVGS = 0000)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][11]	—	11.3	—	bits	0.94 MS/s (FADCK = 60 MHz, HS =1, AVGS = 0010)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][11]	—	10.9	—	bits	3.75 MS/s (FADCK = 60 MHz, HS = 1, AVGS = 0000)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][11]	—	92.1	—	dB	23.4 kS/s (FADCK = 60 MHz, HS = 1, AVGS = 0111)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][11]	—	82.4	—	dB	187.5 kS/s (FADCK = 60 MHz, HS = 1, AVGS = 0100)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][11]	—	77.6	—	dB	750 kS/s (FADCK = 60MHz, HS = 1, AVGS = 0010)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][11]	—	72.2	—	dB	3.0 MS/s (FADCK = 60 MHz, HS = 1, AVGS = 0000)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][11]	—	69.8	—	dB	0.94 MS/s (FADCK = 60 MHz, HS = 1, AVGS = 0010)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][11]	—	67.4	—	dB	3.75 MS/s (FADCK = 60 MHz, HS = 1, AVGS = 0000)
SFDR	Spurious free dynamic range [9][11]	—	88.0	—	dB	12b/16b Mode, 1 kHz input, AVGS = 0010

Table continues on the next page...

Table 31. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
SFDR	Spurious free dynamic range [9] [11]	—	82.0	—	dB	12b/16b Mode, 1 kHz input, AVGS = 0000
tADCSTUP	Start-up time [12]	5	—	—	µs	—
E_TS	Temperature sensor error [13]	—	±1	±3	˚C	Tj = -40 to 105 ˚C
E_TS	Temperature sensor error [13]	—	±2	±4	˚C	Tj = -40 to 125 ˚C
A	Temp Sensor Slope Constant [14]	—	738.00	—	˚C	—
B	Temp Sensor Offset Constant [14]	—	287.50	—	˚C	—
α	Temp Sensor Bandgap Constant [14]	—	10.06	—	˚C	—

[1] The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 22.5 MHz, and 60 MHz. For lowest power operation, PWRSEL should be set to 0.
[2] Must meet minimum TSMP requirement
[3] fADCK = 60 MHz (HS Mode)
[4] Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula: TSMP_REQ = B*ln(2)*[RAS*(CAS+CP+CADIN)+ (RAS + RIOMUX + RADIN)* CADIN(typ). RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO”
[5] Min based on 3.5 cycles
[6] Min based on 3.5 cycles at 60 MHz
[7] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
[8] 1 LSB = (VREFH - VREFL)/2N (N = 14 bits), for 16- bit specifications, multiply by 4.
[9] All accuracy numbers assume that the ADC is calibrated with VREFH=VDD_ANA and using a high- speed- dedicated input channel. Typical values assume VDD_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, sample time of 3.5 ADCK cycles (CMDHn[STS]=0h) u nless otherwise stated. Typical values are for reference only, and are not tested in production.
[10] Guaranteed by characterization
[11] Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
[12] Delay required if PWREN=0. Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
[13] The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber
[14] T(°C) = A*[α(Vbe8 - Vbe1)/(Vbe8 + α(Vbe8 - Vbe1))] - B where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor, α is the bandgap coefficient

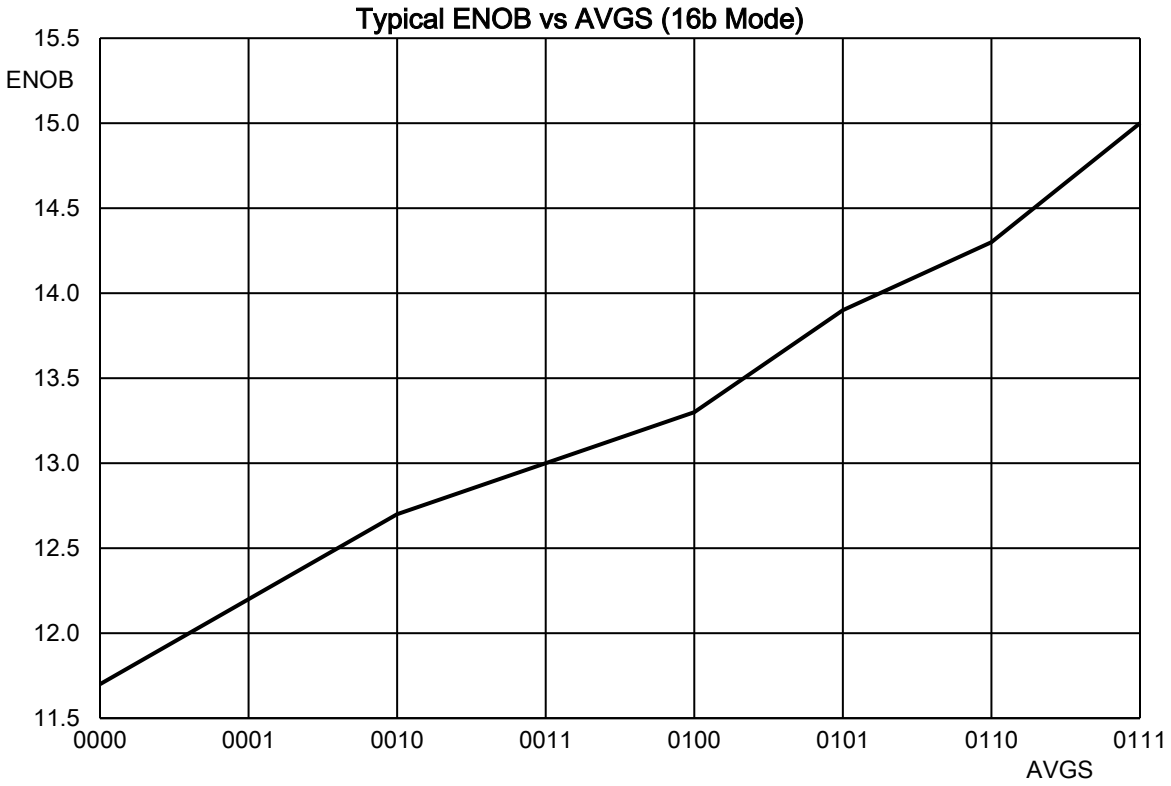


Figure 10. ENOB vs Averaging (16b HS Mode)

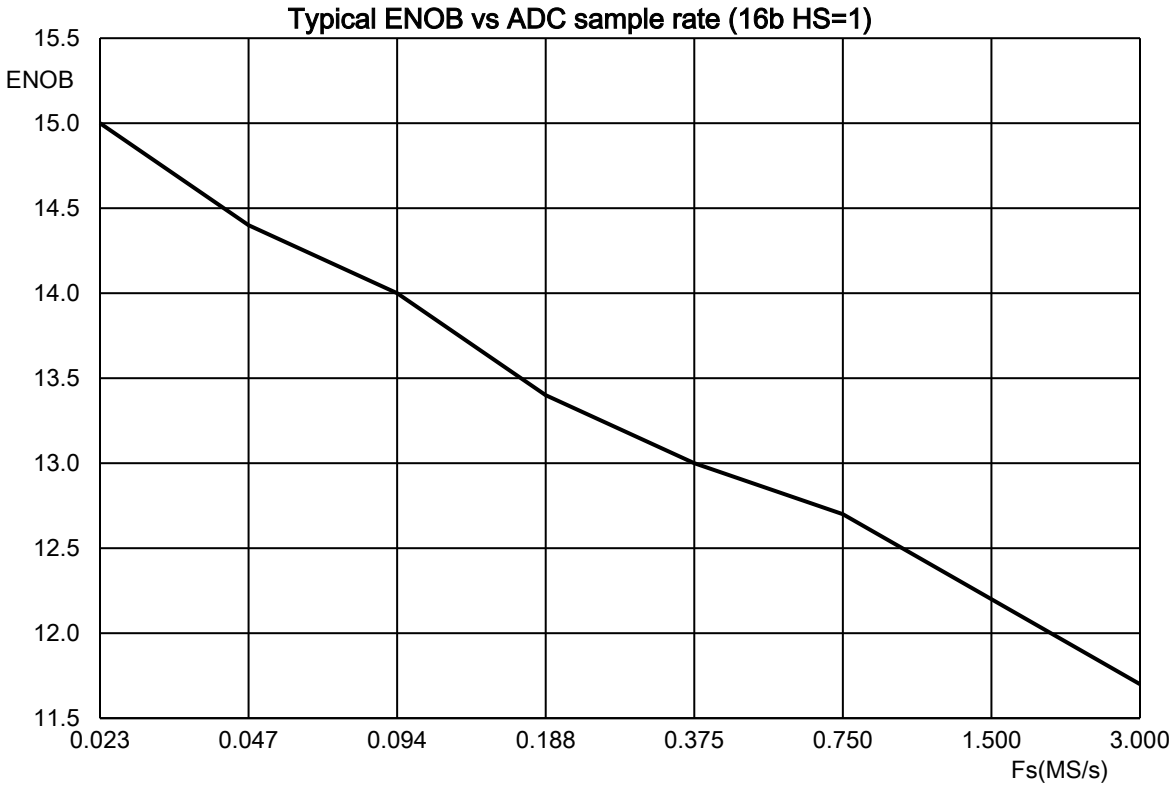


Figure 11. ENOB vs ADC sample rate

4.4.1.2.1 I/O mux resistance table

Table 32. I/O mux resistance table

Symbol	Description	Min	Typ	Max	Unit	Condition
RIOMUX	I/O MUX Resistance	—	—	5.35	kΩ	VDD ≥ 1.71v
RIOMUX	I/O MUX Resistance	—	—	1	kΩ	VDD ≥ 2.1v
RIOMUX	I/O MUX Resistance	—	0.35	0.66	kΩ	VDD ≥ 2.5 v

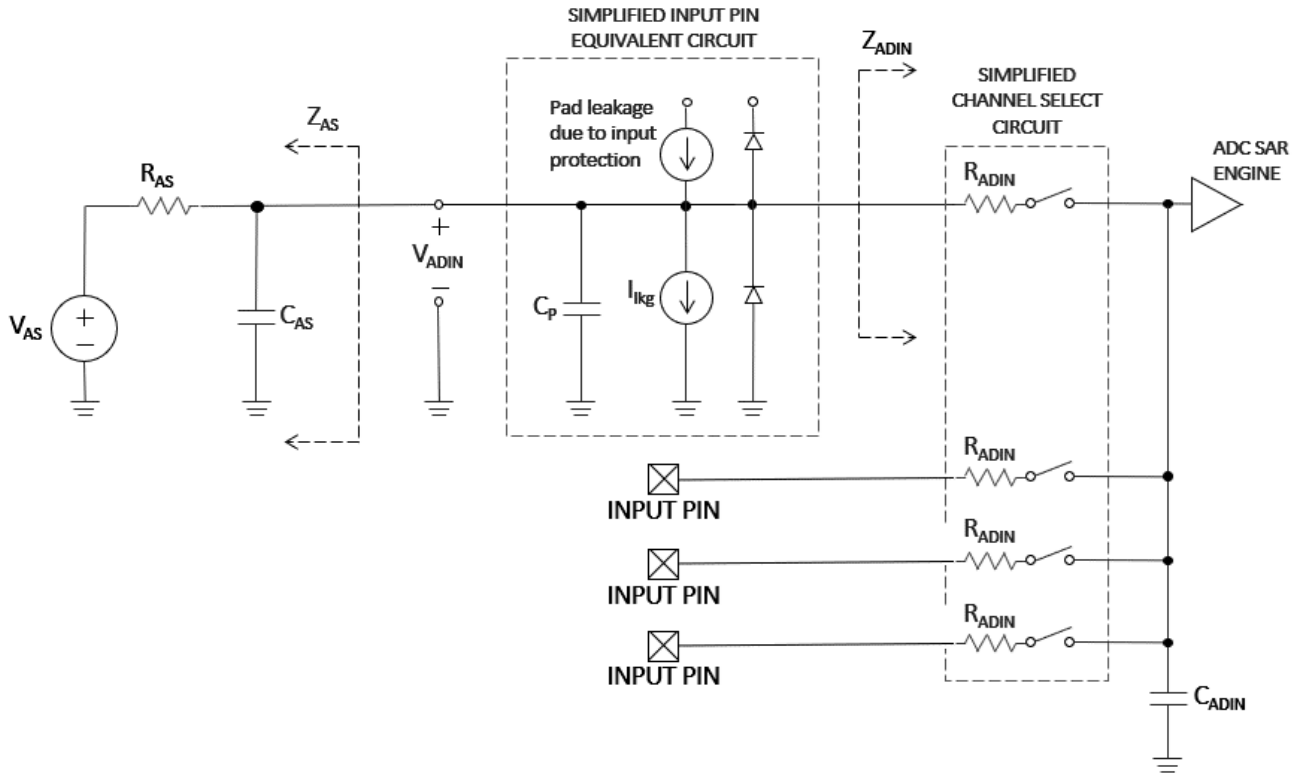


Figure 12. ADC input impedance equivalency diagram

4.4.1.3 Comparator and 8-bit DAC electrical specifications

Table 33. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	—
IDD_CMP	Supply current	—	200	—	µA	High speed mode (EN=1, HPMD=1)
IDD_CMP	Supply current	—	10	—	µA	Normal mode (EN=1, HPMD=0, NPMD=0)
IDD_CMP	Supply current	—	400	—	nA	Low-power mode (EN=1, HPMD=0, NPMD=1)
VAIN	Analog input voltage	VSS	—	VDD	V	—
VAIO	Analog input offset voltage	—	—	20	mV	High speed mode
VAIO	Analog input offset voltage	—	—	20	mV	Normal mode

Table continues on the next page...

Table 33. Comparator and 8-bit DAC electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VAIO	Analog input offset voltage	—	—	40	mV	Low-power mode
VH	Analog comparator hysteresis [1]	—	0	—	mV	CR0[HYSTCTR] = 00
VH	Analog comparator hysteresis [1]	—	10	—	mV	CR0[HYSTCTR] = 01
VH	Analog comparator hysteresis [1]	—	20	—	mV	CR0[HYSTCTR] = 10
VH	Analog comparator hysteresis [1]	—	30	—	mV	CR0[HYSTCTR] = 11
VCMPOh	Output high	VDD - 0.2	—	—	V	—
VCMPOl	Output low	—	—	0.2	V	—
tD	Propagation delay [2]	—	—	25	ns	High speed mode, 100 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	50	ns	High speed mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	600	ns	Normal mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	5	µs	Low-power mode, 30 mV overdrive, power > 1.71V
tinit	Analog comparator initialization delay [3]	—	—	40	µs	—
IDAC8b	8-bit DAC current adder (enabled)	—	10	—	µA	High power mode (EN=1, PMODE=1)
IDAC8b	8-bit DAC current consumption	—	1	—	µA	Low power mode (EN=1, PMODE=0)
INL	8-bit DAC integral non-linearity [4]	-1	—	+1.0	LSB	Low/High power mode, supply power > 1.71V
DNL	8-bit DAC differential non-linearity	-1	—	+1.0	LSB	Low/High power mode, power > 1.71V

[1] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
[2] Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part
[3] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
[4] 1 LSB = Vreference/256

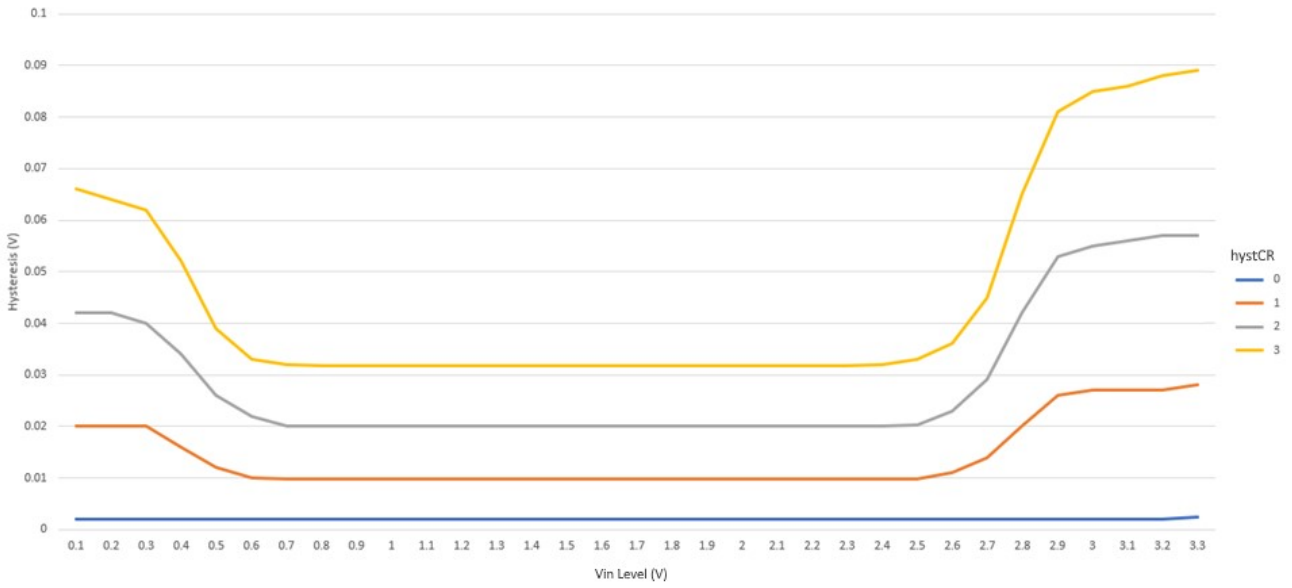


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

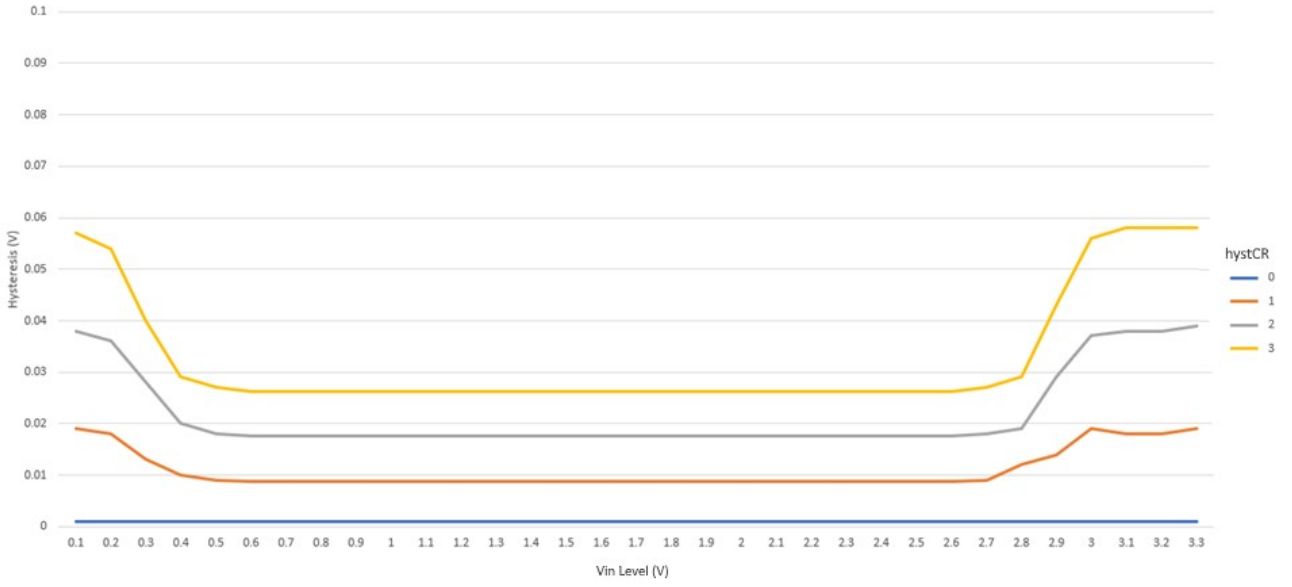


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

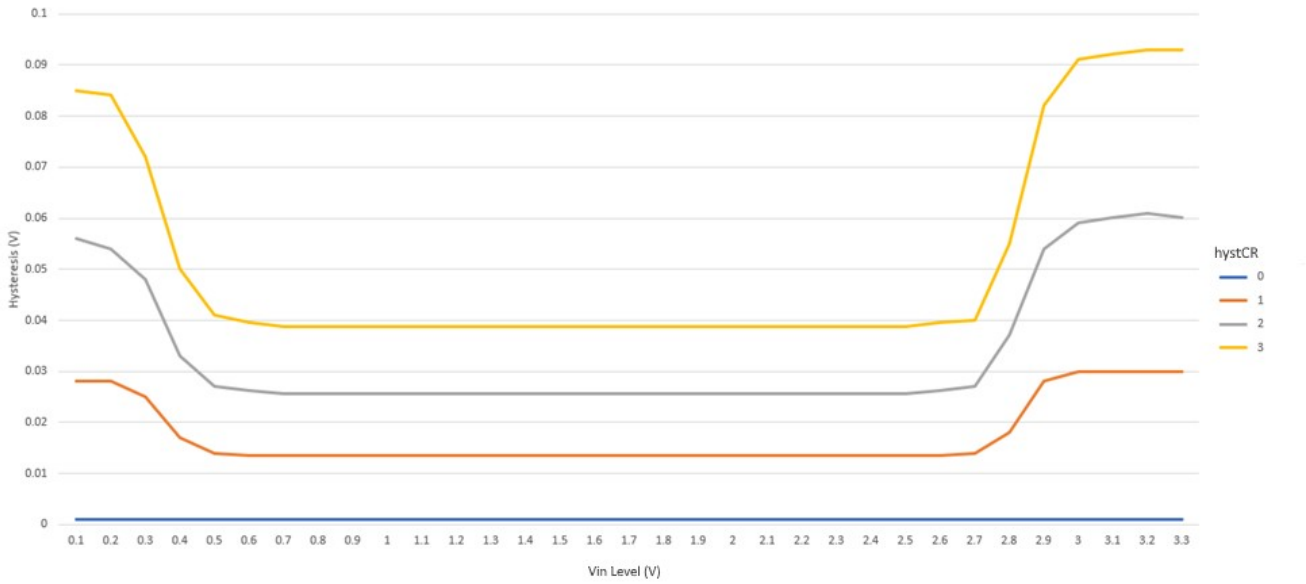


Figure 15. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

4.4.1.4 OpAmp electrical specifications

Table 34. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
TJ	Operation temperature	-40	25	125	°C	—
Vvdda	Analog supply voltage	1.71	3	3.6	V	—
Vvdd	Digital supply voltage	0.9	1.1	1.21	V	—

General

Table 35. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdda	Analog supply current	—	500	—	µA	—
Cin	Input capacitance	—	—	5	pF	—
Cload	Load capacitance	—	—	20	pF	—
Rload	Load resistance	3	—	20	KΩ	—
Vcm	Input common mode voltage range	0	—	Vvdda-1	V	—
Vout	Output voltage range	0.15	—	Vvdda - 0.15	V	—

Table continues on the next page...

Table 35. OpAmp electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Ishuntdown_3v	Leakage current for vdda_3v pin	—	1	80	nA	When Vvdda = 3V
Vos	Input offset voltage	-7	0	7	mV	—
CMRR	Input common mode rejection ratio	—	80	—	dB	—
PSRR	Power supply rejection ratio	—	80	—	dB	—
UGB	Unity gain bandwidth	—	8	—	MHz	CC config=2'b00, gain=2
UGB	Unity gain bandwidth	—	16	—	MHz	CC config=2'b01, gain=4
UGB	Unity gain bandwidth	—	32	—	MHz	CC config=2’b10, gain=8
UGB	Unity gain bandwidth	—	64	—	MHz	CC config=2'b11, gain=16
Av	DC open loop voltage gain	-	95	-	dB	—
PM	Phase marge	-	60	-	deg	—
Tsettle	Settling time	-	450	-	ns	—
SR	Slew rate	-	10	-	V/us	—
Vn	Voltage noise density @1KHz	—	150	—	nV/ sqrtHz	Gain = 1
Zout	Closed-loop output impedance	—	1.703	—	Ohm	cc config=2’b00, f = 200KHz
Zout	Closed-loop output impedance	—	14.72	—	Ohm	cc config=2’b01, f = 200KHz
Zout	Closed-loop output impedance	—	8.514	—	Ohm	cc config=2’b00, f = 1MHz
Zout	Closed-loop output impedance	—	73.47	—	Ohm	cc config=2’b01, f = 1MHz

4.5 Timers

See General switching specifications.

4.6 Communication Interfaces

4.6.1 LPUART

See General switching specifications.

4.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

4.6.2.1 LPSPI controller mode timing

Table 36. LPSPI controller mode timing

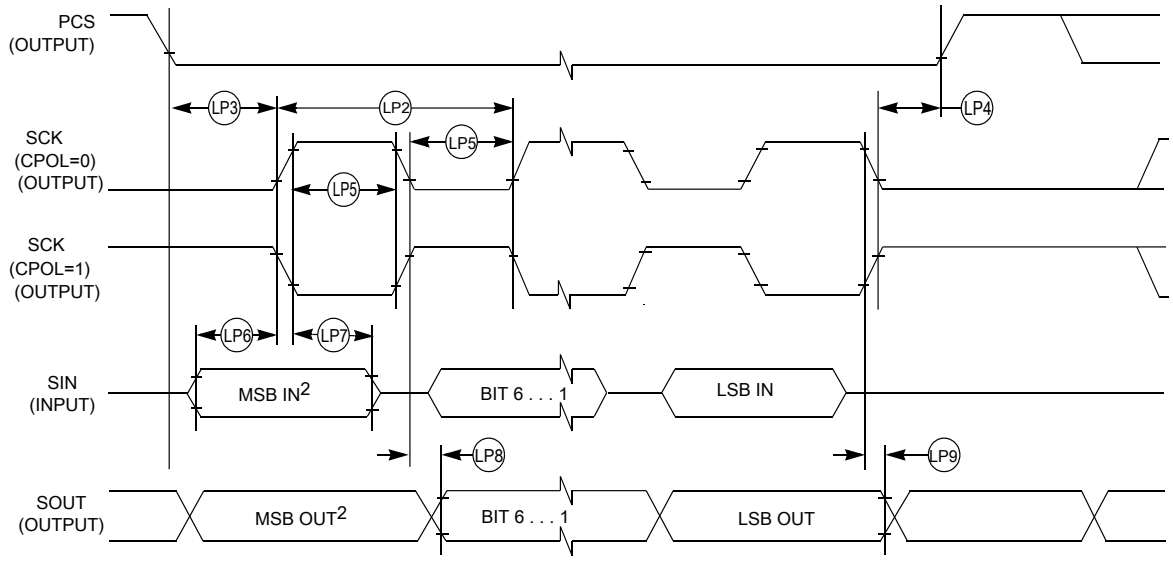
Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation [1]	—	—	—	MHz	—
LP1	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	50	MHz	Controller in OD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	25	MHz	Controller in OD mode
LP1	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	25	MHz	Controller in MD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	25	MHz	Controller in MD mode
LP2	SPSCK period	1000/LP1	—	—	ns	—
LP3	Enable lead time [3]	1/2	—	—	tperiph	—
LP4	Enable lag time [3]	1/2	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSCK/2-3	—	tSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	4.2	ns	Controller in OD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	4.4	ns	Controller in OD mode
LP6	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	5.4	ns	Controller in MD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	5.4	ns	Controller in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	LPSPI0 ~ LPSPI1 medium speed pad [2]	0	—	—	ns	Controller in OD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad [2]	0	—	—	ns	Controller in OD mode
LP7	LPSPI0 ~ LPSPI1 medium speed pad [2]	0	—	—	ns	Controller in MD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad [2]	0	—	—	ns	Controller in MD mode
LP8	Data valid (after SPSCK edge)	—	—	—	ns	—
LP8	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	6.4	ns	Controller in OD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	12.8	ns	Controller in OD mode

Table continues on the next page...

Table 36. LPSPI controller mode timing*...continued*

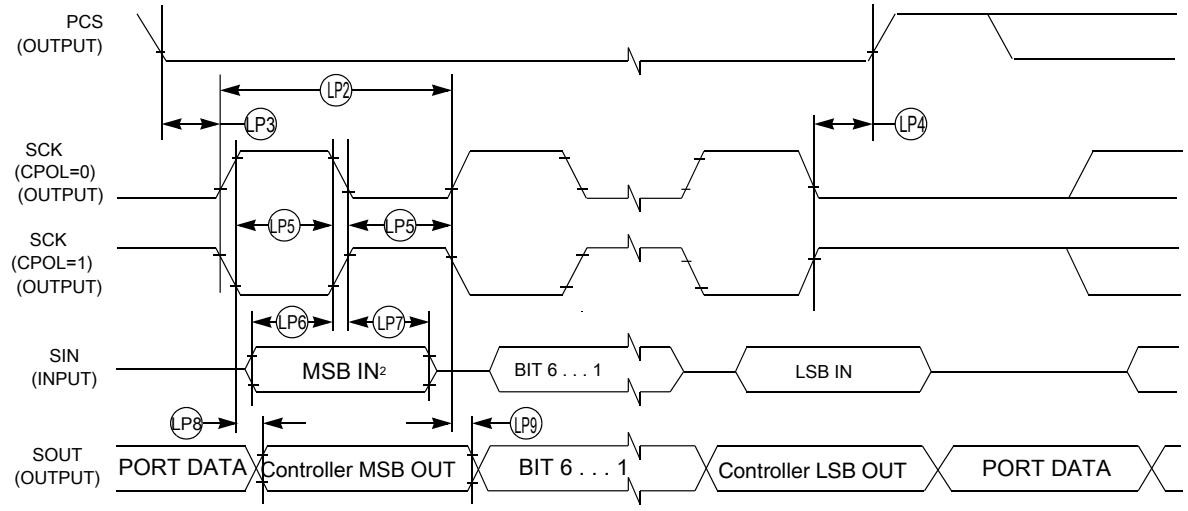
Symbol	Description	Min	Typ	Max	Unit	Condition
LP8	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	13.6	ns	Controller in MD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	13.6	ns	Controller in MD mode
LP9	Data hold time (outputs)	—	—	—	ns	—
LP9	LPSPI0 ~ LPSPI1 slow speed pad [2]	-1	—	—	ns	Controller in OD mode
LP9	LPSPI0 ~ LPSPI1 medium speed pad [2]	-1	—	—	ns	Controller in OD mode
LP9	LPSPI0 ~ LPSPI1 medium speed pad [2]	-1	—	—	ns	Controller in MD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad [2]	-1	—	—	ns	Controller in MD mode

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LPSPI peripheral functional clock.
[2] OD mode is MCU at Over drive mode, MD mode is MCU at Middle drive mode.
[3] tperiph = 1/fperiph



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. LPSPI controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. LPSPI controller mode timing (CPHA = 1)

4.6.2.2 LPSPI peripheral mode timing

Table 37. LPSPI peripheral mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation in OD mode [1]	—	—	—	—	—
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	25	MHz	Peripheral Tx in OD mode
LP1	lpspi0~lpspi1 slow speed pad [1]	—	—	12.5	MHz	Peripheral Tx in OD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	50	MHz	Peripheral Rx in OD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	25	MHz	Peripheral Rx in OD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Peripheral Tx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Peripheral Tx in MD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Peripheral Rx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Peripheral Rx in MD mode
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time [2]	1	—	—	tperiph	—

Table continues on the next page...

Table 37. LPSPI peripheral mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK/ 2 - 5	—	tSPSCK/ 2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	lpspi0~lpspi1 medium speed pad	—	—	3.6	ns	Peripheral Rx in OD mode
LP6	lpspi0~lpspi1 slow speed pad	—	—	7.2	ns	Peripheral Rx in OD mode
LP6	lpspi0~lpspi1 medium speed pad	—	—	12.8	ns	Peripheral Rx in MD mode
LP6	lpspi0~lpspi1 slow speed pad	—	—	12.8	ns	Peripheral Rx in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Peripheral Rx in OD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Peripheral Rx in OD mode
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Peripheral Rx in MD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Peripheral Rx in MD mode
LP8	Peripheral access time [2][3]	—	—	tperiph	ns	—
LP9	Peripheral MISO disable time [2] [4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	—	ns	—
LP10	lpspi0~lpspi1 medium speed pad	—	—	15.6	ns	Peripheral Tx in OD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	—	Peripheral Tx in OD mode
LP10	lpspi0~lpspi1 medium speed pad	—	—	29.2	ns	Peripheral Tx in MD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	29.2	ns	Peripheral Tx in MD mode
LP11	Data hold time (outputs)	—	—	—	ns	—
LP11	lpspi0~lpspi1 medium speed pad	2	—	—	ns	Peripheral Tx in OD mode
LP11	lpspi0~lpspi1 slow speed pad	2	—	—	ns	Peripheral Tx in OD mode

Table continues on the next page...

Table 37. LPSPI peripheral mode timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP11	lpspi0~lpspi1 medium speed pad	2	—	—	ns	Peripheral Tx in MD mode
LP11	lpspi0~lpspi1 slow speed pad	2	—	—	ns	Peripheral Tx in MD mode

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/4, where fperiph is the LPSPI peripheral functional clock.
[2] tperiph = 1/fperiph
[3] Time to data active from high-impedance state
[4] Hold time to high-impedance state

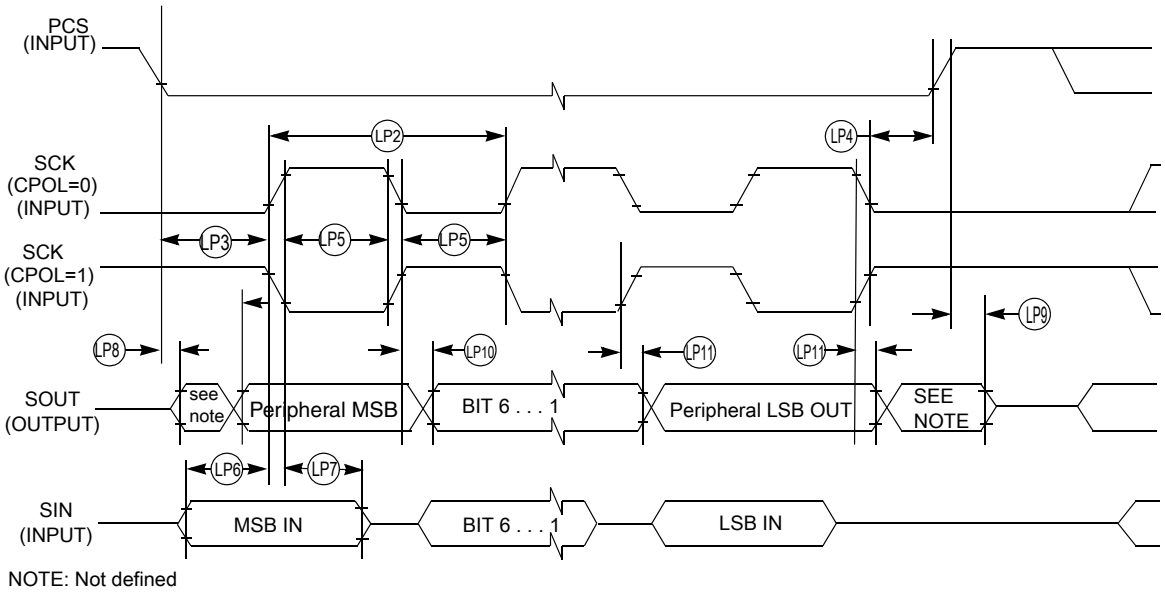


Figure 18. LPSPI peripheral mode timing (CPHA = 0)

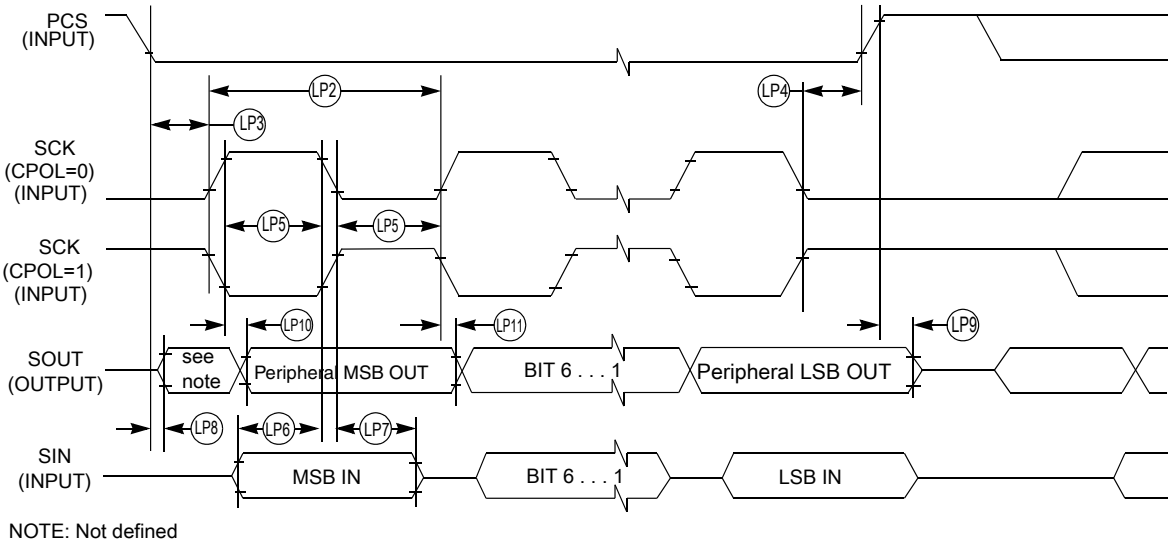


Figure 19. LPSPI peripheral mode timing (CPHA = 1)

4.6.3 LPI2C timing

Table 38. LPI2C timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency in standard mode	0	—	100	kHz	—
fSCL	SCL Clock Frequency in fast mode	0	—	400	kHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode	4	—	—	µs	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode	0.6	—	—	µs	—
tLOW	LOW period of the SCL clock in standard mode	4.7	—	—	µs	—
tLOW	LOW period of the SCL clock in fast mode	1.25	—	—	µs	—
tHIGH	HIGH period of the SCL clock in standard mode	4	—	—	µs	—
tHIGH	HIGH period of the SCL clock in fast mode	0.6	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in standard mode	4.7	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in fast mode	0.6	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices in standard mode [1][2]	0	—	3.45	µs	—
tHD; DAT	Data hold time for I2C bus devices in fast mode [1][3]	0	—	0.9	µs	—
tSU; DAT	Data set-up time in standard mode [4]	250	—	—	ns	—
tSU; DAT	Data set-up time in fast mode [2][5]	100A	—	—	ns	—
tr	Rise time of SDA and SCL signals in standard mode [6]	—	—	1000	ns	—
tr	Rise time of SDA and SCL signals in fast mode [6]	20 +0.1Cb	—	300	ns	—
tf	Fall time of SDA and SCL signals in standard mode [5]	—	—	300	ns	—

Table continues on the next page...

Table 38. LPI2C timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tf	Fall time of SDA and SCL signals in fast mode [5]	20 +0.1Cb	—	300	ns	—
tSU; STO	Set-up time for STOP condition in standard mode	4	—	—	µs	—
tSU; STO	Set-up time for STOP condition in fast mode	0.6	—	—	µs	—
tBUF	Bus free time between STOP and START condition in standard mode	4.7	—	—	µs	—
tBUF	Bus free time between STOP and START condition in fast mode	1.3	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter in standard mode	N/A	—	N/A	ns	—
tSP	Pulse width of spikes that must be suppressed by the input filter in fast mode	0	—	50	ns	—

[1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[2] The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal
[3] Input signal Slew = 10 ns and Output Load = 50 pF
[4] Set-up time in target-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[5] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
[6] Cb = total capacitance of the one bus line in pF.

4.6.4 I2C 1 Mbps timing

Table 39. I2C 1 Mbps timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	1	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	HIGH period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices	0	—	—	µs	—
tSU; DAT	Data set-up time	50	—	—	ns	—

Table continues on the next page...

Table 39. I2C 1 Mbps timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tr	Rise time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tSU; STO	Set-up time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] Cb = total capacitance of the one bus line in pF for maximum value

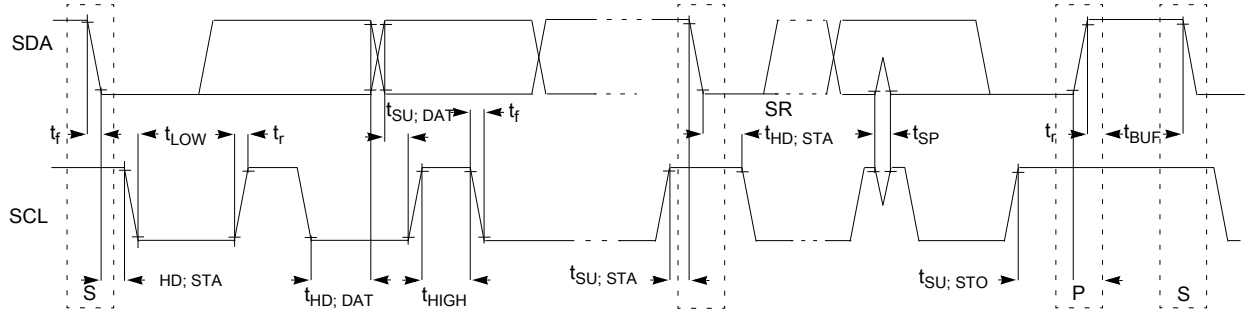


Figure 20. Timing definition for devices on the I2C bus

4.6.5 I2C HS mode timing

Table 40. I2C HS mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	3.4	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	High period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices [1]	0	—	—	µs	—
tSU; DAT	Data setup time	34	—	—	ns	—
tr	Rise time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—

Table continues on the next page...

Table 40. I2C HS mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tf	Fall time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tSU; STO	Setup time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.
[2] Cb = total capacitance of the one bus line in pF. The typical Cb value is 20 pF

4.6.6 FlexCAN

See General switching specifications.

4.7 Human Machine Interface (HMI) modules

4.7.1 General Purpose Input/Output (GPIO)

See General switching specifications.

5 Package dimensions

5.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

Table 41. Obtaining package dimensions

If you want the drawing for this package	Then use this document number
LQFP100	98ASS23308W
LQFP64	98ASS23234W
LQFP48	98ASH00962A
H-PQFN32	98ASA02110D

6 Pinout

6.1 MCX A173, A174 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the "Pinout" tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, the pinout table is as given below

Table 42. Pinmux

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
P1_8	1	2	1	1	**ALT0** - P1_8 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPUART1_RXD **ALT3** - LPI2C0_SDA **ALT4** - CT_INP8 **ALT5** - CT0_MAT2 **ALT7** - SMARTDMA_PIO4	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ISP** - I2C_SDA **VDD SYS** - WUU0_IN10
P1_9	2	3	2	2	**ALT0** - P1_9 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPUART1_TXD **ALT3** - LPI2C0_SCL **ALT4** - CT_INP9 **ALT5** - CT0_MAT3 **ALT7** - SMARTDMA_PIO5	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ISP** - I2C_SCL
P1_10	3	4	--	--	**ALT0** - P1_10 **ALT2** - LPUART1_RTS_B **ALT3** - LPI2C0_SDAS **ALT4** - CT2_MAT0 **ALT7** - SMARTDMA_PIO6 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A8
P1_11	4	5	--	--	**ALT0** - P1_11 **ALT1** - TRIG_OUT2 **ALT2** - LPUART1_CTS_B **ALT3** - LPI2C0_SCLS **ALT4** - CT2_MAT1 **ALT7** - SMARTDMA_PIO7 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A9 **VDD SYS** - WUU0_IN11
P1_12	5	6	--	--	**ALT0** - P1_12 **ALT2** - LPI2C1_SDA	**IO Supply** - VDD **Pad type** - SLOW	**ANALOG** - ADC1_A10 **VDD SYS** - WUU0_IN12

Table continues on the next page...

Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT3 - LPUART2_RXD **ALT4** - CT2_MAT2 **ALT7** - SMARTDMA_PIO8 **ALT11** - CAN0_RXD	**Default** - DIS	
P1_13	6	7	--	--	**ALT0** - P1_13 **ALT1** - TRIG_IN3 **ALT2** - LPI2C1_SCL **ALT3** - LPUART2_TXD **ALT4** - CT2_MAT3 **ALT7** - SMARTDMA_PIO9 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A11
P1_14	7	--	--	--	**ALT0** - P1_14 **ALT2** - LPI2C1_SCLS **ALT3** - LPUART2_RTS_B **ALT7** - SMARTDMA_PIO10	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A12
P1_15	8	--	--	--	**ALT0** - P1_15 **ALT2** - LPI2C1_SDAS **ALT3** - LPUART2_CTS_B **ALT7** - SMARTDMA_PIO11	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A13 **VDD SYS** - WUU0_IN13
P1_29	9	8	3	3	**ALT0** - P1_29 **ALT1** - RESET_B **ALT2** - SPC_LPREQ	**IO Supply** - VDD **Pad type** - RST **Default** - ALT1	**VDD SYS** - RESET_B
P1_30	10	9	4	4	**ALT0** - P1_30 **ALT1** - TRIG_OUT3 **ALT3** - LPI2C0_SDA **ALT4** - CT_INP16	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - XTAL48M
P1_31	11	10	5	5	**ALT0** - P1_31 **ALT1** - TRIG_IN4 **ALT3** - LPI2C0_SCL **ALT4** - CT_INP17	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - EXTAL48M
VSS	12	11	6	0		**IO Supply** - VDD	
VSS	12	11	6	0		**IO Supply** - VDD	

Table continues on the next page...

Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
VREFH	13	12	7	6		**IO Supply** - VDD	
VDD_ANA	14	12	7	6		**IO Supply** - VDD	
VDD	15	13	8	7		**IO Supply** - VDD	
P4_2	16	--	--	--	**ALT0** - P4_2 **ALT1** - CLKOUT **ALT3** - LPUART3_RXD **ALT5** - PWM0_A2 **ALT7** - SMARTDMA_PIO22	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN16
P4_3	17	--	--	--	**ALT0** - P4_3 **ALT5** - PWM0_B2 **ALT7** - SMARTDMA_PIO23	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_4	18	--	--	--	**ALT0** - P4_4 **ALT5** - PWM0_A1 **ALT7** - SMARTDMA_PIO24	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN17
P4_5	19	--	--	--	**ALT0** - P4_5 **ALT1** - TRIG_OUT3 **ALT3** - LPUART3_TXD **ALT5** - PWM0_B1 **ALT7** - SMARTDMA_PIO25	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_6	20	--	--	--	**ALT0** - P4_6 **ALT1** - TRIG_IN4 **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_A0 **ALT7** - SMARTDMA_PIO26	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_7	21	--	--	--	**ALT0** - P4_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT5** - PWM0_B0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	

Table continues on the next page...

Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SMARTDMA_PIO27		
P2_0	22	14	9	--	**ALT0** - P2_0 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RXD **ALT4** - CT_INP16 **ALT5** - CT2_MAT0 **ALT7** - SMARTDMA_PIO24	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A0 **VDD SYS** - WUU0_IN18
P2_1	23	15	10	--	**ALT0** - P2_1 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_TXD **ALT4** - CT_INP17 **ALT5** - CT2_MAT1 **ALT7** - SMARTDMA_PIO25	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A0
P2_2	24	16	11	8	**ALT0** - P2_2 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RTS_B **ALT3** - LPUART2_TXD **ALT4** - CT_INP12 **ALT5** - CT2_MAT2 **ALT7** - SMARTDMA_PIO26	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ISP** - UART_TXD **ANALOG** - ADC0_A4/ CMP0_IN0/CMP1_INN4
P2_3	25	17	12	9	**ALT0** - P2_3 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_CTS_B **ALT3** - LPUART2_RXD **ALT4** - CT_INP13 **ALT5** - CT2_MAT3 **ALT7** - SMARTDMA_PIO27	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ISP** - UART_RXD **ANALOG** - ADC0_A3/ CMP1_IN0/ADC1_A4 **VDD SYS** - WUU0_IN19
P2_4	26	18	--	--	**ALT0** - P2_4 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP14 **ALT5** - CT1_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A1

Table continues on the next page...

Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SMARTDMA_PIO28		
P2_5	27	19	--	--	**ALT0** - P2_5 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP15 **ALT5** - CT1_MAT1 **ALT7** - SMARTDMA_PIO29	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A1
P2_6	28	20	13	--	**ALT0** - P2_6 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_PCS1 **ALT4** - CT_INP18 **ALT5** - CT1_MAT2 **ALT7** - SMARTDMA_PIO30	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A3
P2_7	29	21	14	10	**ALT0** - P2_7 **ALT1** - TRIG_IN5 **ALT4** - CT_INP19 **ALT5** - CT1_MAT3 **ALT7** - SMARTDMA_PIO31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - VREFI/ ADC0_A7/ADC1_A7
P2_10	30	--	--	--	**ALT0** - P2_10 **ALT1** - TRIG_OUT5 **ALT3** - LPUART2_TXD **ALT7** - SMARTDMA_PIO14	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_11	31	--	--	--	**ALT0** - P2_11 **ALT1** - TRIG_IN4 **ALT3** - LPUART2_RXD **ALT7** - SMARTDMA_PIO15	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VSS	32	--	--	0		**IO Supply** - VDD	
VDD	33	--	--	--		**IO Supply** - VDD	
P2_12	34	22	15	11	**ALT0** - P2_12 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A5/OPAMP0_INP **VDD SYS** - WUU0_IN20

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT5 - CT0_MAT0 **ALT7** - SMARTDMA_PIO16 **ALT11** - CAN0_RXD		
P2_13	35	23	16	12	**ALT0** - P2_13 **ALT1** - TRIG_IN8 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_TXD **ALT5** - CT0_MAT1 **ALT7** - SMARTDMA_PIO17 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A5/OPAMP0_INN
P2_15	36	24	17	13	**ALT0** - P2_15 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT5** - CT0_MAT2 **ALT7** - SMARTDMA_PIO18	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_OUT/ ADC0_A2/ CMP0_INP4**VDD SYS** - WUU0_IN21
P2_16	37	25	18	--	**ALT0** - P2_16 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT5** - CT0_MAT2 **ALT7** - SMARTDMA_PIO19	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A6
P2_17	38	26	19	14	**ALT0** - P2_17 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT5** - CT0_MAT3 **ALT7** - SMARTDMA_PIO20	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A6
P2_19	39	27	20	--	**ALT0** - P2_19 **ALT1** - TRIG_OUT5 **ALT7** - SMARTDMA_PIO21	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A2/CMP1_INP4
P2_20	40	--	--	--	**ALT0** - P2_20	**IO Supply** - VDD	

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT1 - TRIG_IN8 **ALT2** - LPSPI1_PCS2 **ALT4** - CT2_MAT0 **ALT7** - SMARTDMA_PIO22	**Pad type** - SLOW **Default** - DIS	
P2_21	41	--	--	--	**ALT0** - P2_21 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS3 **ALT4** - CT2_MAT1 **ALT7** - SMARTDMA_PIO23	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_23	42	--	--	--	**ALT0** - P2_23 **ALT1** - TRIG_OUT5 **ALT4** - CT2_MAT3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_24	43	--	--	--	**ALT0** - P2_24 **ALT1** - TRIG_OUT6 **ALT4** - CT_INP8	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_25	44	--	--	--	**ALT0** - P2_25 **ALT1** - TRIG_OUT7 **ALT4** - CT_INP9	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_26	45	--	--	--	**ALT0** - P2_26 **ALT1** - TRIG_IN5 **ALT4** - CT_INP10	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VSS	46	28	21	0		**IO Supply** - VDD	
VDD	47	29	22	--		**IO Supply** - VDD	
P3_31	48	30	23	--	**ALT0** - P3_31 **ALT1** - TRIG_IN10 **ALT2** - LPI2C1_SDAS **ALT4** - CT0_MAT3 **ALT7** - PWM1_B0 **ALT10** - SMARTDMA_PIO31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A20 **VDD SYS** - LPTMR0_ALT2
P3_30	49	31	24	--	**ALT0** - P3_30 **ALT1** - TRIG_OUT6 **ALT2** - LPI2C1_SCLS	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A21

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT4 - CT0_MAT2 **ALT7** - PWM1_A0 **ALT10** - SMARTDMA_PIO30		
P3_29	50	32	25	15	**ALT0** - P3_29 **ALT1** - ISPMODE_N **ALT2** - LPI2C1_HREQ **ALT4** - CT_INP3 **ALT10** - SMARTDMA_PIO29	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - ADC1_A22 **VDD SYS** - WUU0_IN27
P3_28	51	33	26	16	**ALT0** - P3_28 **ALT1** - TRIG_IN11 **ALT2** - LPI2C1_SDA **ALT4** - CT_INP12 **ALT7** - PWM1_B3 **ALT10** - SMARTDMA_PIO28	**IO Supply** - VDD **Pad type** - 5VTOL **Default** - DIS	**VDD SYS** - WUU0_IN26
P3_27	52	34	27	17	**ALT0** - P3_27 **ALT1** - TRIG_OUT7 **ALT2** - LPI2C1_SCL **ALT4** - CT_INP13 **ALT7** - PWM1_A3 **ALT10** - SMARTDMA_PIO27	**IO Supply** - VDD **Pad type** - 5VTOL **Default** - DIS	**VDD SYS** - WUU0_IN30
P3_22	53	--	--	--	**ALT0** - P3_22 **ALT3** - LPUART1_RTS_B **ALT4** - CT_INP10 **ALT7** - PWM1_X2 **ALT10** - SMARTDMA_PIO22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_21	54	--	--	--	**ALT0** - P3_21 **ALT1** - TRIG_OUT1 **ALT3** - LPUART1_TXD **ALT4** - CT2_MAT3 **ALT5** - PWM0_X3 **ALT7** - PWM1_B3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT10 - SMARTDMA_PIO21		
P3_20	55	--	--	--	**ALT0** - P3_20 **ALT1** - TRIG_OUT0 **ALT3** - LPUART1_RXD **ALT4** - CT2_MAT2 **ALT5** - PWM0_X2 **ALT7** - PWM1_A3 **ALT10** - SMARTDMA_PIO20	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_19	56	--	--	--	**ALT0** - P3_19 **ALT4** - CT2_MAT1 **ALT5** - PWM0_X1 **ALT7** - PWM1_X1 **ALT10** - SMARTDMA_PIO19	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_18	57	--	--	--	**ALT0** - P3_18 **ALT4** - CT2_MAT0 **ALT5** - PWM0_X0 **ALT7** - PWM1_X0 **ALT10** - SMARTDMA_PIO18	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_17	58	--	--	--	**ALT0** - P3_17 **ALT4** - CT_INP9 **ALT7** - PWM1_B0 **ALT10** - SMARTDMA_PIO17	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_16	59	--	--	--	**ALT0** - P3_16 **ALT4** - CT_INP8 **ALT7** - PWM1_A0 **ALT10** - SMARTDMA_PIO16	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_15	60	35	--	--	**ALT0** - P3_15 **ALT2** - LPUART2_TXD **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT5** - PWM0_X3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - PWM1_B1 **ALT10** - SMARTDMA_PIO15		
P3_14	61	36	--	--	**ALT0** - P3_14 **ALT2** - LPUART2_RXD **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_X2 **ALT7** - PWM1_A1 **ALT10** - SMARTDMA_PIO14	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN25
P3_13	62	37	28	--	**ALT0** - P3_13 **ALT2** - LPUART2_CTS_B **ALT3** - LPUART3_RXD **ALT4** - CT1_MAT3 **ALT5** - PWM0_X1 **ALT7** - PWM1_B2 **ALT10** - SMARTDMA_PIO13	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_12	63	38	29	--	**ALT0** - P3_12 **ALT2** - LPUART2_RTS_B **ALT3** - LPUART3_TXD **ALT4** - CT1_MAT2 **ALT5** - PWM0_X0 **ALT7** - PWM1_A2 **ALT10** - SMARTDMA_PIO12	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VSS	64	--	--	0		**IO Supply** - VDD	
VDD	65	--	--	--		**IO Supply** - VDD	
P3_11	66	39	30	18	**ALT0** - P3_11 **ALT1** - TRIG_IN6 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT1_MAT1 **ALT5** - PWM0_B2 **ALT10** - SMARTDMA_PIO11	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN24

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
P3_10	67	40	31	19	**ALT0** - P3_10 **ALT1** - TRIG_IN5 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RTS_B **ALT4** - CT1_MAT0 **ALT5** - PWM0_A2 **ALT10** - SMARTDMA_PIO10	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P3_9	68	41	32	20	**ALT0** - P3_9 **ALT1** - TRIG_IN4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_TXD **ALT4** - CT_INP5 **ALT5** - PWM0_B1 **ALT10** - SMARTDMA_PIO9	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P3_8	69	42	33	21	**ALT0** - P3_8 **ALT1** - TRIG_IN3 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_RXD **ALT4** - CT_INP4 **ALT5** - PWM0_A1 **ALT10** - SMARTDMA_PIO8 **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN23
P3_7	70	43	--	--	**ALT0** - P3_7 **ALT1** - TRIG_IN2 **ALT2** - LPSPI1_PCS2 **ALT3** - LPUART3_CTS_B **ALT5** - PWM0_B3 **ALT7** - PWM1_B0 **ALT10** - SMARTDMA_PIO7	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P3_6	71	44	--	--	**ALT0** - P3_6 **ALT1** - CLKOUT **ALT2** - LPSPI1_PCS3 **ALT3** - LPUART3_RTS_B	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT5 - PWM0_A3 **ALT7** - PWM1_A0 **ALT10** - SMARTDMA_PIO6 **ALT12** - FREQME_CLK_OUT1		
P3_1	72	45	34	22	**ALT0** - P3_1 **ALT1** - TRIG_IN1 **ALT3** - LPUART3_TXD **ALT4** - CT_INP17 **ALT5** - PWM0_B0 **ALT7** - PWM1_X1 **ALT10** - SMARTDMA_PIO1 **ALT12** - FREQME_CLK_OUT0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	
P3_0	73	46	35	23	**ALT0** - P3_0 **ALT1** - TRIG_IN0 **ALT3** - LPUART3_RXD **ALT4** - CT_INP16 **ALT5** - PWM0_A0 **ALT7** - PWM1_X0 **ALT10** - SMARTDMA_PIO0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**VDD SYS** - WUU0_IN22
VSS	74	47	36	0		**IO Supply** - VDD	
VDD	75	48	37	24		**IO Supply** - VDD	
P0_0	76	49	38	25	**ALT0** - P0_0 **ALT1** - TMS/SWDIO **ALT2** - LPUART0_RTS_B **ALT3** - LPSPI0_PCS0 **ALT4** - CT_INP0	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	
P0_1	77	50	39	26	**ALT0** - P0_1 **ALT1** - TCLK/SWCLK **ALT2** - LPUART0_CTS_B **ALT3** - LPSPI0_SDI **ALT4** - CT_INP1	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
P0_2	78	51	40	27	**ALT0** - P0_2 **ALT1** - TDO/SWO **ALT2** - LPUART0_RXD **ALT3** - LPSPI0_SCK **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP0	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	
P0_3	79	52	41	28	**ALT0** - P0_3 **ALT1** - TDI **ALT2** - LPUART0_TXD **ALT3** - LPSPI0_SDO **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP1 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ANALOG** - CMP1_IN1/ADC0_A14
P0_6	80	53	42	--	**ALT0** - P0_6 **ALT1** - ISPMODE_N **ALT2** - LPI2C0_HREQ **ALT3** - LPSPI0_PCS1 **ALT4** - CT_INP2 **ALT7** - SMARTDMA_PIO2 **ALT8** - CMP1_OUT **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - ADC0_A15
P0_14	81	--	--	--	**ALT0** - P0_14 **ALT4** - CT_INP2 **ALT5** - UTICK_CAP0 **ALT7** - SMARTDMA_PIO4	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P0_15	82	--	--	--	**ALT0** - P0_15 **ALT4** - CT_INP3 **ALT5** - UTICK_CAP1 **ALT7** - SMARTDMA_PIO5	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P0_16	83	54	43	--	**ALT0** - P0_16 **ALT2** - LPI2C0_SDA **ALT3** - LPSPI0_PCS2 **ALT4** - CT0_MAT0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**VDD SYS** - WUU0_IN2

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT5 - UTICK_CAP2 **ALT7** - SMARTDMA_PIO6		
P0_17	84	55	44	--	**ALT0** - P0_17 **ALT2** - LPI2C0_SCL **ALT3** - LPSPI0_PCS3 **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP3 **ALT7** - SMARTDMA_PIO7	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	
P0_18	85	--	--	--	**ALT0** - P0_18 **ALT2** - LPI2C0_SCLS **ALT4** - CT0_MAT2 **ALT7** - SMARTDMA_PIO8 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A8
P0_19	86	--	--	--	**ALT0** - P0_19 **ALT2** - LPI2C0_SDAS **ALT4** - CT0_MAT3 **ALT7** - SMARTDMA_PIO9 **ALT8** - CMP1_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A9 **VDD SYS** - WUU0_IN3
P0_20	87	--	--	--	**ALT0** - P0_20 **ALT3** - LPUART0_RXD **ALT4** - CT_INP0 **ALT7** - SMARTDMA_PIO10	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A10 **VDD SYS** - WUU0_IN4
P0_21	88	--	--	--	**ALT0** - P0_21 **ALT3** - LPUART0_TXD **ALT4** - CT_INP1 **ALT7** - SMARTDMA_PIO11	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A11
P0_22	89	--	--	--	**ALT0** - P0_22 **ALT3** - LPUART0_RTS_B **ALT4** - CT_INP2 **ALT5** - CT0_MAT0	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A12

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Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SMARTDMA_PIO12		
P0_23	90	--	--	--	**ALT0** - P0_23 **ALT3** - LPUART0_CTS_B **ALT4** - CT_INP3 **ALT5** - CT0_MAT1 **ALT7** - SMARTDMA_PIO13	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A13 **VDD SYS** - WUU0_IN5
P1_0	91	56	45	29	**ALT0** - P1_0 **ALT1** - TRIG_IN0 **ALT2** - LPSPI0_SDO **ALT3** - LPI2C1_SDA **ALT4** - CT_INP4 **ALT5** - CT0_MAT2	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SDO **ANALOG** - ADC0_A16/CMP0_IN3 **VDD SYS** - WUU0_IN6/ LPTMR0_ALT3
P1_1	92	57	46	30	**ALT0** - P1_1 **ALT1** - TRIG_IN1 **ALT2** - LPSPI0_SCK **ALT3** - LPI2C1_SCL **ALT4** - CT_INP5 **ALT5** - CT0_MAT3	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SCK **ANALOG** - ADC0_A17/CMP1_IN3
P1_2	93	58	47	31	**ALT0** - P1_2 **ALT1** - TRIG_OUT0 **ALT2** - LPSPI0_SDI **ALT3** - LPI2C1_SDAS **ALT4** - CT1_MAT0 **ALT5** - CT_INP0 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - SPI_SDI **ANALOG** - ADC0_A18
P1_3	94	59	48	32	**ALT0** - P1_3 **ALT1** - TRIG_OUT1 **ALT2** - LPSPI0_PCS0 **ALT3** - LPI2C1_SCLS **ALT4** - CT1_MAT1 **ALT5** - CT_INP1 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - SPI_PCS **ANALOG** - ADC0_A19/CMP0_IN1 **VDD SYS** - WUU0_IN7
VDD	95	60	--	--		**IO Supply** - VDD	
VSS	96	61	--	0		**IO Supply** - VDD	

Table continues on the next page...

Table 42. Pinmux...*continued*

Pin Name	MCX A173A174 LQFP100	MCX A173A174 LQFP64	MCX A173A174 LQFP48	MCX A173A174 QFN32	Pinmux Assignment	Pad Settings	Alternate Functions
P1_4	97	62	--	--	**ALT0** - P1_4 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPSPI0_PCS3 **ALT3** - LPUART2_RXD **ALT4** - CT1_MAT2 **ALT7** - SMARTDMA_PIO0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A20/CMP0_IN2 **VDD SYS** - WUU0_IN8
P1_5	98	63	--	--	**ALT0** - P1_5 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPSPI0_PCS2 **ALT3** - LPUART2_TXD **ALT4** - CT1_MAT3 **ALT7** - SMARTDMA_PIO1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A21/CMP1_IN2
P1_6	99	64	--	--	**ALT0** - P1_6 **ALT1** - TRIG_IN2 **ALT2** - LPSPI0_PCS1 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP6 **ALT7** - SMARTDMA_PIO2 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A22
P1_7	100	1	--	--	**ALT0** - P1_7 **ALT1** - TRIG_OUT2 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP7 **ALT7** - SMARTDMA_PIO3 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A23 **VDD SYS** - WUU0_IN9

Note:

- +I2C_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- HD in Pad Type represents that the pin can support up to 20mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 5VTOL in Pad Type represents that the pin is 5V tolerant.
- DIS in default column represents that the pin's input buffer is disabled by default

- RST pads support passive filter and 1M ohm pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.
- PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.
- 5VTol and HD pads support two DSE bits in Pin Control register of the pin.
- SLOW in Pad Type represents the IO supports 25MHz. MED in Pad Type represents the IO supports 50MHz.
- +TAM in Pad Type represents the IO supports 1M ohm pull resistor.
- P0_6 is the ISP_ENTRY pin for LQFP100 , LQFP64 and LQFP48 package
- P3_29 is the ISP_ENTRY pin for QFN32 package

6.2 MCX A173, A174 Pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the "Pinout" tab in the Excel file.

6.3 Recommended connection for unused analog and digital pins

Table 43 shows the recommended connections for pins if those pins are not used in the customer's application

Table 43. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD	Must be powered	VDD is the IO supply of P0,P1,P2 and P4, and supplies internal modules including Flash, CMP, and etc.. It must be on
Power	VDD_ANA	Must be powered	VDD_ANA must be same level with VDD, and ramps up together with VDD_ANA
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	ADC*n*_*x*/DAC*n*_OUT	Float	
Analog/non-GPIO	EXTAL	Float	
Analog/non-GPIO	XTAL	Float	Analog output - Float
GPIO/Analog	Px/ADC*n*_*x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	JTAG_TCLK	Float	Float (default is JTAG with pulldown)

Table continues on the next page...

Table 43. Recommended connection for unused interfaces...*continued*

Pin Type	Pin Function	Recommendation	Comments
GPIO/Digital	JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

7 Ordering parts

7.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCXA174VLL

Note:

For complete list of Orderable part numbers, please refer Table 1

8 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8.2 Part number format

Part numbers for this device have the following format:

B PS F C D FS T PG SR PT

Table 44. Part number fields descriptions

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• A
F	Family	• 1 = Baseline
C	Core Features	• 7 = 180 MHz, 2x ADC, 2x Motor PWM, 4x UART, 1x CAN
FS	Flash Size	• 3 = 128 KB • 4 = 256 KB
T	Junction Temperature range (°C)	• V = –40 to 125

Table continues on the next page...

Table 44. Part number fields descriptions...*continued*

Field	Description	Values
PG	Package	• FM = HPQFN32 • LQ = LQFP144 • LL = LQFP100 • LF = LQFP48
SR	Silicon Revision	• A = Initial Mask set • B = 1st Major spin • C = 2nd Major spin
PT	Package Type	• R = Tape and Reel • T = Tray

8.3 Example

This is an example part number:

MCXA174VLH

8.4 Small package marking

8.4.1 Package marking information

Table 45. Package Marking

Line	H-PQFN32	LFP48	LQFP64	LQFP100
First Line	AAAAAA	AAAAAA	AAAAAAA	AAAAAAAAAA
Second Line	MMMMM	MMMMM	AAA MMMMM	MMMMM
Third Line	XXYWXX	XXXYWXX	XXXXYYWWXX	XXXXYYWWXX

Table 46. Package marking

Identifier	Description
A	Part number code, refer to Ordering Information
M	Mask set
Y	Year
W	Work week
X	NXP internal use

9 Terminology and guidelines

9.1 Definitions

Key terms are defined in the following table:

Table 47. Definitions

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. ***Note:*** *The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.*
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions ***Note:*** *Typical values are provided as design guidelines and are neither tested nor guaranteed.*

9.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

Figure 21. Examples

9.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 48. Typical-value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

Note: *Typical values are based on characterization but not covered by test limits in production.*

9.4 Relationship between ratings and operating requirements

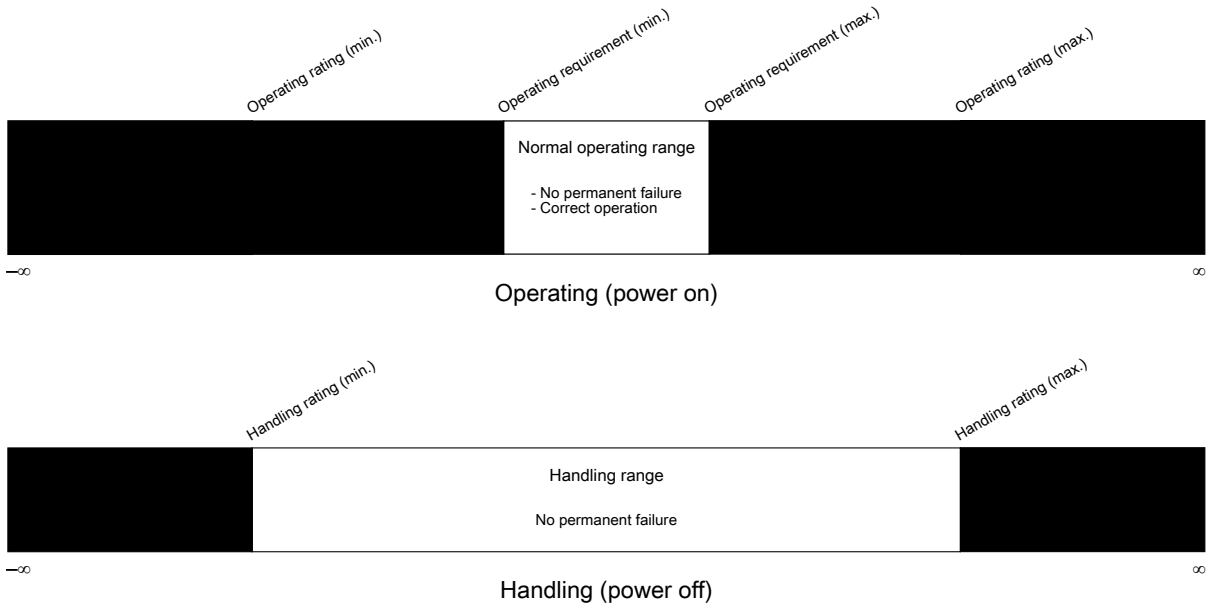

Figure 22. Relationship between ratings and operating requirements

9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9.6 Specification Test Methods

Each specification is tested using one of these methods.

Table 49. Specification test methods

Code	Method	Description
P	Production direct	On every chip during production, testing the specification

Table continues on the next page...

Table 49. Specification test methods*...continued*

Code	Method	Description
I	Production indirect	On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself
C	Characterization on a production tester	Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature ***Note:*** *Typical values are not necessarily characterized across process.*
L	Characterization on lab equipment or a nonproduction tester	
D	Guaranteed by design	Specification based on scientific and engineering principles
O	Other	Using methods such as: • Performing silicon simulations • Performing package thermal simulations • Calculating specifications using reliability data

10 Revision History

The following table provides a revision history for this document.

Table 50. Revision History

Document ID	Release Datae	Description
MCXAP100M180F41 v.2	30 November 2025	• Initial public version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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