FS26

Safety system basis chip with low power for ASIL D/ASIL B

Rev. 6.0 — 12 December 2025 **Product short data sheet**

SAFE ASSURE by NXP

Document information

Information	Content
Keywords	Safety, SBC, automotive, low power, ASIL B, ASIL D
Abstract	Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, such as those in the S32K3 series.

1 About this document

This short data sheet is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

The technical content in this short data sheet is a subset of the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant FS26 full data sheet, including all aspects related to functional safety, available via the NXP Secure Files content interface to those with non-disclosure agreement (NDA) access.

2 General description

Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin-to-pin and software compatible. These versions support a wide range of applications with Automotive Safety Integrity Levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power-up sequencing, and integrated system-level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. It offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionalities for system control and diagnostics, including an analog multiplexer, general-purpose input/outputs (GPIOs), and selectable wake-up events from I/O, long duration timer, or serial peripheral interface (SPI) communication.

The FS26 is developed in compliance with the ISO 26262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

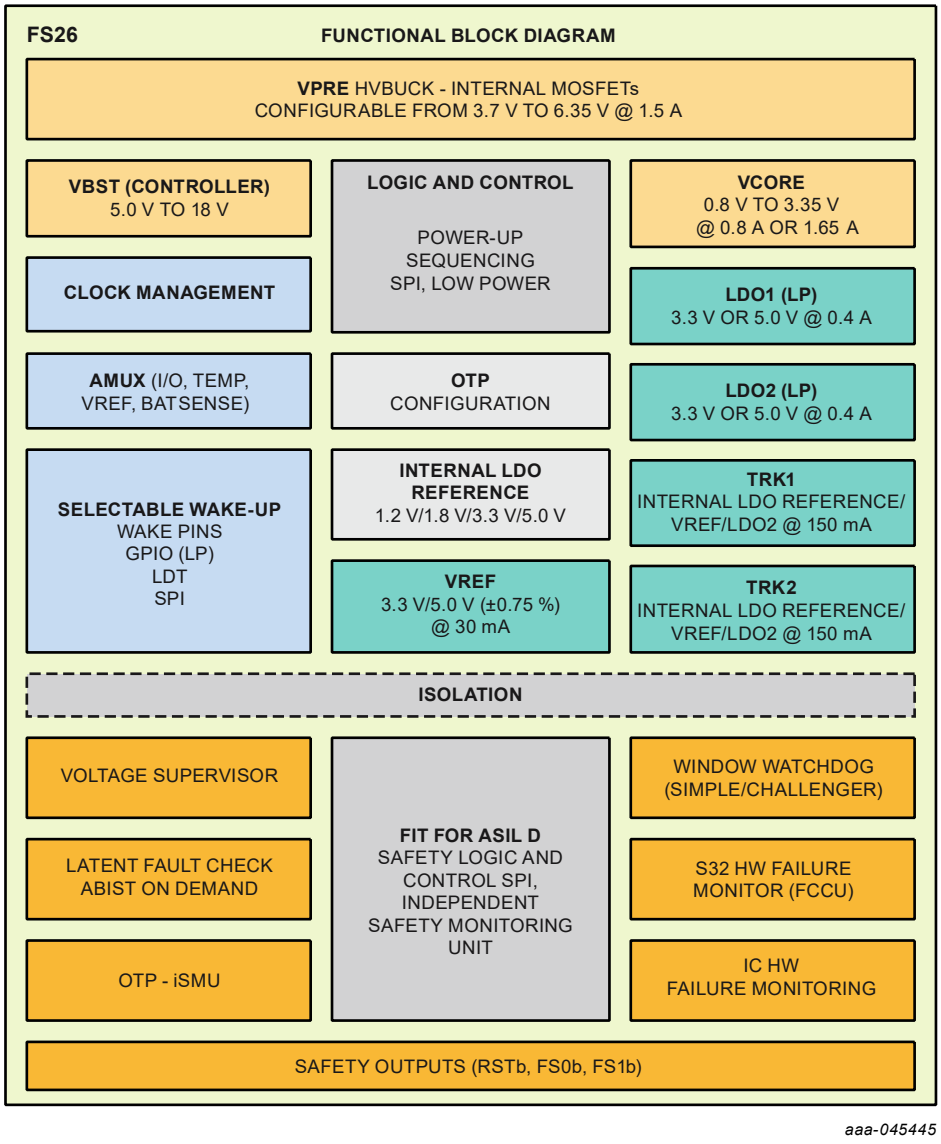

Figure 1. Functional block diagram

3 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Supports operating voltage range down to battery 3.2 V with VBST in front-end
- Supports operating voltage range down to battery 6 V without VBST in front-end
- Low-power *LPOFF mode* with 30 µA quiescent current
- Low-power *standby mode* with 29 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low-power *standby mode* operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: Asynchronous boost controller with external low-side switch, diode, and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Supports high-voltage protection for ECU off- board operation. Each tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with wake-up capability or HS/LS driver
- Programmable long duration timer (LDT) for system shutdown and wake-up control
- Monitoring of system voltages (Including Battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI activity
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC)

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from automotive safety integrity levels (ASIL) B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup
- Analog built-in self-test (ABIST2) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP Emulation mode for hardware development and evaluation
- *Debug mode* for software development, MCU programming, and debugging

4 Simplified application diagram

Figure 2 shows a simplified block diagram for a typical system with an FS26, using the boost controller to support battery cold-crank events.

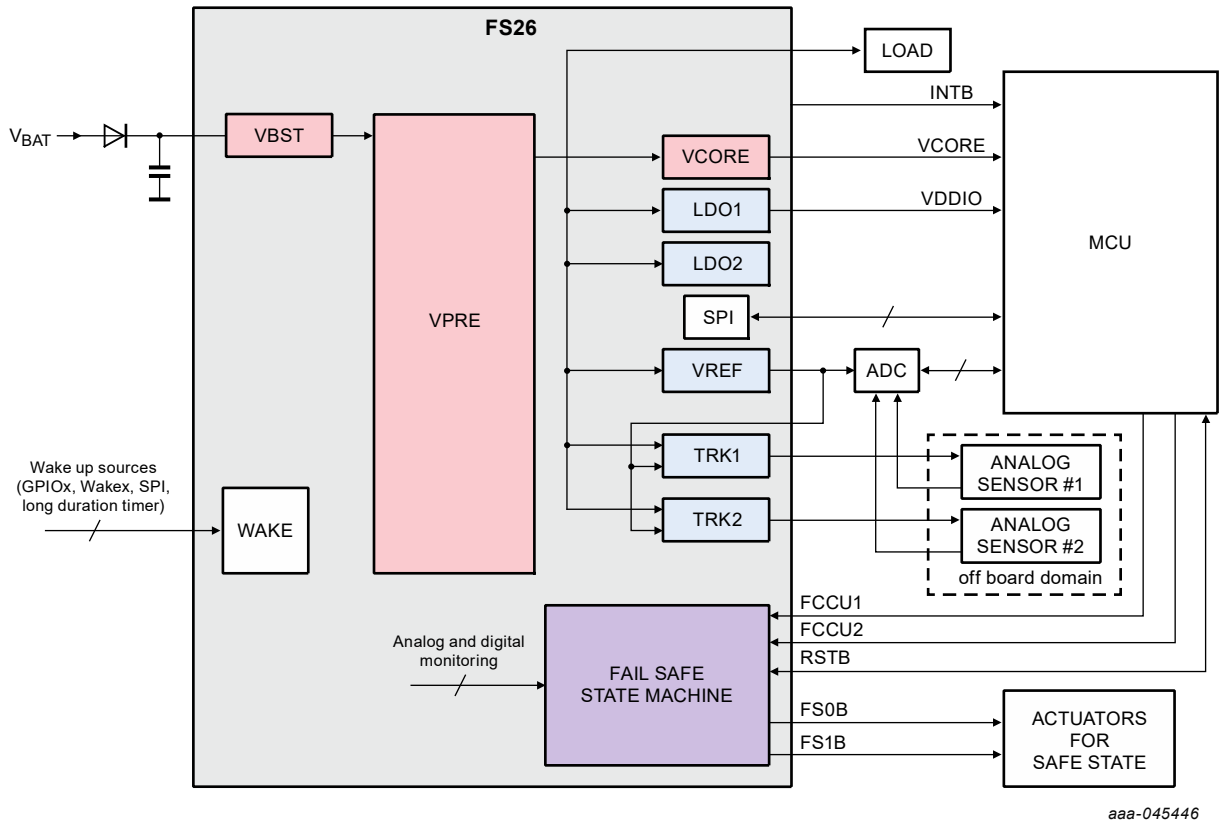

Figure 2. Example of application diagram with VBST as a front-end regulator

Figure 3 shows a simplified block diagram for a typical system with an FS26, using the boost controller to generate a voltage above the high-voltage buck output voltage.

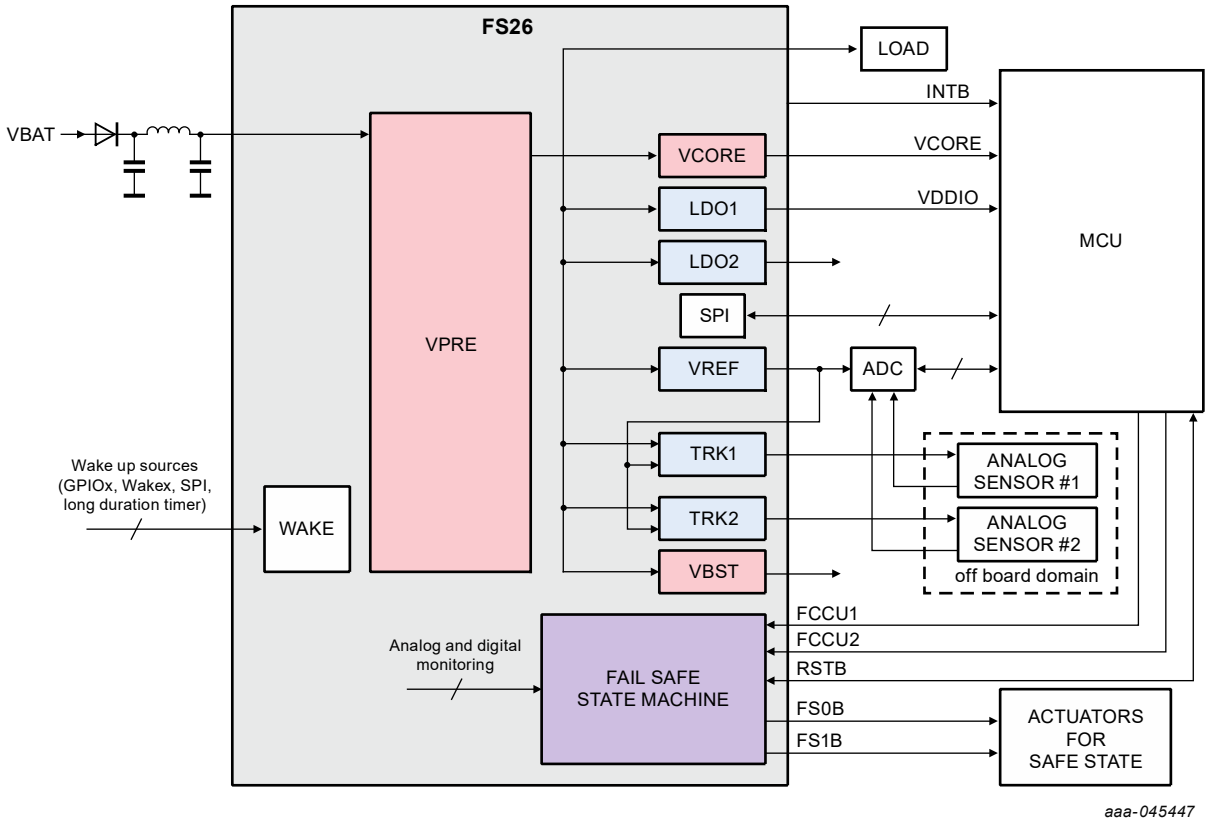

Figure 3. Example of application diagram with VBST as a back-end regulator

5 Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

5.1 Part number definition

Figure 4 shows how the FS26xyz part number is used to describe the available feature set of each device.

FS26xx
Product Numbering Scheme

P	FS	26 X Y	A	M	Zzz	AD
Release Type	Family	Product Core	Release Version	Temperature	Funct. or Param. variant	Package
P Prototype	FS High Voltage Power Management	2600-2633 Core	A Initial release	M -40 to 125 °C	A0 No OTP	AD LQFP48
M Standard production			H Enhanced manufacturability		A1-ZZ Unique part identification	
S Specific production			B-Z As required			

FS 2 6 X Y Z

Z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

X	PMIC Solution
0	VCORE 0.8 A, VBST, 1 MV Buck, 2 LDOs 1 Tracker
1	VCORE 0.8 A, VBST, 1 MV Buck, 2 LDOs 2 Trackers
2	VCORE 1.65 A, VBST, 1 MV Buck, 2 LDOs 1 Tracker
3	VCORE 1.65 A, VBST, 1 MV Buck, 2 LDOs 2 Trackers

aaa-045498

Figure 4. Part number breakdown

Figure 5 maps FS26 part numbers vs. product feature sets.

Vcore	0.8 A core				1.65 A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

aaa-045499

Figure 5. Part number mapping versus features set

5.2 Part number list

Table 1. Device segmentation

Part Number	DEV_ID[5:0]	Tracker 2 TRK2	VCORE current capability	Long Duration Timer (LDT)	Tracker 2 monitoring VMON_TRK2	FS1B	ABIST on demand ABIST2	Watchdog type	Fault recovery	FCCU monitoring	LBIST
FS2600B	01h	NO	0.8 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2601B	02h	NO	0.8 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2602B	03h	NO	0.8 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2603B	04h	NO	0.8 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2600D	05h	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2601D	06h	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	07h	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	08h	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	09h	YES	0.8 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2611B	0Ah	YES	0.8 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2612B	0Bh	YES	0.8 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2613B	0Ch	YES	0.8 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2610D	0Dh	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0Eh	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0Fh	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	10h	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	11h	NO	1.65 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2621B	12h	NO	1.65 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2622B	13h	NO	1.65 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2623B	14h	NO	1.65 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2620D	15h	NO	1.65 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	16h	NO	1.65 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	17h	NO	1.65 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	17h	NO	1.65 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	19h	YES	1.65 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2631B	1Ah	YES	1.65 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2632B	1Bh	YES	1.65 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2633B	1Ch	YES	1.65 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2630D	1Dh	YES	1.65 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	1Eh	YES	1.65 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	1Fh	YES	1.65 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	20h	YES	1.65 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Additional part numbers will exist with different features and parametric settings. Table 1 is an example of a part number list.

Table 2. Orderable production part numbers

Part number	Description	Package
MFS2613HMDA2AD MFS2613AMDA2AD	S32K344 + FS26 EVB ASIL D S32K3X4EVB-x257	LQFP48
MFS2613HMDA3AD MFS2613AMDA3AD	S32K344 400 V HVBMS Reference design	
MFS2613HMDA4AD MFS2613AMDA4AD	S32K344 Body Control Module Reference design (White board)	
MFS2613HMDA6AD MFS2613AMDA6AD	S32K344 48 V MC Development platform	
MFS2621HMDABAD MFS2621AMDABAD	AURIX TC38x, TC29x	
MFS2613HMDDCAD MFS2613AMDDCAD	S32K324 5G T-BOX + Gateway	
MFS2633HMDALAD MFS2633AMDALAD	S32K3x8 and S32K396 MCU attach	
MFS2633HMDE4AD MFS2633AMDE4AD	S32K396 Reference design	
MFS2613HMDH3AD MFS2613AMDH3AD	S32K344 400 V HVBMS Reference design (No VBST)	
MFS2633HMDAHAD MFS2633AMDAHAD	S32K396 BMS Reference Design	
MFS2633HMDAJAD MFS2633AMDAJAD	S32K358 400 V & 800 V HVBMS Reference design	
MFS2633HMDC3AD MFS2633AMDC3AD	S32K358 400 V & 800 V HVBMS Reference design (wireless)	
MFS2633HMDAKAD MFS2633AMDAKAD	S32K358 400 V & 800 V HVBMS Reference design (No VBST)	
MFS2633HMDADAD MFS2633AMDADAD	RH850UA2x for BMS and ZCU Applications (VCORE = 1.09 V)	
MFS2623HMDAEAD MFS2623AMDAEAD	RH850C, RH850P or RH850F for EPS, BMS, Motor control and DCDC applications (VCORE = 1.25 V)	
MFS2633HMDAMAD MFS2633AMDAMAD	RH850UA2x for ADAS, Smart cockpit and 3.3 V applications (VCORE = 1.09 V)	
MFS2613HMDAAAD MFS2613AMDAAAD	S32K344 + FS26 14 V/48 V/HV BMS Reference design ASIL D KITBMS_MTR_EVM	
MFS2613HMDHKAD MFS2613AMDHKAD	S32K344 + FS26 BMS ASIL D	
MFS2633HMDB2AD MFS2633AMDB2AD	S32K3x8 + FS26 Standby support ASIL D Smart-cockpit	
MFS2600HMBA0AD MFS2600AMBA0AD	OTP Blank variant for FS2600B devices	
MFS2600HMDA0AD MFS2600AMDA0AD	OTP Blank variant for FS2600D devices	
MFS2601HMBA0AD MFS2601AMBA0AD	OTP Blank variant for FS2601B devices	
MFS2601HMDA0AD MFS2601AMDA0AD	OTP Blank variant for FS2601D devices	
MFS2602HMBA0AD MFS2602AMBA0AD	OTP Blank variant for FS2602B devices	
MFS2602HMDA0AD MFS2602AMDA0AD	OTP Blank variant for FS2602D devices	
MFS2603HMBA0AD MFS2603AMBA0AD	OTP Blank variant for FS2603B devices	
MFS2603HMDA0AD MFS2603AMDA0AD	OTP Blank variant for FS2603D devices	
MFS2610HMBA0AD MFS2610AMBA0AD	OTP Blank variant for FS2601B devices	
MFS2610HMDA0AD MFS2610AMDA0AD	OTP Blank variant for FS2610D devices	
MFS2611HMBA0AD MFS2611AMBA0AD	OTP Blank variant for FS2611B devices	

Table 2. Orderable production part numbers*...continued*

Part number	Description	Package
MFS2611HMDA0AD MFS2611AMDA0AD	OTP Blank variant for FS2611D devices	
MFS2612HMBA0AD MFS2612AMBA0AD	OTP Blank variant for FS2612B devices	
MFS2612HMDA0AD MFS2612AMDA0AD	OTP Blank variant for FS2612D devices	
MFS2613HMBA0AD MFS2613AMBA0AD	OTP Blank variant for FS2613B devices	
MFS2613HMDA0AD MFS2613AMDA0AD	OTP Blank variant for FS2613D devices	
MFS2620HMBA0AD MFS2620AMBA0AD	OTP Blank variant for FS2620B devices	
MFS2620HMDA0AD MFS2620AMDA0AD	OTP Blank variant for FS2620D devices	
MFS2621HMBA0AD MFS2621AMBA0AD	OTP Blank variant for FS2621B devices	
MFS2621HMDA0AD MFS2621AMDA0AD	OTP Blank variant for FS2621D devices	
MFS2622HMBA0AD MFS2622AMBA0AD	OTP Blank variant for FS2622B devices	
MFS2622HMDA0AD MFS2622AMDA0AD	OTP Blank variant for FS2622D devices	
MFS2623HMBA0AD MFS2623AMBA0AD	OTP Blank variant for FS2623B devices	
MFS2623HMDA0AD MFS2623AMDA0AD	OTP Blank variant for FS2623D devices	
MFS2630HMBA0AD MFS2630AMBA0AD	OTP Blank variant for FS2630B devices	
MFS2630HMDA0AD MFS2630AMDA0AD	OTP Blank variant for FS2630D devices	
MFS2631HMBA0AD MFS2631AMBA0AD	OTP Blank variant for FS2631B devices	
MFS2631HMDA0AD MFS2631AMDA0AD	OTP Blank variant for FS2631D devices	
MFS2632HMBA0AD MFS2632AMBA0AD	OTP Blank variant for FS2632B devices	
MFS2632HMDA0AD MFS2632AMDA0AD	OTP Blank variant for FS2632D devices	
MFS2633HMBA0AD MFS2633AMBA0AD	Superset covering FS2633B devices	
MFS2633HMDA0AD MFS2633AMDA0AD	Superset covering FS2633D devices	

Note: *Parts with release version "A" are no longer recommended for new designs. Instead, the comparable part with release version "H" should be used.*

Empty OTP samples can be ordered for engineering purposes using part numbers MFS2633AMDA0AD, MFS2633AMBA0AD, MFS2633HMDA0AD, or MFS2633HMBA0AD. See Table 127 for the complete OTP content description.

6 Applications

xEV and powertrain market

- Inverter
- Onboard charger (OBC), DCDC
- Battery management system (BMS)
- Belt starter generator (BSG)

Body market

- Gateway
- Zonal control
- Body controller
- Smart junction box

Safety and chassis

- Suspension
- Power steering

MCU attach

- NXP S32K3 family
- Infineon Aurix family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

7 Block diagram

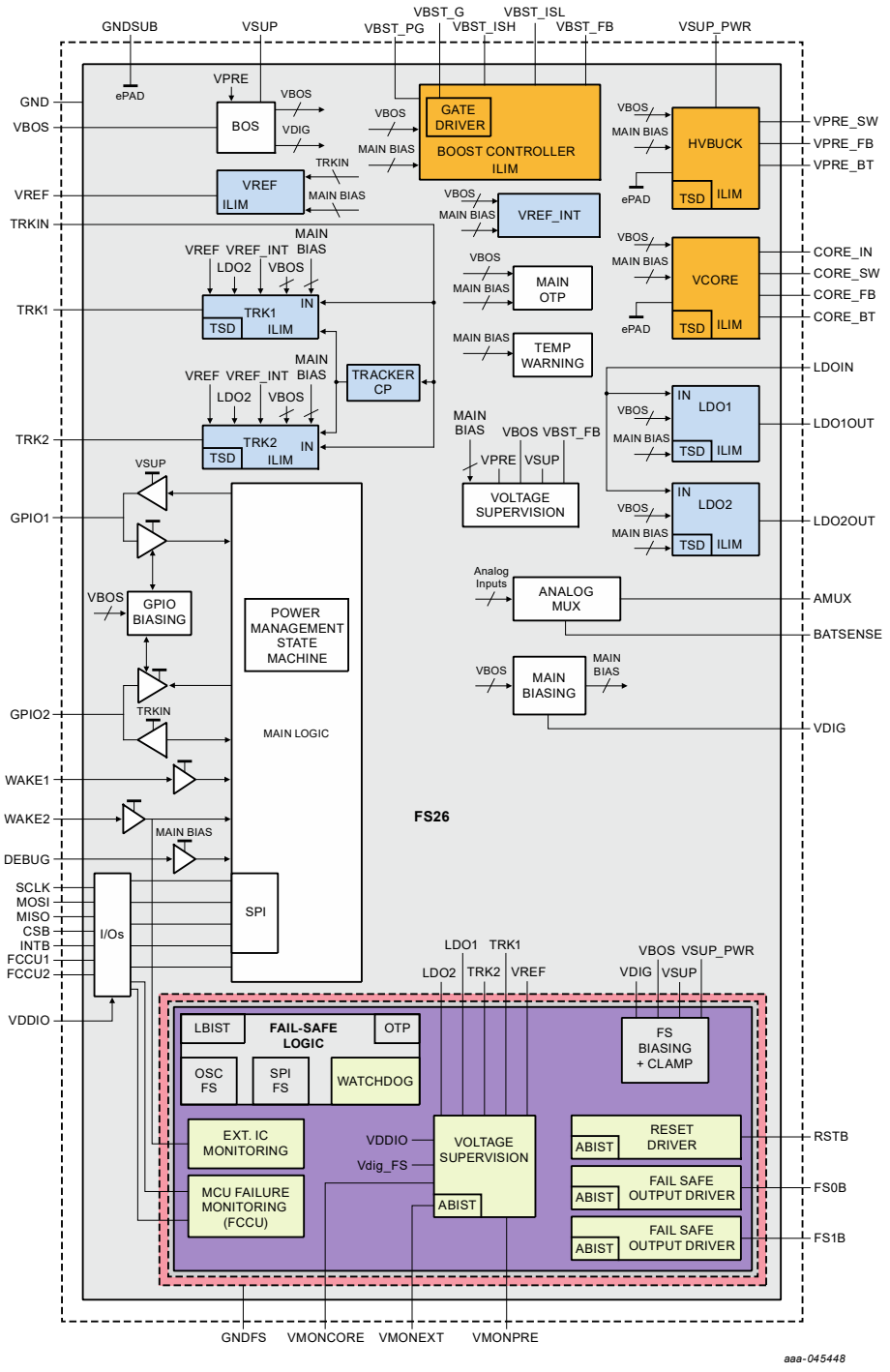

Figure 6. Block diagram of the FS26

8 Pinning information

8.1 Pinning

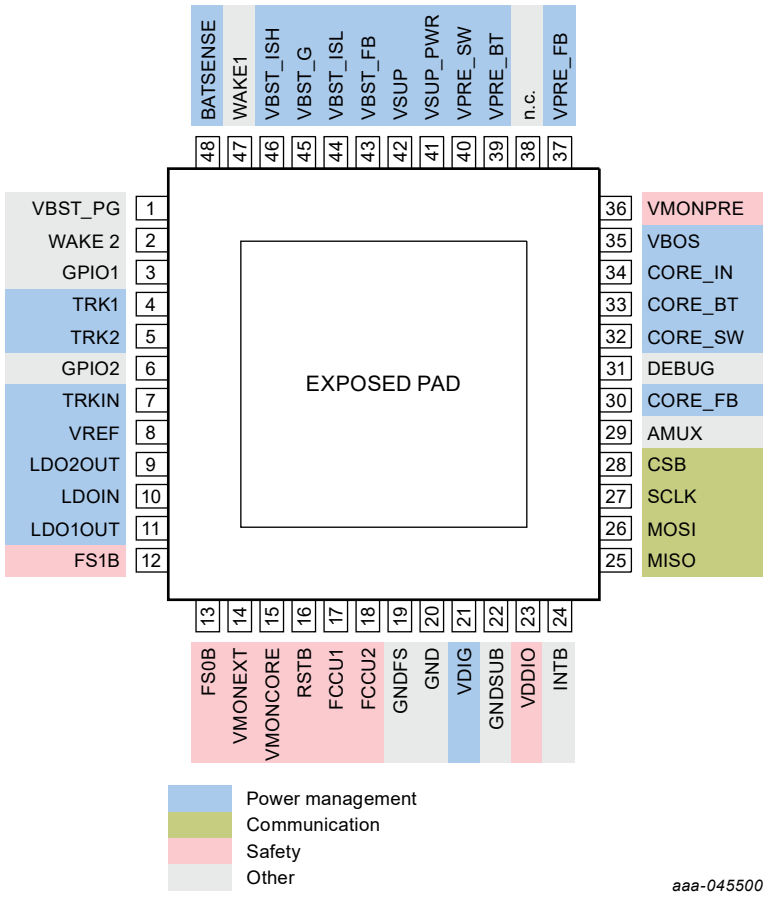

Figure 7. Pin assignment in LQFP48 package with exposed pad

8.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin Number	Type	Description
VBST_PG	1	Digital output	Power Good signal of VBST
WAKE2	2	Analog input	WAKE2 input pin or ERRMON input
GPIO1	3	Analog output / Digital Input	General Purpose I/O 1 (GPIO1)
TRK1	4	Analog output	TRK1 regulator output
TRK2	5	Analog output	TRK2 regulator output
GPIO2	6	Analog output / Digital Input	General Purpose I/O 2 (GPIO2)
TRKIN	7	Analog input	TRK1, TRK2 and VREF regulators input
VREF	8	Analog output	Voltage reference output (VREF)
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO1 and LDO2 regulator input voltage supply
LDO1OUT	11	Analog output	LDO1 regulator output
FS1B	12	Digital output	Safety output #1 (FS01)

Table 3. Pin descriptions*...continued*

Symbol	Pin Number	Type	Description
FS0B	13	Digital output	Safety output #0 (FS02)
VMONEXT	14	Analog input	VMON_EXT voltage monitoring input
VMONCORE	15	Analog input	VMON_CORE voltage monitoring input
RSTB	16	Digital input/output	Reset input/output (RSTB)
FCCU1	17	Digital input	Fault Control Collection Unit (FCCU) pin 1
FCCU2	18	Digital input	Fault Control Collection Unit (FCCU) pin 2
GNDFS	19	Ground connection	Ground connection for fail-safe circuitry
GND	20	Ground connection	Ground connection for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI Primary In Secondary out
MOSI	26	Digital input	SPI Primary Out Secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog multiplexer (AMUX) output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin. Used to enter OTP and *debug mode*
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best Of Supply (BOS) decoupling output
VMONPRE	36	Analog input	VMON_PRE voltage monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to ground)

9 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	8.5	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EP	DC voltage at GNDFS, GND, GNDSUB pins, and exposed pad (EP)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

10 Electrostatic discharge

Table 5. ESD

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

11 Thermal ratings

Table 6. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S bit	145	155	170	°C

Table 7. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient[1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom[2][3] (with uniform power dissipation on the silicon die)	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top[1]	13.5	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

12 EMC compliance

The FS26 EMC performance is verified against BISS generic IC EMC Test Specification version 2.0 from 07.2012 and FMC1278 Rev3 Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems from 2018. For performance results and specific conditions, refer to the FS26 webpage.

13 Supply voltage and operating range

13.1 Supply voltage

Depending on the chosen front-end voltage regulator (VPRE or VBST), the FS26 can support two different supply voltage ranges.

If VBST is chosen to be the front-end DCDC converter (directly connected to the battery), the supply voltage of the FS26 can go down to voltage levels typical of a cold-crank event. Because of this, the FS26 can still provide all available regulated voltages, even when the battery line drops below the VPRE output voltage. In this case, the supply voltage operating range is extended to V_{BST_IN} range.

When VPRE is chosen to be the first DCDC converter connected to the battery, the FS26 is unable to provide power rails when the supply voltage is below the V_{PRE_IN} minimum limit. This topology can be used in applications where $V_{SUP\_PWR} > V_{PRE\_PWM} + V_{PRE\_HDR}$, avoiding degraded operation (drop-out mode). Note that there is a drop between V_{BAT} and V_{SUP}. VSUP_UVTH_OTP = 1 is then mandatory.

If an application requires voltages above the VPRE output voltage, the boost controller can be used to generate these voltages. In this case, the supply voltage operating range is narrowed down to the V_{PRE_IN} voltage range.

The VSUP pin voltage V_{SUP} is monitored to avoid erratic startup and shutdown of the FS26. Specific voltage thresholds are implemented with hysteresis. When V_{SUP} is rising, the FS26 does not start until the V_{SUP} crosses the V_{SUP_UVH} threshold. If V_{SUP} goes below V_{SUP_UVL} before the end of the power-up sequence, the device will restart. Once the power-up sequence is finished and the device is in *normal mode*, V_{SUP_UVL} has no effect.

The VSUPUV6_I SPI bit can notify the system that the input voltage of the FS26 is decreasing, indicating that V_{SUP} has crossed the V_{SUP_UV6} voltage threshold.

Table 8. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. $V_{SUP\_UVH} < V_{SUP} < 36$ V, $V_{PRE\_PWM} + V_{PRE\_HDR} < V_{SUP\_PWR} < 36$ V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{SUP}	Device input supply voltage (on VSUP pin)	V_{SUP_UVL}	12	36	V
V_{SUP_PWR}	Device input supply voltage (on VSUP_PWR pin)	V_{PRE_IN}	12	36	V
V_{SUP_OV}	Threshold voltage to latch the interrupt VSUPOV_I (on VSUP pin)	19.3	20	20.7	V
V_{SUP_UV6}	Threshold voltage to latch the interrupt VSUPUV6_I (on VSUP pin)	5.8	6.0	6.2	V
V_{SUP_UVH}	V_{SUP} undervoltage threshold (rising edge on VSUP pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.6 5.95	 4.8 6.1	 5.0 6.25	V
V_{SUP_UVL}	V_{SUP} undervoltage threshold (falling edge on VSUP pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.1 5.5	 4.3 5.65	 4.5 5.8	V
V_{PRE_UVH}	V_{PRE} undervoltage threshold high (rising edge on VPRE pin)	2.9	3.0	3.1	V
V_{PRE_UVL}	V_{PRE} undervoltage threshold low (falling edge on VPRE pin)	2.5	2.6	2.7	V
V_{PRE_UVBOS}	V_{PRE} undervoltage threshold to switch VBOS from VPRE to VSUP when BOS_IN_OTP[1:0] = 0	3.4	3.55	3.7	V

13.2 Operating range

FS26 operation range is divided in subranges with its own specificities:

- **No Operation** means the device is not providing the expected functionality or is shut down.
- **Low Voltage Extended Operation** means the device remains functional but with reduced electrical performance.
  - VPRE may be in drop out mode. VPRE output voltage may decrease below its nominal value and the transient load will be degraded.
- **Full Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet and within the operating mission profile of the safety manual.
- **High-voltage Extended Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet but for a limited period of time. This could occur during load dump or double-battery jump-start events, for example.
- **Electrical Characteristics not guaranteed** means the device remains functional, but with reduced electrical performance.
  - In Low-power mode, the quiescent current will increase.
  - In *normal mode*, the VPRE thermal limitation may trigger the thermal shutdown. VPRE transient load will be degraded.
- **Risk of damage** means the device is overstressed, with a risk of damage to the device.

The ranges are shown in Figure 8 and Figure 9.

13.2.1 Operating range in *Normal* mode

The FS26 device supports two distinct topologies for boost converter configuration, giving two distinct operating ranges for the input voltage. When the boost is used as a front-end regulator, a wider input supply range is supported. When the boost is used as a back-end regulator or is not used, V_{SUP} and V_{SUP_PWR} must be V_{PRE_HDR} higher than the VPRE output voltage V_{PRE} (V_{PRE_PWM} and / or V_{PRE_PFM}) to ensure full parametric operation.

Figure 8 describes the supply range of the FS26 with or without the boost used as a front-end or back-end regulator. Front-end topology should be used to support cold-crank events on the battery input. In the back-end configuration, full operation is guaranteed when V_{SUP} is higher than V_{PRE_PWM} + V_{PRE_HDR}. (See Section 18.2 for V_{PRE_HDR}).

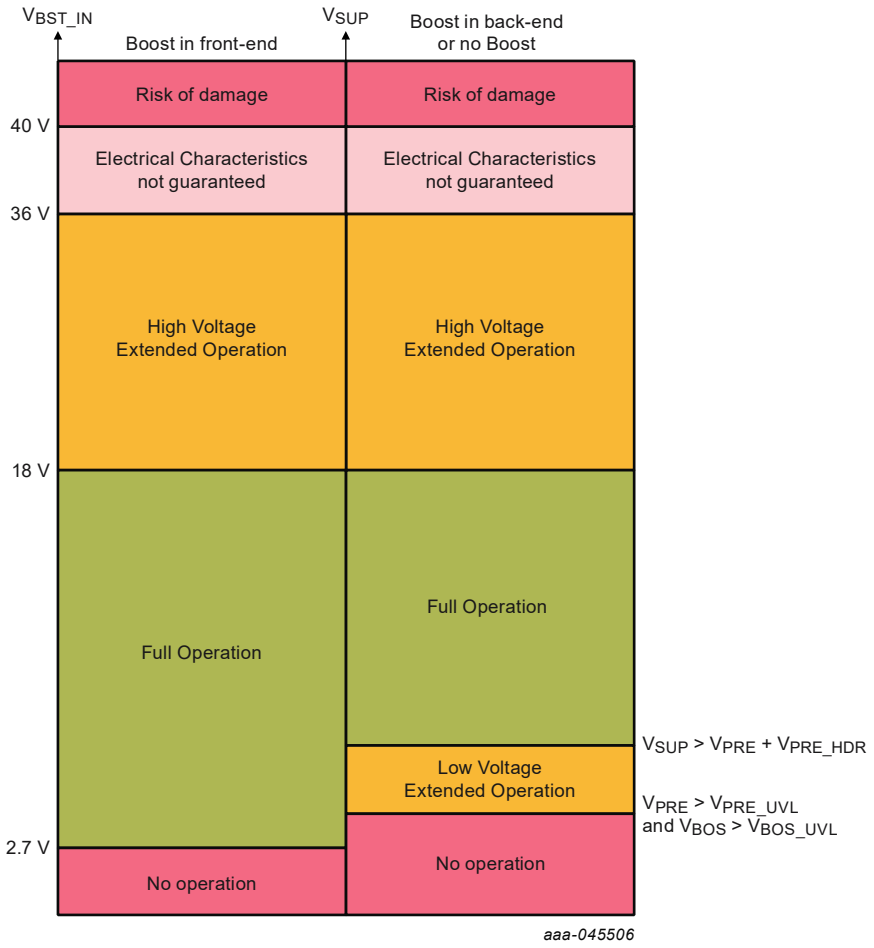

Figure 8. Input voltage range in *normal mode*

13.2.2 Operating range in *Low-power* modes

In *standby mode* and *LPOFF mode*, monitors are disabled to ensure lowest current consumption. The minimum operating condition is V_{BOS_POR}.

Figure 9 describes the supply range of the FS26 in *standby mode* and *LPOFF mode*. When transitioning to *standby mode*, the boost regulator will be turned off and VPRE will switch from VPRE_OTP[5:0] to VPRE_LP_OTP[5:0].

When the device is in *LPOFF mode*, all the regulators are turned off.

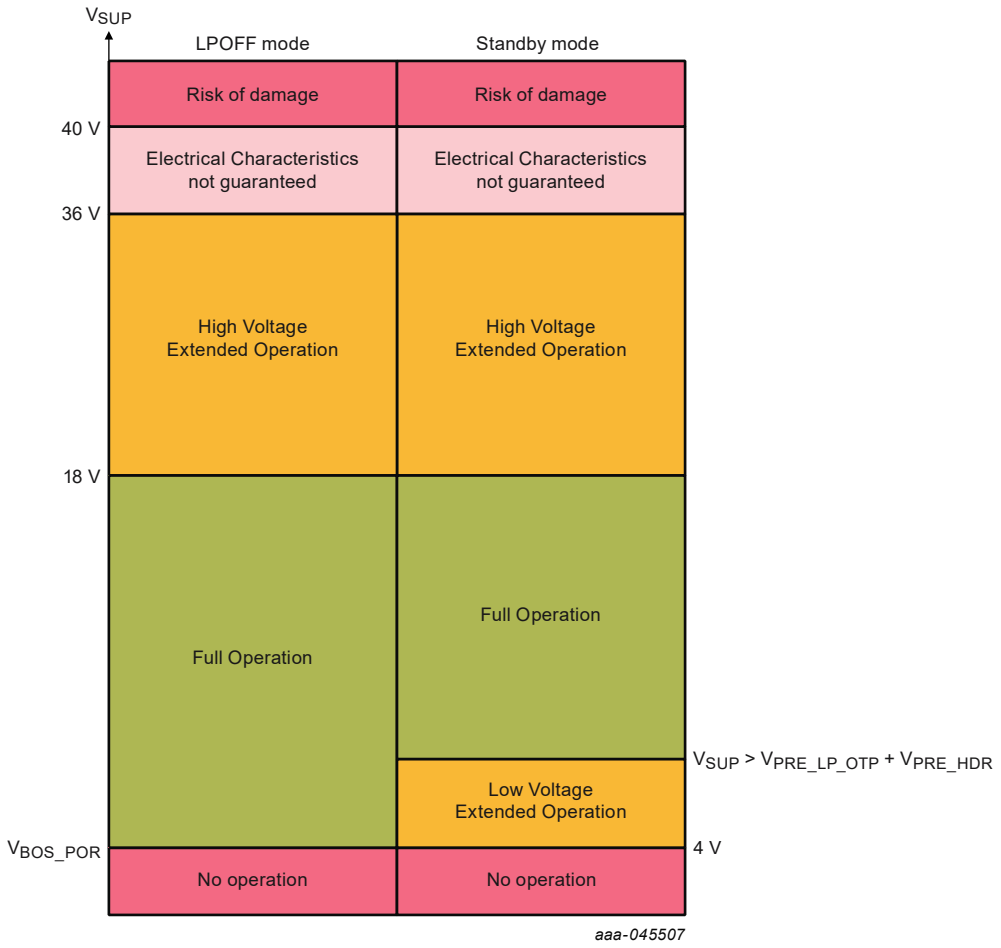

Figure 9. Input voltage range in *standby mode* and *LPOFF mode* (legend)

14 Current consumption

Table 9. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Quiescent current					
I_{Q_NORMAL}	Current consumption in *normal mode* on the battery: • V_{SUP} = V_{SUP_PWR} = 13.5 V (including current from BATSENSE pin) • VBST enabled but not switching. • VPRE output voltage set at 5.5 V • L_{PRE} = 10 µH • VCORE enabled and output voltage set at 1.5 V • LDO1 enabled and output voltage set at 5.0 V • LDO2 enabled and output voltage set at 3.3 V • TRK1 and TRK2 enabled and output voltage set at 5 V • VREF enabled and output voltage set at 5 V • Long Duration Timer enabled • All regulators output current = 0 A		15	25	mA
I_{Q_STBY}[1]	Current consumption in *standby mode* on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 12 V, 18 V (including current from BATSENSE pin) • V_{PRE_PFM} = 3.7 V (PFM mode) • L_{PRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled, < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE_PFM} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in *standby mode*.		32 36 40	— — 60	µA
I_{Q_STBY}	Current consumption in *standby mode* on the battery • T_A = 25 °C • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V (including current from BATSENSE pin) • V_{PRE_PFM} = 3.7 V and 5.05 V (PFM mode) • L_{PRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V when V_{PRE_PFM} = 3.7 V, V_{LDO1} = 5.0 V when V_{PRE_PFM} = 5.05 V. • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE_PFM} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in *standby mode*.		90 110	— 130	µA
I_{Q_LPOFF}, I_{Q_DFS}	Current consumption in *LPOFF mode* and *Deep Fail Safe* (DFS) state on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V, 12 V, 18 V • (Including current from BATSENSE pin) • All regulators are disabled. • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in LPOFF		30 32 40	— — 60	µA

[1] VBAT current is reduced in *standby mode* due to the ratio between VBAT and VPRE voltages.
[2] Guaranteed by characterization. Tested in production at 25 °C only.

14.1 Total battery current consumption estimation in *Standby* mode

The *standby mode* current consumption can be estimated using Figure 10 and Figure 11 at T_A = 25 °C and T_A = 85 °C, depending on the use case. The measurements were made with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{PRE} = 10 µH
- Long Duration Timer disabled.
- GPIOx disabled in standby.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in *standby mode*.
- All regulators unloaded.

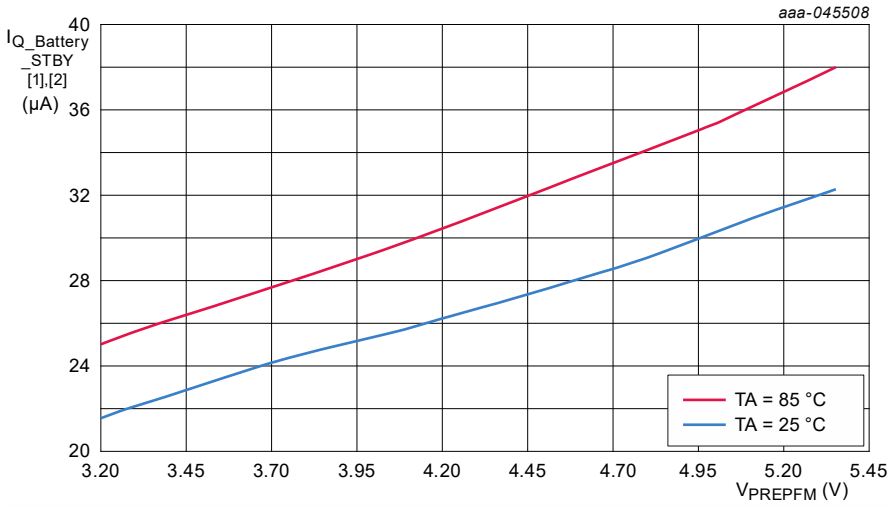

Figure 10. Battery current consumption in standby mode (LDO1 and LDO2 disabled)

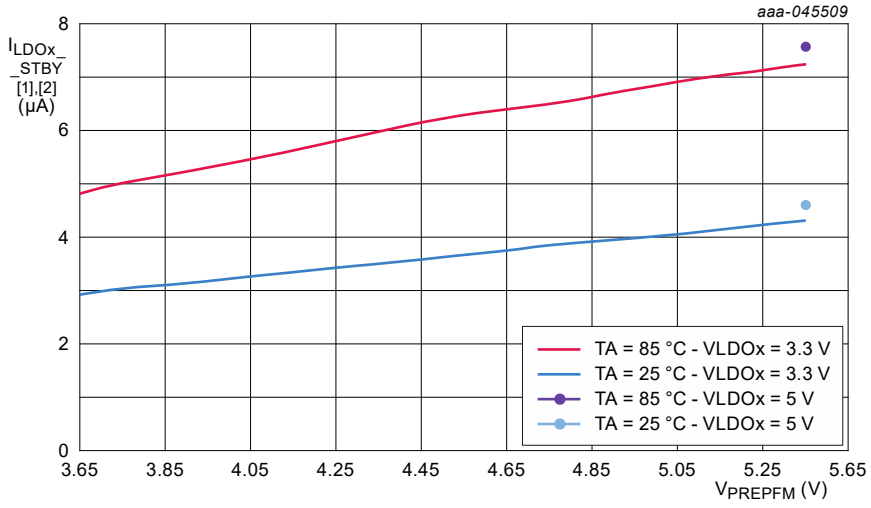

Figure 11. LDOx current consumption in standby mode

When LDOx is used at 5 V, VPRE output voltage in *standby mode* must be 5.35 V to comply with the LDOx minimum dropout voltage. [1] [2]

1 In *standby mode* VBAT current is reduced, due to the ratio between VBAT and VPRE voltages.

The total *standby mode* current consumption can be estimated at either T_A = 25 °C or T_A = 85 °C using the following formula:

$$I_{Q\_Total\_Battery\_STBY}(\mu A) = I_{Q\_Battery\_STBY} + I_{LDOx\_STBY} \times N$$

where N is the number of LDOx used.

14.2 *Standby mode* current consumption

In most cases, LDO1 or LDO2 regulators are used in *standby mode* to supply light loads.

The total battery current consumption can be estimated using Figure 12 at T_A = 25 °C and T_A = 85 °C, depending on the LDO1 or LDO2 load. The measurements have been done with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{PRE} = 10 µH
- Long duration timer disabled.
- GPIOx disabled in *standby*.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in *standby mode*.
- LDO1 and LDO2 enabled.
- V_{LDO1} = 3.3 V, V_{LDO2} = 5 V and V_{PRE_PFM} = 5.35 V.
- No external load on VPRE.

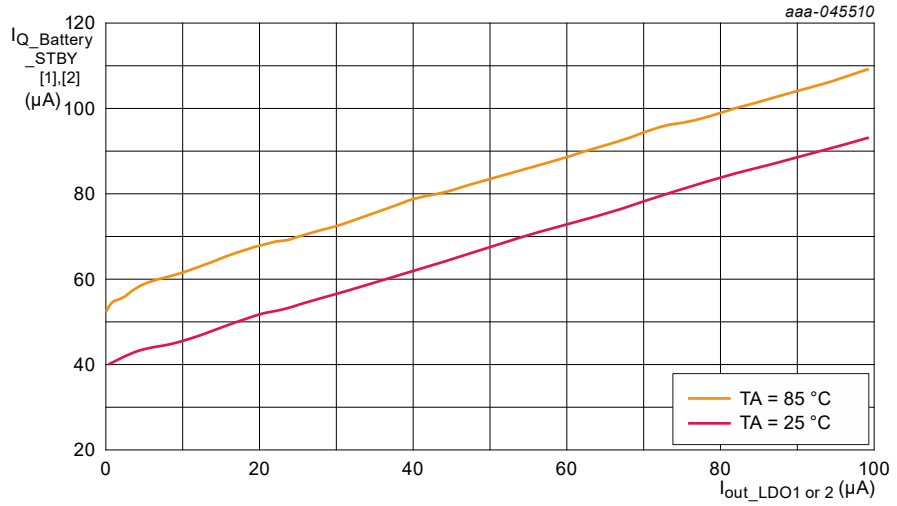

Figure 12. Total battery current consumption in *standby mode*

The total battery current consumption can also vary depending on the chosen inductor for L_{PRE}. The additional measurements shown in Section 14.2 were made using the following assumptions (see Figure 13):

- Long duration timer disabled
- GPIOx disabled in *standby*
- RSTB released and pulled up to VPRE
- V_{SUP} = V_{SUP_PWR} = 12 V

2 Guaranteed by characterization. Tested in production at 25 °C only.

- FS0B asserted, FS1B pulled up to a disabled supply in *standby mode*
- LDO1 and LDO2 disabled
- V_{PRE_PFM} = 5.35 V or 3.7 V
- No external load on VPRE

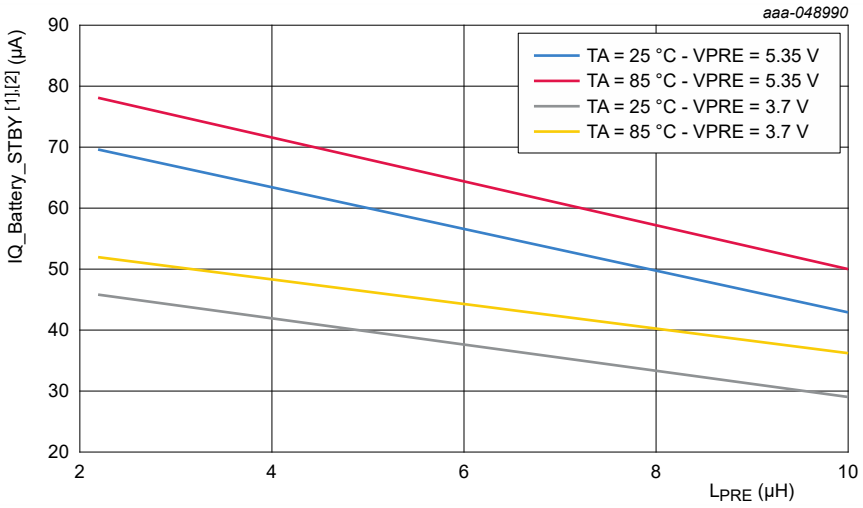

Figure 13. Battery current consumption in *standby mode* with V_{PRE_PFM} = 3.70 V or 5.35 V and LDOx disabled

15 General device operation

15.1 Functional device operation and power modes

FS26 operation is divided in two independent logic blocks to achieve best-in-class functional safety coverage. The main state machine manages the power management, the Low-power modes, and the wake-up sources, while the fail-safe state machine manages the monitoring of the power management, the monitoring of the microcontroller, and the monitoring of an external IC with ERRMON.

The FS26 provides three main operating modes:

- ***Normal mode*** is intended to be the fully functional mode. All power supplies are enabled as required by the system, and all system functionality provided by the FS26 is available. During *normal mode*, the fail-safe state machine is available and providing full monitoring and operation of all the safety features in the device.
- ***Standby mode*** is intended to be the Low-power ON mode, providing support to the minimum system requirements with low current consumption from the battery. During the *standby mode*, only the VPRE remains enabled to supply the microcontroller I/O rails. LDO1 and LDO2 can be enabled in this mode depending on the OTP configuration. GPIO1 and GPIO2 can remain at the same state as in *normal mode*, depending on the SPI configuration. *standby mode* is assumed to be a safe state with no critical activity, and therefore the fail-safe state machine is disabled to achieve minimum current consumption by the system.
- ***LPOFF mode*** is intended to be the Low-power OFF mode, with no active system supplies except GPIO1, which can remain enabled. Logic circuitry is internally supplied to allow proper wake up from any of the available wake-up mechanisms, with the minimum current consumption possible.

The system can wake up from any of the Low-power modes via any of the following selectable wake-up mechanisms available in the device (availability is dependent on part number):

- WAKE1 and WAKE2 pins
- GPIO1 and GPIO2 pins
- Long-duration timer (LDT) expiration
- SPI activity via edge detection of the CSB pin

Table 10 summarizes the operating modes and available features:

Table 10. Operating modes summary

Operating mode	Power supply state			Wake-up sources and capabilities		
	VPRE	LDOx GPIOx	VBST, VCORE TRK1, TRK2, VREF	WAKEx, GPIOx	LDT	MCU
Normal mode	PWM, ON	ON (Optional)	ON (Optional)	N/A	N/A	N/A
Standby mode	PFM, ON	ON (Optional)	OFF	YES	YES (Optional)	YES
LPOFF mode	OFF	OFF (GPIO1 optional)	OFF	YES	YES (Optional)	NO

The FS26 can also move to or through these two states:

- ***Load fuse*** state is a transitional state where the device loads its complete OTP configuration, previously programmed in its fuses. The Main and the Fail-safe state machines both have to go through this state when resuming from a power-up event.
- ***Deep Fail Safe*** (DFS) state is the device protection state. In this state, all regulators are OFF, **safety outputs are asserted**, the SPI interface is not accessible. The device waits for specific events to restart and to move to *load fuse* state to restart, and the safety outputs remain asserted until release conditions are met. DFS

state entry can be disabled by setting MDFS_DIS_OTP = 1 and DFS_DIS_OTP = 1, transition request sources listed hereafter will be ignored, however the safety pins are asserted accordingly with fault sources and reactions configuration.

Below is an exhaustive list of conditions that put the FS26 in the *Deep Fail Safe* state:

- RSTB pin is sensed to low level for a time longer than 8 seconds.
- Too many faults occur: fault error counter reaches its programmed limit (FLT_ERR_CNT[3:0] = @FLT_ERR_CNT_LIMIT[1:0]).
- When FAULT_DFS_EN_OTP = 1 the device enters the Deep Fail Safe state upon detection of an RSTB or FS0B fault, regardless of the actual states of the RSTB or FS0B pins.
- VPRE output voltage crosses V_{PRE_OVP} threshold for a time longer than t_{PRE_OVP}.
- Each regulator is disabled when an overtemperature event is detected, that is thermal shutdown (TSD). Additionally, the TSD event can be configured with M_TSD_CFG register to lead device to *Deep Fail Safe* state (for instance VPRETSD_I = 1 and VPRETDFS = 1).

Below is an exhaustive list of conditions that make the device leave the *Deep Fail Safe* state for the *load fuse* state:

- WAKE1 event: resumes if WK1DFS_DIS_OTP = 0 and WAKE1 pin is toggled from low to high or from high to low logic level.
- Infinite auto-retry mode: the FS26 makes attempts to resume periodically and RETRY_CNT[7:0] increments every try. Once the RETRY_CNT[7:4] reaches the RETRY_MSK_OTP[3:0] value, the RETRY_CNT[7:0] time value is clamped and retries occur infinitely to the last clamped retry frequency (RETRY_MSK_OTP[3:0]) until a valid resume condition is detected. The OTP configuration to select this mode is RETRY_DIS_OTP = 0 and RETRY_MODE_OTP = 1.
- Limited auto-retry mode: the FS26 makes attempts to resume while RETRY_CNT[7:4] is smaller than RETRY_MSK_OTP[3:0]. When the RETRY_CNT[7:4] reaches the RETRY_MSK_OTP[3:0] value, the FS26 stays in the *Deep Fail Safe* state until a power-on reset event occurs ($V_{BOS} < V_{BOS\_POR}$). The OTP configuration to select this mode is RETRY_DIS_OTP = 0 and RETRY_MODE_OTP = 0.

Example: the first time the device enters *Deep Fail Safe* state, it will try to exit this state every 100 ms, and RETRY_CNT[7:0] increments at each attempt. After 16 consecutive failed attempts, RETRY_CNT[7:4] increments and the counter uses the next value of 200 ms, and so on, until RETRY_CNT[7:4] = RETRY_MSK_OTP[3:0].

Note: the retry counter RETRY_CNT[7:0] is divided in two parts. RETRY_CNT[7:4] represents the timing the counter is currently using (100 ms, 200 ms, and so on) and RETRY_CNT[3:0] is the number of attempts performed at the current used timing. RETRY_CNT[7:0] can be read as the total number of attempts performed by the device since the first *Deep Fail Safe* entry.

15.2 Application flowchart

In an application, the debug pin is connected to ground and a watchdog refresh is required as soon as the *initialization phase* is closed. The system enters *normal mode* once the safety outputs are released. Figure 14 is a high-level flowchart illustrating entry into *normal mode* in the application.

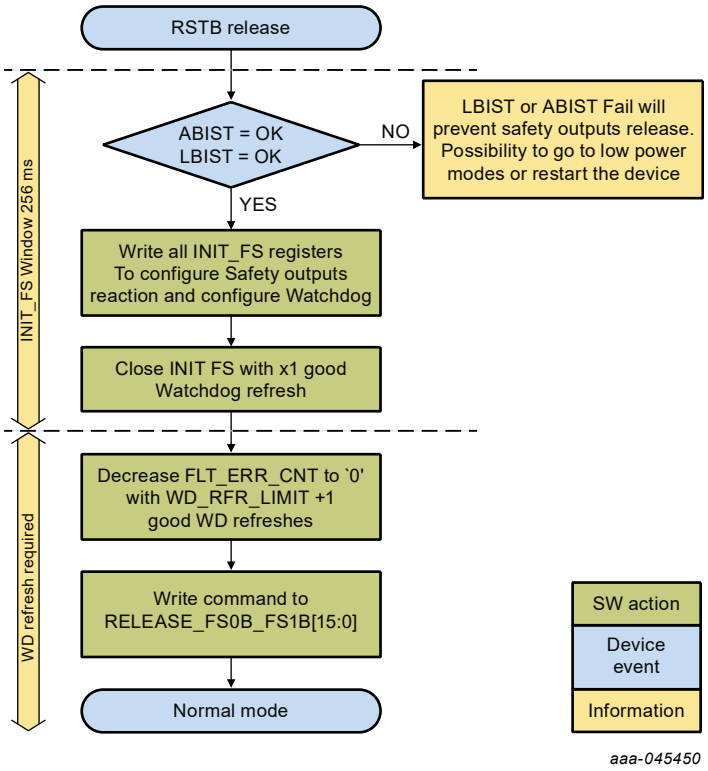

Figure 14. Application flowchart

15.3 Input power topology

The FS26 provides two input topologies to address various system needs. A reverse protection Schottky diode (D_{BAT}) between battery voltage (V_{BAT}) and the FS26 is required. Depending on the system configuration, the FS26 can obtain V_{SUP} in two main configurations:

1. The switching boost controller (VBST) can be used as the front-end supply to support system cranking events with voltage drops down to 2.7 V at the V_{BST_IN} input.
   When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation when V_{SUP} > VBST, the boost controller stops switching and operates in pass-through mode.

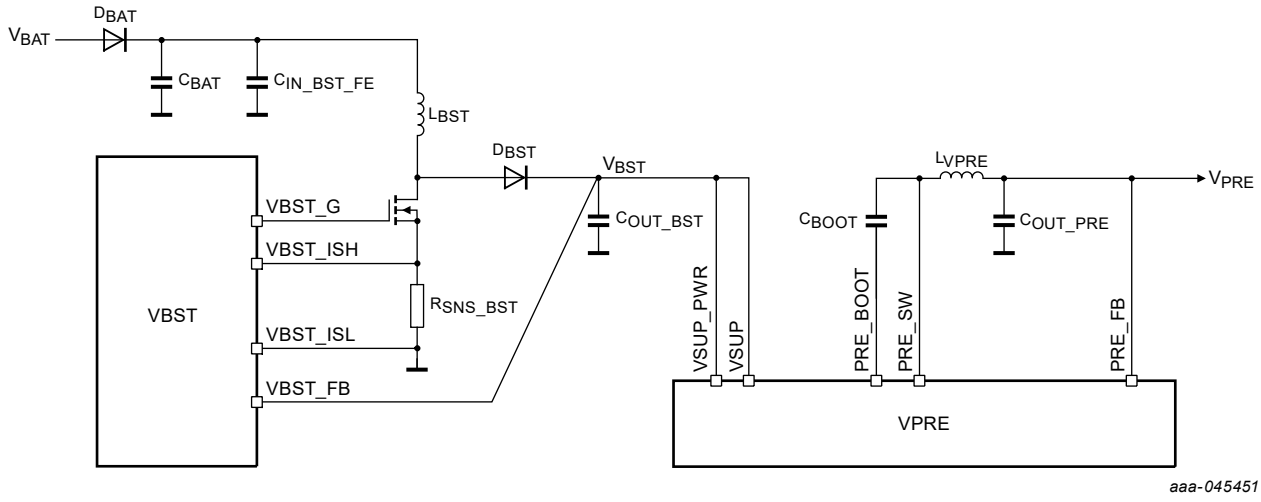

Figure 15. Input topology: front-end boost controller

When V_{SUP} < VBST, the boost controller starts switching to maintain V_{SUP} above the V_{SUP_UVH} threshold, thus ensuring system operation during crank profiles.

2. For systems with less severe or no cranking events, the input power can be applied directly to the VSUP pin. In this scenario, the FS26 can ensure functionality if V_{SUP} > V_{PREPWM} + V_{PRE_HDR} (Section 18.2 for V_{PRE_HDR}). The device will shut down if V_{PREPWM} < V_{PRE_UVL}. The reverse voltage protection diode and a PI-filter are needed to guarantee optimal EMI performance.

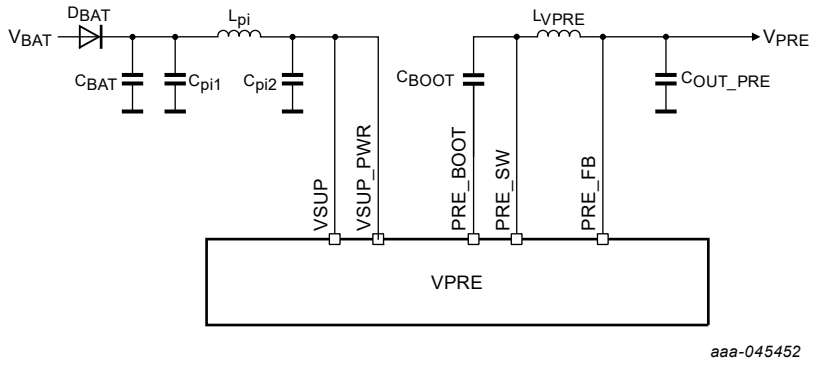

Figure 16. Input topology: direct VSUP connection

At the chip level, the power-up sequencing and operating thresholds are referenced to VSUP input. However, proper considerations should be made to ensure the system level requirements are met with respect to V_{BAT} voltage.

15.4 System power-up and power-down

When a voltage is applied to the VSUP pin, the FS26 starts its internal power-up biasing. As the internal best of supply (BOS) reaches regulation and the default OTP configuration is loaded, the system proceeds to turn on the output regulators based on the OTP configuration of the device. The regulators' power-up sequence is dependent on the input power topology used in the system:

With VBST used as the front-end supply

- VBST is enabled first and will ensure V_{SUP} > V_{SUP_UVH}.

- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start as set in the OTP power-up sequence configuration.

Direct connection to VSUP

- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start in their corresponding power-up slot as set in the OTP power-up sequence configuration.

15.4.1 Regulator power-up sequence

Seven slots are available to program the startup sequence of VCORE, LDO1, LDO2, VREF, TRK1, and TRK2, as well as the GPIO1 and GPIO2 signals for external control.

The power-up sequence starts from SLOT_0 to SLOT_6, with a TSLOT_OTP[1:0] delay between each slot. RSTB is released after SLOT_6. Regulators assigned to SLOT_7 / OFF are not started during the power-up sequence and can be enabled later in *normal mode* via a SPI command. When VBST is used in back-end supply, it can only be enabled via a SPI command once the device is in *normal mode*.

Each regulator is assigned to a slot by OTP configuration using the dedicated OTP bits. Each slot is executed regardless of whether a regulator is assigned to a slot or not. Slots can be bypassed with SLOT_BYP_OTP[2:0]. A regulator assigned to a bypassed slot will not start in the power-up sequence.

When the last power-up slot is completed, monitoring of the voltages is enabled. If the soft start of a regulator is not achieved and the output voltage is still below the UV monitoring, the UV is detected and reported in the corresponding flag. Therefore, NXP recommends clearing all the UV flags at each startup during *initialization phase*.

When VCORE is enabled, the bootstrap capacitor must be charged. Therefore, the VCORE regulator output starts to ramp-up with a delay of 100 µs from the beginning of the slot.

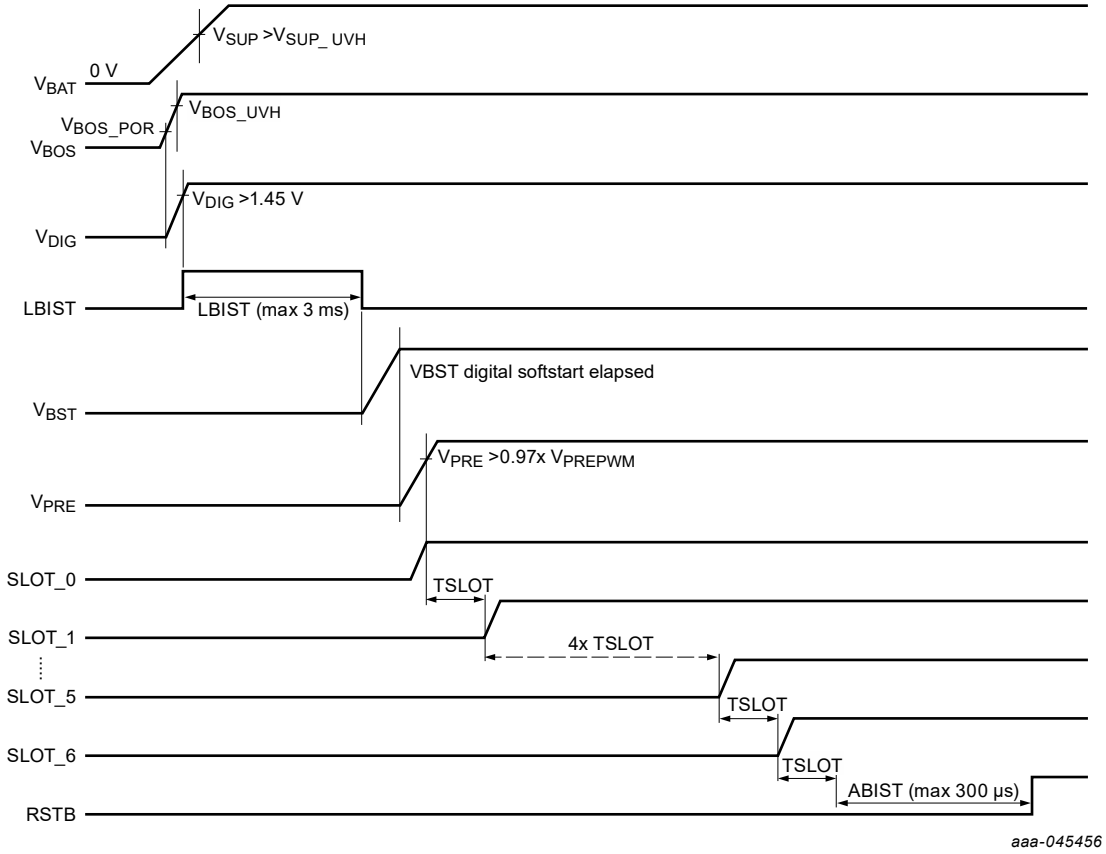

Figure 17. Power-up example with VBST as front-end supply

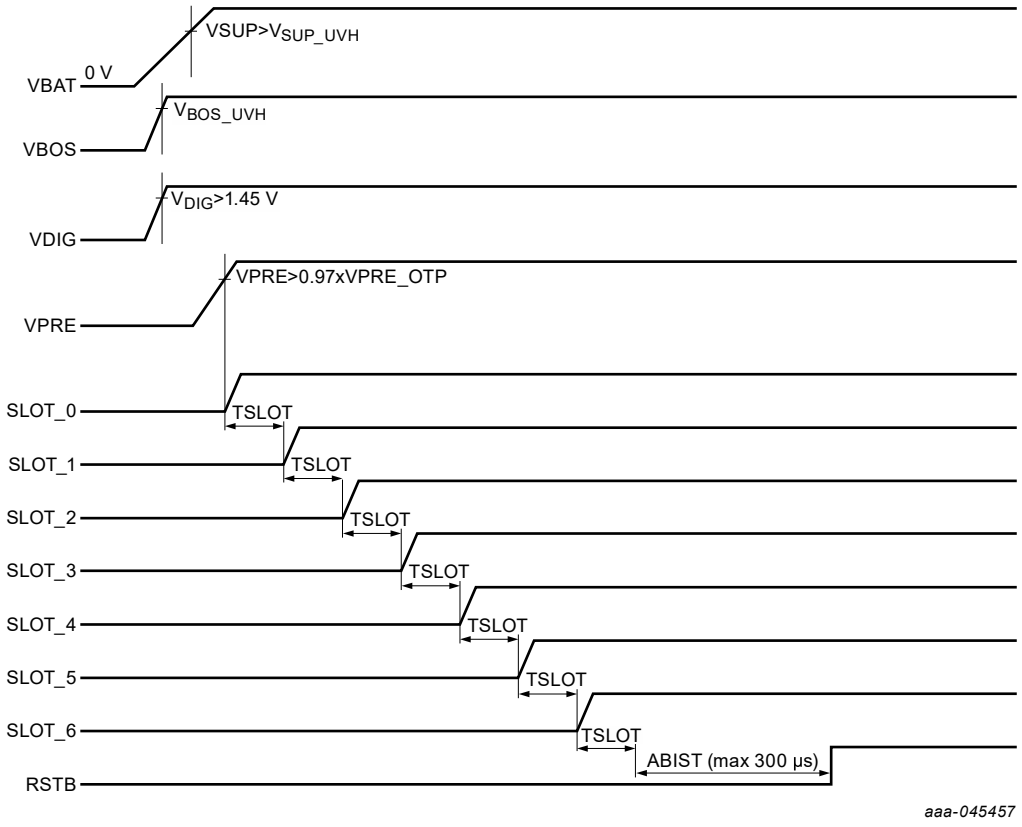

Figure 18. Power-up example with direct battery supply

To reduce the power-up timing, SLOT_BYP_OTP[2:0] setting is provided to bypass the unused slots. Devices slots jumps from the slot SLOT_BYP_OTP[2:0] to *normal mode*, bypassing SLOT_X to SLOT_6.

Once the power-up sequence is completed, the Main state machine is in *normal mode*, which is the application running mode with all the regulators ON.

15.4.2 System power-down sequence

During a power-down event, the device uses the same slot bits to turn off the voltage regulators, in reverse order from the power-up sequence.

If a slot bypass configuration is enabled, the device will start the power-down sequence from the selected slot in the OTP configuration.

When powering down to the *standby mode*, VPRE remains enabled. LDO1 and LDO2 can be programmed to also remain enabled during the *standby mode*. GPIO1 and GPIO2 can also remain in the same state that they were in, in *normal mode*. All other regulators are disabled as defined by the slot bits.

When powering down into the *LPOFF mode*, all voltage regulators are disabled as described in the power-down sequence. Once the voltage regulators in the sequencer are disabled, the VPRE will start powering off, followed by the VBST if it is used as the front-end supply.

If VBST is used in back-end mode, the regulator will be turned off in the first power-down slot.

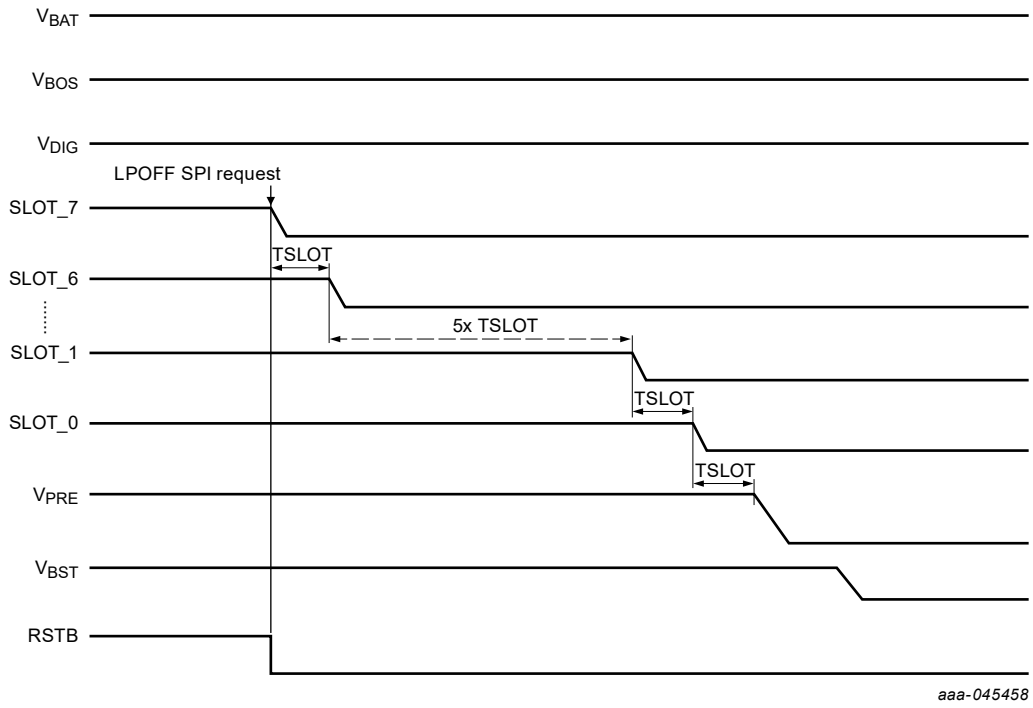

Figure 19. Power-down example with VBST as front-end supply

15.5 Wake-up sources

The FS26 has several selectable wake-up sources from the Low-power modes:

- WAKEx pin:
  - The WAKEx pins can be configured to detect wake-up events internal or external to the ECU.
  - The WAKEx pins can detect wake-up event on high level or low level.
- GPIOx pin:
  - The GPIOx pins can be configured as inputs to detect wake-up events internal to the ECU.
  - The GPIOx pins can detect wake-up event on high level or low level.
- SPI chip select wake-up (only when VDDIO is supplied):
  - When the SPI wake up is enabled, the device wakes up with any activity on the SPI bus (transition from high to low of CSB pin).
  - In case of a SPI wake up, the first SPI command is ignored, and the FS26 will be able to respond to the subsequent SPI commands after 1.5 ms.
- Long Duration Timer (LDT) expired:
  - Wake up from the LDT is available (part number dependent).
  - When the LDT is enabled, it can be configured to generate a wake-up event when the timer expires. This feature allows the system to perform cyclic system verifications while it is in the Low-power mode.

15.6 SPI communication

The FS26 uses a 32-bit SPI, with the following arrangement:

MOSI (Main Out, Secondary In) bits:

- Bit 31: Main or fail-safe registers selection
- Bits 30 to 25: Register address

- Bit 24: Read/Write (for reading bit 24 = 0; for writing bit 24 = 1)
- Bits 23 to 8: Control bits
- Bits 7 to 0: Cyclic redundant check (CRC)

MISO (Main In, Secondary Out) bits:

- Bits 31 to 24: General device status (see Table 12)
- Bits 23 to 8: Extended device status, or device internal control register content or device flags
- Bits 7 to 0: Cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is the primary driving MOSI and FS26 is the secondary driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge, MSB first. In a write command, MISO[23:8] bits are the previous register bits and MISO[7:0] is the CRC of the message sent by the FS26. In a read command, MOSI[23:8] bits are all 0 and MOSI[7:0] is the CRC of the message sent by the MCU. Figure 20 and Figure 21 describe the SPI communication protocol for writing data into the FS26 or reading data from the FS26.

The FS_EN bit is set high as soon as the fail-safe state machine enters Enable monitoring state. The bit remains enabled during the normal operation until the system has successfully moved into any of the low power states.

In all other states, FS_EN = 0.

The M_AVAL bit is set high as soon as the main state machine is in *normal mode* state. In all other states, this bit is set to 0.

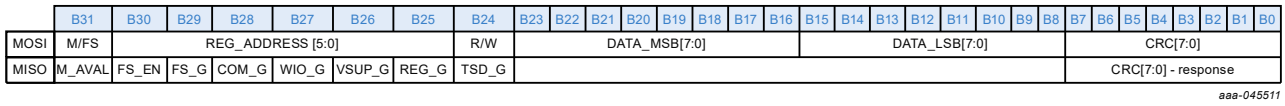

Figure 20. SPI write operation protocol

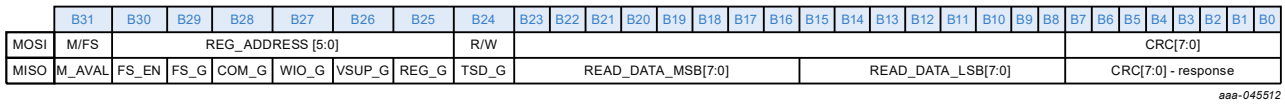

Figure 21. SPI read operation protocol

Table 11. MOSI general bit description

Bit	Symbol	Description	
31	M/FS	**Device domain access**	
		0	Main domain register map
		1	Fail-safe domain register map
30 to 25	REG_ADDESS[5:0]	**Register address**	
		See Table 15 for main domain register mapping	
24	R/W	**Operation requested**	
		0	Read
		1	Write
23 to 8	DATA[15:0]	**Register data**	
7 to 0	CRC[7:0]	**Cyclic redundancy check data sent by MCU**	

Table 12. MISO general device status bit descriptions

Bit	Symbol	Description	
31	M_AVAL	**Main state machine availability**	
		0	Not available (the main state machine is not in *normal mode*)
		1	Available and able to respond (the main state machine is in *normal mode*)
		Reset on power-on reset (POR_M)	
30	FS_EN	**Fail-safe state machine status**	
		0	Fail-safe state machine is not available.
		1	Fail-safe state machine is available and able to respond
		Reset on power-on reset (POR_M)	
29	FS_G	**Event notification from the fail-safe domain**	
		0	No event reported in the fail-safe domain
		1	Event reported in the fail-safe domain
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Flags Reporting: VPRE_OV, VPRE_UV, CORE_OV, CORE_UV, LDO1_OV, LDO1_UV, LDO2_OV, LDO2_UV, TRK1_OV, TRK1_UV, TRK2_OV, TRK2_UV, REF_OV, REF_UV, EXT_OV, EXT_UV, BAD_WD_DATA, BAD_WD_TIMING, FCCU12, FCCU1, FCCU2, ERRMON, ABIST1_PASS, ABIST2_PASS, LBIST_STATUS[1:0]	
28	COM_G	**Event notification from the M_COM_FLG**	
		0	No event reported in M_COM_FLG
		1	Event reported in the M_COM_FLG
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_COM_FLG	
		Flags Reporting: MSPI_CRC_I, MSPI_CLK_I, MSPI_REQ_I	
27	WIO_G	**Event notification from the M_WIO_FLG register**	
		0	No event reported ino M_WIO_FLG register
		1	Event reported in the M_WIO_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_WIO_FLG	
		Flags Reporting: WUEVENT[3:0], LDT_I, GPIO2_I, GPIO1_I, WK2_I, WK1_I	
26	VSUP_G	**Event notification from the M_VSUP_FLG register**	
		0	No event reported in M_VSUP_FLG register
		1	Event reported in the M_VSUP_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_VSUP_FLG	
		Flags Reporting: VBOSUVH_I, VSUPOV_I, VSUPUV6_I, VSUPUVH_I	
25	REG_G	**Event notification from the M_REG_FLG register**	
		0	No event reported in M_REG_FLG register

Table 12. MISO general device status bit descriptions...*continued*

Bit	Symbol	Description	
		1	Event reported in the M_REG_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_REG_FLG	
		Flags Reporting: VBSTOV_I, VPREUVH_I, VPREOC_I, TRK2OC_I, TRK1OC_I, COREOC_I, LDO2OC_I, LDO1OC_I, VBSTOC_I	
24	TSD_G	**Event notification from the M_TSD_FLG register**	
		0	No event reported in M_TSD_FLG register
		1	Event reported in the M_TSD_FLG register
		Reset on power-on reset (POR_M), cleared when all individual bits are cleared	
		Source Register: M_TSD_FLG	
		Flags Reporting: TWARN_I, GPIO1TSD_I, VPRETSD_I, TRK2TSD_I, TRK1TSD_I, CORETSD_I, LDO2TSD_I, LDO1TSD_I	

15.6.1 Cyclic redundancy check

An 8-bit cyclic redundancy check (CRC) is required for each Write and Read SPI command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

Figure 22 is an example of CRC encoding HW implementation:

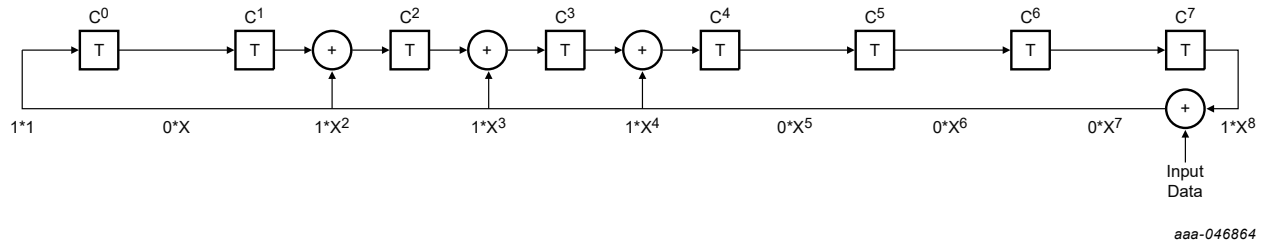

Figure 22. CRC encoder example

The effect of the CRC encoding procedure is shown in Table 13. The seed value is appended into the most significant bits of the shift register.

Table 13. Data preparation for CRC encoding

Seed	M/FS	Register Address	Read/Write	DATA_MSB	DATA_LSB
0xFF	Bit[31]	Bits[30:25]	Bit[24]	Bits[23:16]	Bits[15:8]

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 32-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, the initial CRC byte composed of zeros is replaced and the CRC is transmitted.

Procedure for CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.

2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

- If the shift register contains all zeros, the CRC is correct.
- If the shift register contains a value other than zero, the CRC is incorrect.

15.6.2 SPI electrical characteristics and timing diagram

Table 14. SPI Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Interface I/O input supply					
V_{DDIO}	VDDIO supply voltage range	3.0	—	5.5	V
Static Electrical Characteristics					
V_{SPI_VIL}	CSB, SCLK, MOSI low level input voltage threshold	—	—	0.3 x V_{DDIO}	V
V_{SPI_VIH}	CSB, SCLK, MOSI high level input voltage threshold	0.7 x V_{DDIO}	—	—	V
R_{SCLK_IPD}	SCLK internal pull-down current source	7	10	13	µA
V_{MISO_VOH}	MISO high output voltage (I = 2.0 mA)	V_{DDIO} - 0.4	—	—	V
V_{MISO_VOL}	MISO low output voltage (I = 2.0 mA)	—	—	0.4	V
I_{MISO_LEAK}	3-state leakage current (VDDIO = 5.0 V)	- 5.0	—	5.0	µA
R_{SPI_PU}	CSB, MOSI internal pull-up (pull-up to VDDIO)	190	450	800	kΩ
C_{SPI}	Input capacitor at CSB, SCLK, MOSI	—	—	10	pF
Dynamic Electrical Characteristics					
F_{SPI}	SPI operation frequency (50 % DC)	0.5	—	10	MHz
t_{CLH}	Minimum time SCLK = HIGH	50	—	—	ns
t_{CLL}	Minimum time SCLK = LOW	50	—	—	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns
t_{CSDV}	CSB = low to data at MISO active	—	—	70	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	70	—	—	ns
t_{HCLCL}	SCLK change L/H after CSB = low	70	—	—	ns
t_{SCLD}	SDI input setup time (SCLK change H/L after MOSI data valid)	35	—	—	ns
t_{HCLD}	SDI input hold time (MOSI data hold after SCLK change H/L)	35	—	—	ns
t_{SCLCL}	SCLK low before CSB high	90	—	—	ns
t_{HCLCH}	SCLK high after CSB high	90	—	—	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	—	—	75	ns
t_{ONCSB}	CSB min. high time	500	—	—	ns
t_{CBS_MIN}	CSB filter time	10	—	40	ns

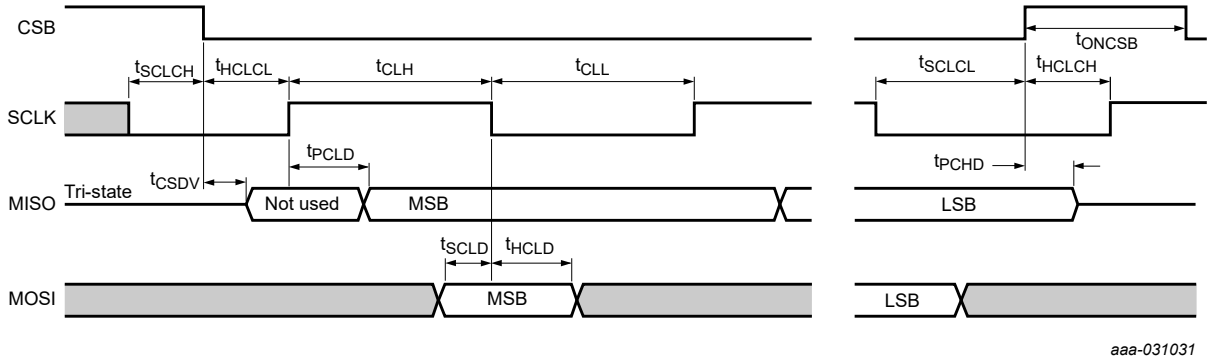

Figure 23. SPI timing diagram

16 Register mapping

16.1 Register map overview

Table 15. Main SPI register map overview

Register Name	ADDRESS (Hex)	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
M_DEVICEID	00	FULL_LAYER_REV [15:13]			METAL_LAYER_REV [12:10]			FAM_ID [9:6]				DEV_ID [5:0]					
M_PROGID	01	PROG_IDH [15:8]								PROG_IDL [7:0]							
M_STATUS	02	TWARN_S	VDBG_VOLT_S	VBST_ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S	VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S
M_TSD_FLG	03	TWARN_I	0	0	0	0	0	0	0	0	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
M_TSD_MSK	04	TWARN_M	0	0	0	0	0	0	0	0	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
M_REG_FLG	05	0	0	0	0	0	0	0	VBSTOV_I	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
M_REG_MSK	06	0	0	0	0	0	0	0	VBSTOV_M	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
M_VSUP_FLG	07	0	0	0	0	0	0	0	0	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
M_VSUP_MSK	08	0	0	0	0	0	0	0	0	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
M_WIO_FLG	09	WU_CLR	0	0	0	WUEVENT [11:8]				0	0	0	LDT_I	IO2_I	IO1_I	WK2_I	WK1_I
M_WIO_MSK	0A	0	0	0	0	0	0	0	0	0	0	0	LDT_M	IO2_M	IO1_M	WK2_M	WK1_M
M_COM_FLG	0B	0	0	0	0	0	0	0	0	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
M_COM_MSK	0C	0	0	0	0	0	0	0	0	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
M_SYS_CFG	0D	RETRY_CNT [15:8]								RETRY_CLR	0	0	INTB_TEST	INT_PWIDTH	FSS_FMOD	0	FSS_EN
M_TSD_CFG	0E	0	0	0	0	0	0	0	0	0	0	VPR ETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
M_REG_CFG	0F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VREF_PD	VBST_TMD
M_WIO_CFG	10	0	0	0	0	GPIO2 WUPOL	GPIO1 WUPOL	WAKE2 POL	WAKE1 POL	0	0	CSBWUEN	LDTWUEN	GPIO2 WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
M_REG_CTRL1	11	0	0	GPIO2LP_ON	GPIO1LP_ON	0	0	GPIO2HI	GPIO1HI	VREFEN	VBSTEN	0	TRK2EN	TRK1EN	COREEN	LDO2EN	LDO1EN
M_REG_CTRL2	12	0						IO2LO	IO1LO	VREFDIS	VBSTDIS	0	TRK2DIS	TRK1DIS	COREDIS	LDO2DIS	LDO1DIS
M_AMUX_CTRL	13	0	0	0	0	0	0	0	0	0	AMUX_EN	AMUX_DIV	AMUX [4:0]				

Table 15. Main SPI register map overview*...continued*

M_LDT_CFG1	14	LDT_AFTER_RUN [15:0]													
M_LDT_CFG2	15	LDT_WUP_H [15:0]													
M_LDT_CFG3	16	0	0	0	0	0	0	0	0	LDT_WUP_L [7:0]					
M_LDT_CTRL	17	0	0	0	0	0	0	0	0	0	LDT_FNCT [6:4]	LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
M_MEMORY0	18	MEM0 [15:0]													
M_MEMORY1	19	MEM1 [15:0]													

Register map overview legend

Bit types	READ / WRITE	READ	WRITE

16.2 Main register mapping

16.2.1 M_DEVICEID

Table 16. M_DEVICEID register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FULL_LAYER_REV[2:0]			METAL_LAYER_REV[2:0]			FAM_ID[3:0]				DEV_ID[5:0]					
Reset	0	1	1	0	0	1	0	1	1	1	OTP	OTP	OTP	OTP	OTP	OTP

Go to main register map

Table 17. M_DEVICEID register bit description

Bit	Symbol	Value	Description
15 to 13	FULL_LAYER_REV[2:0]	Full layer mask revision	
		3h	Pass C silicon for A release version
		1h	Pass A silicon for H release version
		Reset condition: N/A	
12 to 10	METAL_LAYER_REV[2:0]	Metal mask revision	
		1h	Rev X.1 for A release version
		0h	Rev X.0 for H release version
		Reset condition: N/A	
9 to 6	FAM_ID[3:0]	Device family Identification	
		7h	FS26 family. Defined on metal mask.
		Reset condition: N/A	
5 to 0	DEV_ID[5:0]	Device ID	
		FS26 version dependent. See Table 1	
		Reset condition: N/A	

16.2.2 M_PROGID

Table 18. M_PROGID register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PROG_IDH[7:0]								PROG_IDL[7:0]							
Reset	OTP								OTP							

Go to main register map

Table 19. M_PROGID register bit description

Bit	Symbol	Description
15 to 8	PROG_IDH[7:0]	Higher byte to set the first letter for the OTP ID code (see Table 96)
		PROG_IDH_OTP[7:0]
		Reset condition: N/A
7 to 0	PROG_IDL[7:0]	Lower byte to set the second letter for OTP ID code (see Table 97)
		PROG_IDL_OTP[7:0]
		Reset condition: N/A

16.2.3 M_STATUS

Table 20. M_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	TWARN_S	VDBG_VOLT_S	VBST_ ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 21. M_STATUS register bit description

Bit	Symbol	Value	Description
15	TWARN_S	Real-time status of Thermal Warning flag	
		0h	$T_J < T_{WARN}$
		1h	$T_J > T_{WARN}$
		Real-time information	
14	VDBG_VOLT_S	Real-time status of DEBUG pin voltage	
		0h	DEBUG pin voltage $V_{DEBUG} < V_{NORM}$
		1h	DEBUG pin voltage $V_{DEBUG} > V_{DBG}$
		Real-time information	
13	VBST_ACTIVE_S	Real-time status of VBST switching status	
		0h	VBST switching node is not switching
		1h	VBST switching node is switching
		Real-time information	
12	VBSTFB_UV_S	Real-time status of VBST_FB pin	
		0h	VBST_FB pin voltage $V_{BST} > V_{BST\_UV\_TH}$
		1h	VBST_FB pin voltage $V_{BST} < V_{BST\_UV\_TH}$
		Real-time information	
11	WK2_S	Real-time status of WAKE2 pin	
		0h	WAKE2 is low (V_{IL_WAKEx})
		1h	WAKE2 is high (V_{IH_WAKEx})
		Real-time information	
10	WK1_S	Real-time status of WAKE1 pin	
		0h	WAKE1 is low (V_{IL_WAKEx})
		1h	WAKE1 is high (V_{IH_WAKEx})
		Real-time information	
9	GPIO2_S	GPIO2 pin status	
		0h	GPIO2 is low (V_{IL_GPIOx})
		1h	GPIO2 is high (V_{IH_GPIOx})
		Real-time information	
8	GPIO1_S	GPIO1 pin status	
		0h	GPIO1 is low (V_{IL_GPIOx})
		1h	GPIO1 is high (V_{IH_GPIOx})
		Real-time information	
7	VREF_S	Real time status of VREF regulator	

Table 21. M_STATUS register bit description*...continued*

Bit	Symbol	Value	Description
		0h	VREF is disabled
		1h	VREF is enabled
		Real-time information	
6	VBST_S	Real time status of VBST regulator	
		0h	VBST is disabled
		1h	VBST is enabled
		Real-time information	
5	VPRE_S	Real time status of VPRE regulator	
		0h	VPRE is disabled
		1h	VPRE is enabled
		Real-time information	
4	TRK2_S	Real time status of TRK2 regulator	
		0h	TRK2 is disabled
		1h	TRK2 is enabled
		Real-time information	
3	TRK1_S	Real time status of TRK1 regulator	
		0h	TRK1 is disabled
		1h	TRK1 is enabled
		Real-time information	
2	CORE_S	Real time status of VCORE regulator	
		0h	VCORE is disabled
		1h	VCORE is enabled
		Real-time information	
1	LDO2_S	Real time status of LDO2 regulator	
		0h	LDO2 is disabled
		1h	LDO2 is enabled
		Real-time information	
0	LDO1_S	Real time Status of LDO1 regulator	
		0h	LDO1 is disabled
		1h	LDO1 is enabled
		Real-time information	

16.2.4 M_TSD_FLG

Table 22. M_TSD_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_I	0	0	0	0	0	0	0
Read	TWARN_I	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Read	RESERVED	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 23. M_TSD_FLG register bit description

Bit	Symbol	Value	Description
15	TWARN_I	Central temperature sensor thermal warning flag Set when $T_J > T_{WARN}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
6	GPIO1TSD_I	GPIO1 thermal shutdown flag. Set when local $T_J > TSD_{GPIO1}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
5	VPRETSD_I	VPRE thermal shutdown flag. Set when local $T_J > TSD_{PRE}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
4	TRK2TSD_I	TRK2 thermal shutdown flag. Set when local $T_J > TSD_{TRKx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
3	TRK1TSD_I	TRK1 thermal shutdown flag. Set when local $T_J > TSD_{TRKx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
2	CORETSD_I	VCORE thermal shutdown flag. Set when local $T_J > TSD_{CORE}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
1	LDO2TSD_I	LDO2 thermal shutdown flag. Set when local $T_J > TSD_{LDOx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
0	LDO1TSD_I	LDO1 thermal shutdown flag. Set when local $T_J > TSD_{LDOx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	

16.2.5 M_TSD_MSK

Table 24. M_TSD_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_M	0	0	0	0	0	0	0
Read	TWARN_M	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Read	RESERVED	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 25. M_TSD_MSK register bit description (default value in bold)

Bit	Symbol	Value	Description
15	TWARN_M	Inhibit interrupt (INTB pulse) related to TWARN_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
6	GPIO1TSD_M	Inhibit interrupt (INTB pulse) related to GPIO1TSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
5	VPRETSD_M	Inhibit interrupt (INTB pulse) related to VPRETSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
4	TRK2TSD_M	Inhibit interrupt (INTB pulse) related to TRK2TSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	TRK1TSD_M	Inhibit interrupt (INTB pulse) related to TRK1TSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	CORETSD_M	Inhibit interrupt (INTB pulse) related to CORETSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	LDO2TSD_M	Inhibit interrupt (INTB pulse) related to LDO2TSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	LDO1TSD_M	Inhibit interrupt (INTB pulse) related to LDO1TSD_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

16.2.6 M_REG_FLG

Table 26. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBSTOV_I
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
Read	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 27. M_REG_FLG register bit description

Bit	Symbol	Value	Description
8	VBSTOV_I	VBST overvoltage flag. Set when $V_{BST} > V_{BST\_OV\_TH}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
7	VPREUVH_I	VPRE undervoltage flag. Set when $V_{PRE\_PWM} < V_{PRE\_UVH}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
6	VBSTOC_I	VBST overcurrent event. Set when VBST_ISH pin voltage minus VBST_ISL pin voltage > $V_{BST\_ILIM\_TH}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
5	VPREOC_I	VPRE overcurrent event. Set when $I_{PRE\_PWM} > I_{PRE\_OC\_FLAG}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
4	TRK2OC_I	TRK2 overcurrent event. Set when $I_{TRK2} > I_{LIM\_TRKx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
3	TRK1OC_I	TRK1 overcurrent event. Set when $I_{TRK1} > I_{LIM\_TRKx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
2	COREOC_I	VCORE overcurrent event. Set when $I_{CORE} > I_{CORE\_PEAK\_0A8}$ (for FS260x and FS261x) or $I_{CORE} > I_{CORE\_PEAK\_1A65}$ (for FS262x and FS263x)	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
1	LDO2OC_I	LDO2 overcurrent event. Set when $I_{LDO2} > I_{LIM\_LDOx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	
0	LDO1OC_I	LDO1 overcurrent event. Set when $I_{LDO1} > I_{LIM\_LDOx}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on write 1	

16.2.7 M_REG_MSK

Table 28. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBSTOV_M
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Read	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 29. M_REG_MSK register bit description

Bit	Symbol	Value	Description
8	VBSTOV_M	Inhibit interrupt (INTB pulse) related to VBSTOV_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
7	VPREUVH_M	Inhibit interrupt (INTB pulse) related to VPREUVH_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
6	VBSTOC_M	Inhibit interrupt (INTB pulse) related to VBSTOC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
5	VPREOC_M	Inhibit interrupt (INTB pulse) related to VPREOC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
4	TRK2OC_M	Inhibit interrupt (INTB pulse) related to TRK2OC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	TRK1OC_M	Inhibit interrupt (INTB pulse) related to TRK1OC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	COREOC_M	Inhibit interrupt (INTB pulse) related to COREOC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

Table 29. M_REG_MSK register bit description*...continued*

Bit	Symbol	Value	Description
1	LDO2OC_M	Inhibit interrupt (INTB pulse) related to LDO2OC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	LDO1OC_M	Inhibit interrupt (INTB pulse) related to LDO1OC_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

16.2.8 M_VSUP_FLG

Table 30. M_VSUP_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 31. M_VSUP_FLG register bit description

Bit	Symbol	Value	Description
3	VBOSUVH_I	VBOS undervoltage flag. Set when $V_{BOS} < V_{BOS\_UVH}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
2	VSUPOV_I	VSUP overvoltage flag. Set when $V_{SUP} > V_{SUP\_OV}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
1	VSUPUV6_I	VSUP undervoltage (6 V) flag. Set when $V_{SUP} < V_{SUP\_UV6}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	
0	VSUPUVH_I	VSUP undervoltage flag. Set when $V_{SUP} < V_{SUP\_UVH}$	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M) or clear on Write (write 1)	

16.2.9 M_VSUP_MSK

Table 32. M_VSUP_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 33. M_VSUP_MSK register bit description

Bit	Symbol	Value	Description
3	VBOSUVH_M	Inhibit interrupt (INTB pulse) related to VBOSUVH_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	VSUPOV_M	Inhibit interrupt (INTB pulse) related to VSUPOV_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	VSUPUV6_M	Inhibit interrupt (INTB pulse) related to VSUPUV6_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	VSUPUVH_M	Inhibit interrupt (INTB pulse) related to VSUPUVH_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

16.2.10 M_WIO_FLG

Table 34. M_WIO_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WU_CLR	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	WUEVENT[3:0]			
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	LDT_I	GPIO2_I	GPIO1_I	WK2_I	WK1_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 35. M_WIO_FLG register bit description

Bit	Symbol	Value	Description
15	WU_CLR	Clear wake-up flags	
		0h	Do nothing
		1h	Clear all wake-up flags
		Reset on power-on reset (POR_M), self-clear	
11 to 8	WUEVENT[3:0]	Wake-up event source. Generates interrupt (INTB pulse)	
		0h	No wake up detected
		1h	WAKE1
		2h	WAKE2
		3h	GPIO1
		4h	GPIO2
		5h	LDT expired
		6h	SPI activity
		8h	DFS Recovery
		Fh	BATTERY fail: Reports when the device has lost valid V_{SUP} and Main state machine is reset.
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
4	LDT_I	LDT expired event flag	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
3	GPIO2_I	GPIO2 event flag	
		0h	No event on GPIO2
		1h	Event on GPIO2 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
2	GPIO1_I	GPIO1 event flag	
		0h	No event on GPIO1
		1h	Event on GPIO1 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
1	WK2_I	WAKE2 event flag	
		0h	No event on WAKE2
		1h	Event on WAKE2 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	
0	WK1_I	WAKE1 event flag	
		0h	No event on WAKE1
		1h	Event on WAKE1 has occurred. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), go to *standby mode*, go to *LPOFF mode*, or WU_CLR write 1	

16.2.11 M_WIO_MSK

Table 36. M_WIO_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M

Bit	7	6	5	4	3	2	1	0
Read	RESERVED	RESERVED	RESERVED	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 37. M_WIO_MSK register bit description (default)

Bit	Symbol	Value	Description
4	LDT_M	Inhibit interrupt (INTB pulse) related to LDT_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
3	GPIO2_M	Inhibit interrupt (INTB pulse) related to GPIO2_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
2	GPIO1_M	Inhibit interrupt (INTB pulse) related to GPIO1_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
1	WK2_M	Inhibit interrupt (INTB pulse) related to WK2_I event	
		0h	**Interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	WK1_M	Inhibit interrupt (INTB pulse) related to WK1_I event	
		0h	**interrupt NOT MASKED (default)**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

16.2.12 M_COM_MSK

Table 38. M_COM_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 39. M_COM_MSK register bit description (default value in bold)

Bit	Symbol	Value	Description
2	MSPI_CRC_M	Inhibit interrupt (INTB pulse) related to MSPI_CRC_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED

Table 39. M_COM_MSK register bit description (default value in bold)*...continued*

Bit	Symbol	Value	Description
		Reset on power-on reset (POR_M)	
1	MSPI_CLK_M	Inhibit interrupt (INTB pulse) related to MSPI_CLK_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	
0	MSPI_REQ_M	Inhibit interrupt (INTB pulse) related to MSPI_REQ_I event	
		0h	**Interrupt NOT MASKED**
		1h	Interrupt MASKED
		Reset on power-on reset (POR_M)	

16.2.13 M_COM_FLG

Table 40. M_COM_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 41. M_COM_FLG register bit description

Bit	Symbol	Value	Description
2	MSPI_CRC_I	Main domain SPI message corrupted (CRC not valid) flag	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	
1	MSPI_CLK_I	Main domain SPI wrong number of clock pulses flag	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	
0	MSPI_REQ_I	Main domain SPI access violation (write to an invalid register) flag	
		0h	Event not detected
		1h	Event detected. Generates interrupt (INTB pulse)
		Reset on power-on reset (POR_M), or clear on write 1	

16.2.14 M_SYS_CFG

Table 42. M_SYS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RETRY_CNT[7:0]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	RETRY_CLR	0	0	INTB_TEST	INT_PWIDTH	FSS_FMOD	0	FSS_EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	INT_PWIDTH	FSS_FMOD	RESERVED	FSS_EN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 43. M_SYS_CFG register bit description

Bit	Symbol	Value	Description
15 to 8	RETRY_CNT[7:0]	RETRY_CNT[7:0] indicates the total number of retries attempts (value) RETRY_CNT[7:4] indicates the current duration between two retries (description)	
		0xh	**100 ms (default)**
		1xh	200 ms
		2xh	400 ms
		3xh	800 ms
		4xh	1600 ms
		5xh	3200 ms
		6xh	6400 ms
		7xh	12800 ms
		8xh	25600 ms
		9xh	51200 ms
		Axh	102400 ms
		Bxh	204800 ms
		Cxh	409600 ms
		Dxh	819200 ms
		Exh	1638400 ms
		Fxh	3276800 ms
		Reset on power-on reset (POR_M) or RETRY_CLR write 1	
7	RETRY_CLR	Clear retry counter RETRY_CNT[7:0]	
		0h	No effect
		1h	Clear retry counter
		Reset on power-on reset (POR_M), self-clear	
4	INTB_TEST	Manual test of INTB	
		0h	No effect
		1h	Enable manual test. Generate a pulse of duration t_{INTB_PULSE} at INTB pin for test purpose.
		Reset on power-on reset (POR_M), self-clear	
3	INT_PWIDTH	INTB pulse duration t_{INTB_PULSE}	
		0h	**25 µs (default)**
		1h	100 µs
		Reset on power-on reset (POR_M)	
2	FSS_FMOD	Frequency modulation F_{OSC_MOD} during Frequency Spread Spectrum Operation	
		0h	**High-frequency oscillator divided by 768 (default)**
		1h	High-frequency oscillator divided by 192
		Reset on power-on reset (POR_M)	
0	FSS_EN	Frequency Spread Spectrum enable	
		0h	**FSS is disabled (default)**
		1h	FSS is enabled
		Reset on power-on reset (POR_M)	

16.2.15 M_TSD_CFG

Table 44. M_TSD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Read	RESERVED	RESERVED	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Reset	0	0	OTP	OTP	OTP	OTP	OTP	OTP

Go to main register map

Table 45. M_TSD_CFG register bit description

Bit	Symbol	Value	Description
5	VPRETDFS	*Deep Fail Safe* request in case of VPRE Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (VPRETDFS_OTP)	
4	TRK2TDFS	*Deep Fail Safe* request in case of TRK2 Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (TRK1TDFS_OTP)	
3	TRK1TDFS	*Deep Fail Safe* request in case of TRK1 Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (TRK1TDFS_OTP)	
2	CORETDFS	*Deep Fail Safe* request in case of VCORE Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (CORETDFS_OTP)	
1	LDO2TDFS	*Deep Fail Safe* request in case of LDO2 Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (LDO1TDFS_OTP)	
0	LDO1TDFS	*Deep Fail Safe* request in case of LDO1 Thermal Shutdown	
		0h	Regulator disabled
		1h	Transition to DFS
		Load fuse state (LDO1TDFS_OTP)	

16.2.16 M_REG_CFG

Table 46. M_REG_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	VREF_PD	VBST_TMD
Read	0	0	0	0	0	0	VREF_PD	VBST_TMD
Reset	0	0	0	0	0	0	1	0

Go to main register map

Table 47. M_REG_CFG register bit description (default value in bold)

Bit	Symbol	Description
1	VREF_PD	VREF Internal pull-down configuration (R_{REF_DIS})
		0h Disable internal pull-down when VREF output is disabled
		1h Enable internal pull-down when VREF output is disabled
		Reset on power-on reset (POR_M)
0	VBST_TMD	VBST output verification mode
		h VBST output is regulated to the configured voltage set by OTP
		1h VBST regulate to 17 V to verify availability
		Reset on power-on reset (POR_M)

16.2.17 M_WIO_CFG

Table 48. M_WIO_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	GPIO2WUPOL	GPIO1WUPOL	WAKE2POL	WAKE1POL
Read	0	0	0	0	GPIO2WUPOL	GPIO1WUPOL	WAKE2POL	WAKE1POL
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Read	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 49. M_WIO_CFG register bit description (default value in bold)

Bit	Symbol	Description
11	GPIO2WUPOL	GPIO2 event detection polarity
		0h High level on GPIO2 will wake up the part
		1h Low level on GPIO2 will wake up the part
		Reset on power-on reset (POR_M)
10	GPIO1WUPOL	GPIO1 event detection polarity
		0h High level on GPIO1 will wake up the part
		1h Low level on GPIO1 will wake up the part
		Reset on power-on reset (POR_M)
9	WAKE2POL	WAKE2 event detection polarity
		0h High level on WAKE2 will wake up the part
		1h Low level on WAKE2 will wake up the part
		Reset on power-on reset (POR_M)
8	WAKE1POL	WAKE1 event detection polarity

Table 49. M_WIO_CFG register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		0h High level on WAKE1 will wake up the part
		1h Low level on WAKE1 will wake up the part
		Reset on power-on reset (POR_M)
5	CSBWUEN	CSB Transition wake-up enabled
		0h Disabled
		1h Enabled
		Reset on power-on reset (POR_M)
4	LDTWUEN	Long Duration Timer wake-up enabled
		0h Disabled
		1h Enabled
		Reset on power-on reset (POR_M)
3	GPIO2WUEN	GPIO2 wake-up enabled
		0h Disabled
		1h Enabled
		Reset on power-on reset (POR_M)
2	GPIO1WUEN	GPIO1 wake-up enabled
		0h Disabled
		1h Enabled
		Reset on power-on reset (POR_M)
1	WK2WUEN	WAKE2 wake-up enabled
		0h Disabled
		h Enabled
		Reset on power-on reset (POR_M)
0	WK1WUEN	WAKE1 wake-up enabled
		0h Disabled
		1h Enabled
		Reset on power-on reset (POR_M)

16.2.18 M_REG_CTRL1

Table 50. M_REG_CTRL1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	GPIO2LP_ON	GPIO1LP_ON	0	0	GPIO2HI	GPIO1HI
Read	RESERVED	RESERVED	GPIO2LP_ON	GPIO1LP_ON	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VREFEN	VBSTEN	0	TRK2EN	TRK1EN	COREEN	LDO2EN	LDO1EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 51. M_REG_CTRL1 register bit description

Bit	Symbol	Value	Description
13	GPIO2LP_ON	Configure GPIO2 state in *standby mode*	
		0h	Follow the power down slot configuration
		1h	Keep GPIO2 in the same state as it was in *normal mode*
		Reset on power-on reset (POR_M),	
12	GPIO1LP_ON	Configure GPIO1 state in *standby mode* and in *LPOFF mode*	
		0h	Follow the power down slot configuration
		1h	Keep GPIO1 in the same state as it was in *normal mode*
		Reset on power-on reset (POR_M),	
9	GPIO2HI	Request GPIO2 pin high	
		0h	No effect (GPIO2 remains in current state)
		1h	GPIO2 set high
		Reset on power-on reset (POR_M), self-cleared	
8	GPIO1HI	Request GPIO1 pin high	
		0h	No effect (GPIO1 remains in current state)
		1h	GPIO1 set high
		Reset on power-on reset (POR_M), self-cleared	
7	VREFEN	VREF enable request	
		0h	No effect (regulator remain in its current state)
		1h	VREF enable request
		Reset on power-on reset (POR_M), self-cleared	
6	VBSTEN	VBST enable request	
		0h	No effect (regulator remain in its current state)
		1h	VBST enable request
		Reset on power-on reset (POR_M), self-cleared	
4	TRK2EN	TRK2 enable request	
		0h	No effect (regulator remain in its current state)
		1h	TRK2 enable request
		Reset on power-on reset (POR_M), self-cleared	
3	TRK1EN	TRK1 enable request	
		0h	No effect (regulator remain in its current state)
		1h	TRK1 enable request
		Reset on power-on reset (POR_M), self-cleared	
2	COREEN	VCORE enable request	
		0h	No effect (regulator remain in its current state)
		1h	VCORE enable request
		Reset on power-on reset (POR_M), self-cleared	
1	LDO2EN	LDO2 enable request	
		0h	No effect (regulator remain in its current state)
		1h	LDO2 enable request
		Reset on power-on reset (POR_M), self-cleared	
0	LDO1EN	LDO1 enable request	
		0h	No effect (regulator remain in its current state)
		1h	LDO1 enable request
		Reset on power-on reset (POR_M), self-cleared	

16.2.19 M_REG_CTRL2

Table 52. M_REG_CTRL2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	GPIO2LO	GPIO1LO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VREFDIS	VBSTDIS	0	TRK2DIS	TRK1DIS	COREDIS	LDO2DIS	LDO1DIS
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 53. M_REG_CTRL2 register bit description

Bit	Symbol	Value	Description
9	GPIO2LO	Request GPIO2 pin low	
		0h	No effect (GPIO2 remains in current state)
		1h	GPIO2 set low
		Reset on power-on reset (POR_M), self-cleared	
8	GPIO1LO	Request GPIO1 pin low	
		0h	No effect (GPIO1 remains in current state)
		1h	GPIO1 set low
		Reset on power-on reset (POR_M), self-cleared	
7	VREFDIS	VREF disable request	
		0h	No effect (regulator remain in its current state)
		1h	VREF disable request
		Reset on power-on reset (POR_M), self-cleared	
6	VBSTDIS	VBST disable request	
		0h	No effect (regulator remain in its current state)
		1h	VBST disable request
		Reset on power-on reset (POR_M), self-cleared	
4	TRK2DIS	TRK2 disable request	
		0h	No effect (regulator remain in its current state)
		1h	TRK2 Disable request
		Reset on power-on reset (POR_M), self-cleared	
3	TRK1DIS	TRK1 disable request	
		0h	No effect (regulator remain in its current state)
		1h	TRK1 disable request
		Reset on power-on reset (POR_M), self-cleared	
2	COREDIS	VCORE disable request	
		0h	No effect (regulator remain in its current state)
		1h	VCORE disable request
		Reset on power-on reset (POR_M), self-cleared	
1	LDO2DIS	LDO2 disable request	
		0h	No effect (regulator remain in its current state)
		1h	LDO2 disable request
		Reset on power-on reset (POR_M), self-cleared	
0	LDO1DIS	LDO1 disable request	

Table 53. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Value	Description
		0h	No effect (regulator remain in its current state)
		1h	LDO1 disable request
		Reset on power-on reset (POR_M), self-cleared	

16.2.20 M_AMUX_CTRL

Table 54. M_AMUX_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Read	RESERVED	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 55. M_AMUX_CTRL register bit description

Bit	Symbol	Value	Description
6	AMUX_EN	Enable AMUX block	
		0h	**Disable AMUX block and pin is pulled down to ground (default)**
		1h	Enable AMUX block
		Reset on power-on reset (POR_M), Go to *LPOFF mode*, Go to *standby mode*	
5	AMUX_DIV	Selection of divider ratio V_{AMUX_RATIO}. See Table 114	
		0h	**Divider ratio is 7.5 (default)**
		1h	Divider ratio is 14
		Reset on power-on reset (POR_M)	

Table 55. M_AMUX_CTRL register bit description*...continued*

Bit	Symbol	Value	Description
4 to 0	AMUX[4:0]	AMUX input channel selection	
		00h	**Disabled with AMUX pin in Hi-Z (default)**
		01h	Low-power bandgap (voltage reference)
		02h	Main bandgap (voltage reference)
		03h	Fail-safe bandgap (voltage reference)
		04h	V_{ANA}: Internal main analog voltage supply
		05h	V_{DIG}: internal main digital voltage supply
		06h	V_{DIG_FS}: internal fail-safe digital voltage supply
		07h	VCORE feedback pin CORE_FB voltage
		08h	VPRE feedback pin VPRE_FB voltage
		09h	LDO1 feedback pin LDO1OUT voltage
		0Ah	LDO2 feedback pin LDO1OUT voltage
		0Bh	VREF feedback pin voltage
		0Ch	TRK1 feedback pin voltage
		0Dh	TRK2 feedback pin voltage
		0Eh	VDDIO feedback voltage
		0Fh	VBOS internal pin voltage
		10h	VBST feedback pin VBST_FB voltage (divider ratio configurable with AMUX_DIV)
		11h	VSUP pin voltage V_{SUP} (divider ratio configurable with AMUX_DIV)
		12h	WAKE1 pin voltage (divider ratio configurable with AMUX_DIV)
		13h	WAKE2 pin voltage (divider ratio configurable with AMUX_DIV)
		14h	GPIO1 pin voltage (divider ratio configurable with AMUX_DIV)
		15h	GPIO2 pin voltage (divider ratio configurable with AMUX_DIV)
		16h	BATSENSE pin voltage (divider ratio configurable with AMUX_DIV)
		17h	Die temperature sensor[1]
		18h	VCORE temperature sensor[1]
		19h	VPRE temperature sensor[1]
		1Ah	LDO1 temperature sensor[1]
		1Bh	LDO2 temperature sensor[1]
		1Ch	TRK1 temperature sensor[1]
		1Dh	TRK2 temperature sensor[1]
		1Eh	GPIO1 temperature sensor[1]
		1Fh	Reserved
		Reset on power-on reset (POR_M)	

[1] Temp (°C) = (V_{AMUX_OUT} – V_{TEMP25}) / V_{TEMP_COEFF} + 25

16.2.21 M_LDT_CFG1

Table 56. M_LDT_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	LDT_AFTER_RUN[15:0]															
Read	LDT_AFTER_RUN[15:0]															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Go to main register map

Table 57. M_LDT_CFG1 register bit description

Bit	Symbol	Description
15 to 0	LDT_AFTER_RUN[15:0]	Long Duration Timer (LDT) after-run configuration register
		LDT after-run **target** value in *normal mode*
		Reset on power-on reset (POR_M), LDT count started

16.2.22 M_LDT_CFG2

Table 58. M_LDT_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_WUP_L[15:8]							
Read	LDT_WUP_L[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_L[7:0]							
Read	LDT_WUP_L[7:0]							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 59. M_LDT_CFG2 register bit description

Bit	Symbol	Description
15 to 0	LDT_WUP_L[15:0]	16 less significant bits of Wake-up with Long Duration Timer
		16 less significant bits for the wake up with the Long Duration Timer
		Reset on power-on reset (POR_M), LDT Count started

16.2.23 M_LDT_CFG3

Table 60. M_LDT_CFG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_H[7:0]							
Read	LDT_WUP_H[7:0]							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 61. M_LDT_CFG3 register bit description

Bit	Symbol	Description
7 to 0	LDT_WUP_H[7:0]	8 more significant bits of Long Duration Timer Wake-up Timer
		8 most significant bit for the wake up with the Long Duration Timer
		Reset on power-on reset (POR_M), LDT Count started

16.2.24 M_LDT_CTRL

Table 62. M_LDT_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	0
Read	RESERVED	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 63. M_LDT_CTRL register bit description

Bit	Symbol	Value	Description
6 to 4	LDT_FNCT[2:0]	Long Duration Timer (LDT) function selection	
		0h	**Function 1 (default)**
		1h	Function 2
		2h	Function 3
		3h	Function 4
		4h	Function 5
		Reset on power-on reset (POR_M)	
3	LDT_SEL	Long Duration Timer (LDT) register (LDT_WUP_H[7:0] / LDT_WUP_L[15:0]) content selection	
		0h	**Read / set LDT wake-up target value (default)**
		1h	Read LDT 24-bit real time counter value
		Reset on power-on reset (POR_M)	
2	LDT_MODE	Set Long Duration Timer (LDT) operation mode	
		0h	**Set LDT to long count (default)**
		1h	Set LDT to short count
		Reset on power-on reset (POR_M)	
1	LDT_EN	Start Long Duration Timer (LDT) operation	
		0h	**Disable LDT (default)**
		1h	LDT starts counting
		Reset on power-on reset (POR_M)	
0	LDT_RUN	LDT status	
		0h	**LDT is disabled or not counting (default)**
		1h	LDT is enabled and count is in progress
		Reset on power-on reset (POR_M), LDT stopped	

16.2.25 M_MEMORY0

Table 64. M_MEMORY0 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM0[15:8]							
Read	MEM0[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM0[7:0]							
Read	MEM0[7:0]							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 65. M_MEMORY0 register bit description

Bit	Symbol	Description
15 to 0	MEM0[15:0]	Free 16 bits for application data storage
		MEM0 stored data
		Reset on power-on reset (POR_M)

16.2.26 M_MEMORY1

Table 66. M_MEMORY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM1[15:8]							
Read	MEM1[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM1[7:0]							
Read	MEM1[7:0]							
Reset	0	0	0	0	0	0	0	0

Go to main register map

Table 67. M_MEMORY1 register bit description

Bit	Symbol	Description
15 to 0	MEM1[15:0]	Free 16 bits for application data storage
		MEM1 stored data
		Reset on power-on reset (POR_M)

17 OTP bits description

17.1 OTP overview

Table 68. Main OTP configuration map

Register Name	ADDRESS (Hex)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_SYS_CFG1	20	RETRY_MSK_OTP[3:0]				RETRY_MODE_OTP	RETRY_DIS_OTP	WK1DFS_DIS_OTP	VSUP_UVTH_OTP
OTP_SYS_CFG2	21	MDFS_DIS_OTP	CLK_FREQ_OTP[1:0]		SLOT_BYP_OTP[2:0]			TSLOT_OTP[1:0]	
OTP_SYS_CFG3	22	GPIO2_VCORE_PGOOD_OTP	GPIO2_MODE_OTP	GPIO1_MODE_OTP	VREF_PLIFT_DIS_OTP	LDO2_PLIFT_DIS_OTP	LDO1_PLIFT_DIS_OTP	BOS_IN_OTP[1:0]	
OTP_VBST_CFG1	23	VBST_MAX_DC_OTP[1:0]		—	VBSTLS_SR_OTP	VBST_PH_OTP[1:0]		VBST_OV_OTP	VBST_CFG_OTP
OTP_VBST_CFG2	24	VBST_TON_MIN_OTP[1:0]		VBST_RCOMP_OTP[1:0]		VBST_CCOMP_OTP[1:0]		VBST_GMCOMP_OTP[1:0]	
OTP_VBST_CFG3	25	VBST_ILIM_OTP[1:0]		VBST_SC_OTP[5:0]					
OTP_VBST_VOLT	26	VBST_SS_OTP[1:0]		—	VBST_OTP[4:0]				
OTP_VPRE_CFG1	27	VPRE_OC_OTP[2:0]			VPRE_SR_OTP	VPRE_PH_OTP[1:0]		VPRE_SS_OTP[1:0]	
OTP_VPRE_CFG2	28	—	VPRE_RCOMP_OTP[2:0]			VPRE_CCOMP_OTP[1:0]		VPRE_GM_OTP[1:0]	
OTP_VPRE_CFG3	29	VPRE_OC_DGLT_OTP[1:0]		VPRE_SC_OTP[5:0]					
OTP_VPRE_CFG4	2A	VPRETSD_PD_OTP	VPRETDFS_OTP	VPRE_CLK_OTP	—	VPRE_PFM_TOFF_OTP[1:0]		VPRE_PFM_TON_OTP[1:0]	
OTP_VPRE_VOLT1	2B	—		VPRE_OTP[5:0]					
OTP_VPRE_VOLT2	2C	VPRE_LP_DVS_OTP[1:0]		VPRE_LP_OTP[5:0]					
OTP_VPRE_VOLT3	2D	VPRE_PDWN_DLY_OTP[1:0]		VPRE_BOS_OTP[5:0]					
OTP_CORE_CFG1	2E	—		COREHS_SR_OTP[1:0]		CORE_PH_OTP[1:0]		CORE_ILIM_OTP[1:0]	
OTP_CORE_CFG2	2F	—		CORE_RCOMP_OTP[1:0]		CORE_CCOMP_OTP[1:0]		CORE_GM_OTP[1:0]	
OTP_CORE_CFG3	30	—		CORE_SS_OTP[1:0]		0	CORE_CTRL_OTP	CORE_LSEL_OTP[1:0]	
OTP_CORE_VOLT1	31	VCORE_OTP[7:0]							
OTP_CORE_CFG5	32	CORETSD_PD_OTP	CORETDFS_OTP	—			CORE_SLOT_OTP[2:0]		
OTP_LDO1_CFG	33	LDO1TSD_PD_OTP	LDO1TDFS_OTP	LDO1_LP_EN_OTP	VLDO1_LP_OTP	VLDO1_OTP	LDO1_SLOT_OTP[2:0]		
OTP_LDO2_CFG	34	LDO2TSD_PD_OTP	LDO2TDFS_OTP	LDO2_LP_EN_OTP	VLDO2_LP_OTP	VLDO2_OTP	LDO2_SLOT_OTP[2:0]		
OTP_TRK1_CFG	35	TRK1TSD_PD_OTP	TRK1TDFS_OTP	TRK1_SEL_OTP[1:0]		—	TRK1_SLOT_OTP[2:0]		
OTP_TRK2_CFG	36	TRK2TSD_PD_OTP	TRK2TDFS_OTP	TRK2_SEL_OTP[1:0]		—	TRK2_SLOT_OTP[2:0]		
OTP_VREF_CFG	37	—		VLDO_REF_OTP[1:0]		VREF_OTP	VREF_SLOT_OTP[2:0]		
OTP_GPIO1_CFG	38	GPIO1TSD_PD_OTP	GPIO1PD_OTP	GPIO1PU_OTP	GPIO1STAGE_OTP[1:0]		GPIO1_SLOT_OTP[2:0]		

Table 68. Main OTP configuration map*...continued*

Register Name	ADDRESS (Hex)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_GPIO2_CFG	39	—	GPIO2 PD_OTP	GPIO2 PU_OTP	GPIO2STAGE_OTP[1:0]		GPIO2_SLOT_OTP[2:0]		
OTP_INPUT_CFG	3A	WK2PD_SEL_OTP	WK1PD_SEL_OTP	GPIO2 TH_OTP	GPIO1TH_OTP	WK2PD_OTP	WK1PD_OTP	WK2 TH_OTP	WK1 TH_OTP
OTP_PROG_IDH	3B	PROG_IDH_OTP[7:0]							
OTP_PROG_IDL	3C	PROG_IDL_OTP[7:0]							

17.2 Main OTP registers bit description

17.2.1 OTP_SYS_CFG1

Table 69. OTP_SYS_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 4	RETRY_MSK_OTP[3:0]	Retry counter time limit	1h	200 ms
			2h	400 ms
			3h	800 ms
			4h	1600 ms
			5h	3200 ms
			6h	6400 ms
			7h	12800 ms
			8h	25600 ms
			9h	51200 ms
			Ah	102400 ms
			Bh	204800 ms
			Ch	409600 ms
			Dh	819200 ms
			Eh	1638400 ms
			Fh	3276800 ms
3	RETRY_MODE_OTP	Auto-retry mode	0h	Limited retry
			1h	Infinite retry
2	RETRY_DIS_OTP	Auto-retry power up from DFS	0h	Enabled
			1h	Disabled
1	WK1DFS_DIS_OTP	Exit DFS on WAKE1 event	0h	Enabled
			1h	Disabled
0	VSUP_UVTH_OTP	VSUP UV threshold V_{SUP_UVL} / V_{SUP_UVH}	0h	4.3 V / 4.8 V
			1h	5.65 V / 6.1 V

Go to main OTP configuration map

17.2.2 OTP_SYS_CFG2

Table 70. OTP_SYS_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	MDFS_DIS_OTP	Disable *Deep Fail Safe* entry	0h	DFS entry enabled

Table 70. OTP_SYS_CFG2 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			1h	DFS entry disabled
6 to 5	CLK_FREQ_OTP[1:0]	Clock frequency selection F_{OSC_HIGH}	0h	16 MHz
			1h	17 MHz
			2h	18 MHz
			3h	19 MHz
4 to 2	SLOT_BYP_OTP[2:0]	Power-up slot bypass	0h	Bypass disabled
			1h	Bypass slot 1 to 6
			2h	Bypass slot 2 to 6
			3h	Bypass slot 3 to 6
			4h	Bypass slot 4 to 6
			5h	Bypass slot 5 to 6
			6h	Bypass slot 6
			7h	Bypass disabled
1 to 0	TSLOT_OTP[1:0]	Power up slot time	0h	250 µs
			1h	500 µs
			2h	1000 µs
			3h	2000 µs

Go to main OTP configuration map

17.2.3 OTP_SYS_CFG3

Table 71. OTP_SYS_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	GPIO2_VCORE_PGOOD_OTP	GPIO2 VCORE_PGOOD	0h	GPIO2 is not driven by VCORE_PGOOD
			1h	GPIO2 is driven by VCORE_PGOOD
6	GPIO2_MODE_OTP	GPIO2 Low Side polarity	0h	GPIO2 LS active high
			1h	GPIO2 LS active low
5	GPIO1_MODE_OTP	GPIO1 Low Side polarity	0h	GPIO1 LS active high
			1h	GPIO1 LS active low
4	VREF_PLIFT_DIS_OTP	VREF pin lift detection	0h	VREF pin lift detection enabled
			1h	VREF pin lift detection disabled
3	LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection	0h	LDO2 pin lift detection enabled
			1h	LDO2 pin lift detection disabled
2	LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection	0h	LDO1 pin lift detection enabled
			1h	LDO1 pin lift detection disabled
1 to 0	BOS_IN_OTP[1:0]	BOS input selection	0h	Auto Transition from VPRE to VSUP when $V_{PRE} < V_{PRE\_UVBOS}$
			1h	Force BOS input to VSUP always

Go to main OTP configuration map

17.2.4 OTP_VBST_CFG1

Table 72. OTP_VBST_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_MAX_DC_OTP[1:0]	VBST maximum duty cycle	0h	72.5 %

Table 72. OTP_VBST_CFG1 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
		DC_{BST_MAX}	1h	77.5 %
			2h	82.5 %
			3h	87.5 %
4	VBSTLS_SR_OTP	VBST low-side slew rate I_{BSTG}	0h	PU = 2 Ω / PD = 1.7 Ω
			1h	PU = 1.5 Ω / PD = 1.0 Ω
3 to 2	VBST_PH_OTP[1:0]	VBST phase delay	0h	No delay
			1h	1 clock cycle
			2h	2 clock cycles
			3h	3 clock cycles
1	VBST_OV_OTP	VBST_FB OV monitor mode	0h	Auto-enable mode
			1h	Overvoltage protection mode
0	VBST_CFG_OTP	VBST configuration	0h	Front-end boost
			1h	Back-end boost

Go to main OTP configuration map

17.2.5 OTP_VBST_CFG2

Table 73. OTP_VBST_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_TON_MIN_OTP[1:0]	VBST minimum on time t_{ON_MIN}	0h	200 ns
5 to 4	VBST_RCOMP_OTP[1:0]	VBST comp resistance	0h	1000 kΩ
			1h	740 kΩ
			2h	500 kΩ
			3h	250 kΩ
3 to 2	VBST_CCOMP_OTP[1:0]	VBST comp capacitor	0h	200 pF
			1h	150 pF
			2h	100 pF
			3h	50 pF
1 to 0	VBST_GMCOMP_OTP[1:0]	VBST comp transconductance	0h	3.9 µS
			1h	5.1 µS
			2h	7.7 µS
			3h	15.3 µS

Go to main OTP configuration map

17.2.6 OTP_VBST_CFG3

Table 74. OTP_VBST_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_ILIM_OTP[1:0]	VBST current limit $V_{BST\_ILIM\_TH}$ / R_{SNS_BST}	0h	60 mV / R_{SNS_BST}
			1h	120 mV / R_{SNS_BST}
			2h	150 mV / R_{SNS_BST}
			3h	180 mV / R_{SNS_BST}
5 to 0	VBST_SC_OTP[5:0]	VBST slope compensation	00h	0 mV/µs
			01h	14 mV/µs
			02h	28 mV/µs

Table 74. OTP_VBST_CFG3 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			03h	42 mV/µs
			04h	56 mV/µs
			05h	70 mV/µs
			06h	84 mV/µs
			07h	99 mV/µs
			08h	113 mV/µs
			09h	127 mV/µs
			0Ah	141 mV/µs
			0Bh	155 mV/µs
			0Ch	169 mV/µs
			0Dh	183 mV/µs
			0Eh	197 mV/µs
			0Fh	211 mV/µs
			10h	225 mV/µs
			11h	239 mV/µs
			12h	253 mV/µs
			13h	268 mV/µs
			14h	282 mV/µs
			15h	296 mV/µs
			16h	310 mV/µs
			17h	324 mV/µs
			18h	338 mV/µs
			19h	352 mV/µs
			1Ah	366 mV/µs
			1Bh	380 mV/µs
			1Ch	394 mV/µs
			1Dh	408 mV/µs
			1Eh	422 mV/µs
			1Fh	436 mV/µs
			20h	451 mV/µs
			21h	465 mV/µs
			22h	479 mV/µs
			23h	493 mV/µs
			24h	507 mV/µs
			25h	521 mV/µs
			26h	535 mV/µs
			27h	549 mV/µs
			28h	563 mV/µs
			29h	577 mV/µs
			2Ah	591 mV/µs
			2Bh	605 mV/µs
			2Ch	620 mV/µs
			2Dh	634 mV/µs
			2Eh	648 mV/µs
			2Fh	662 mV/µs

Table 74. OTP_VBST_CFG3 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			30h	676 mV/µs
			31h	690 mV/µs
			32h	704 mV/µs
			33h	718 mV/µs
			34h	732 mV/µs
			35h	746 mV/µs
			36h	760 mV/µs
			37h	774 mV/µs
			38h	788 mV/µs
			39h	803 mV/µs
			3Ah	817 mV/µs
			3Bh	831 mV/µs
			3Ch	845 mV/µs
			3Dh	859 mV/µs
			3Eh	873 mV/µs
			3Fh	887 mV/µs

Go to main OTP configuration map

17.2.7 OTP_VBST_VOLT

Table 75. OTP_VBST_VOLT register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VBST_SS_OTP[1:0]	VBST soft start t_{BST_SS}	0h	425 µs
			1h	850 µs
			2h	1.7 ms
			3h	3.4 ms
4 to 0	VBST_OTP[4:0]	VBST voltage V_{BST}	00h	5.00 V
			01h	5.25 V
			02h	5.50 V
			03h	5.75 V
			04h	6.00 V
			05h	6.25 V
			06h	6.50 V
			07h	6.75 V
			08h	7.00 V
			09h	7.50 V
			0Ah	8.00 V
			0Bh	8.50 V
			0Ch	9.00 V
			0Dh	9.50 V
			0Eh	10.0 V
			0Fh	10.5 V
			10h	11.0 V
			11h	11.5 V
			12h	12.0 V

Table 75. OTP_VBST_VOLT register bit description...*continued*

Bit	Bit Group Name	Description	Value	Settings
			13h	12.5 V
			14h	13.0 V
			15h	13.5 V
			16h	14.0 V
			17h	14.5 V
			18h	15.0 V
			19h	15.5 V
			1Ah	16.0 V
			1Bh	16.5 V
			1Ch	17.0 V
			1Dh	17.5 V
			1Eh	18.0 V
			1Fh	18.0 V

Go to main OTP configuration map

17.2.8 OTP_VPRE_CFG1

Table 76. OTP_VPRE_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 5	VPRE_OC_OTP[2:0]	VPRE overcurrent flag $I_{PRE\_OC\_FLAG}$	0h	0.66 A
			1h	0.88 A
			2h	1.1 A
			3h	1.32 A
			4h	1.54 A
			5h	1.76 A
			6h	1.98 A
			7h	2.2 A
4	VPRE_SR_OTP	VPRE LX slew rate t_{PRESW_SLR}	0h	2 ns - Fast mode
			1h	4 ns - Slow mode
3 to 2	VPRE_PH_OTP[1:0]	VPRE phase delay	0h	No delay
			1h	1 clock cycle
			2h	2 clock cycles
			3h	3 clock cycles
1 to 0	VPRE_SS_OTP[1:0]	VPRE soft start t_{PRE_SS}	0h	269 µs
			1h	538 µs
			2h	1077 µs
			3h	2150 µs

Go to main OTP configuration map

17.2.9 OTP_VPRE_CFG2

Table 77. OTP_VPRE_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
6 to 4	VPRE_RCOMP_OTP[2:0]	VPRE comp resistance	0h	1300 kΩ
			1h	1137 kΩ

Table 77. OTP_VPRE_CFG2 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			2h	975 kΩ
			3h	812 kΩ
			4h	650 kΩ
			5h	512 kΩ
			6h	325 kΩ
			7h	162 kΩ
3 to 2	VPRE_CCOMP_OTP[1:0]	VPRE comp capacitor	0h	12.0 pF
			1h	23.0 pF
			2h	33.5 pF
			3h	44.5 pF
1 to 0	VPRE_GM_OTP[1:0]	VPRE transconductance amp	0h	10 µS
			1h	15 µS
			2h	20 µS
			3h	25 µS

Go to main OTP configuration map

17.2.10 OTP_VPRE_CFG3

Table 78. OTP_VPRE_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_OC_DGLT_OTP[1:0]	VPRE overcurrent deglitch	0h	250 µs
			1h	500 µs
			2h	1000 µs
			3h	2000 µs
5 to 0	VPRE_SC_OTP[5:0]	VPRE slope compensation	2Ah	279 mV/µs
			2Bh	266 mV/µs
			2Ch	254 mV/µs
			2Dh	241 mV/µs
			2Eh	228 mV/µs
			2Fh	214 mV/µs
			30h	201 mV/µs
			31h	189 mV/µs
			32h	176 mV/µs
			33h	163 mV/µs

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17.2.11 OTP_VPRE_CFG4

Table 79. OTP_VPRE_CFG4 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	VPRETSD_PD_OTP	VPRE TSD pull-down	0h	pull-down enabled in TSD
6	VPRETDFS_OTP	VPRE TSD behavior Default value of VPRETDFS	0h	VPRE disabled only
			1h	Go to DFS
5	VPRE_CLK_OTP	VPRE clock selection F_{PRE}	0h	F_{OSC_HIGH} / 40
			1h	F_{OSC_HIGH} / 8

Table 79. OTP_VPRE_CFG4 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
3 to 2	VPRE_PFM_TOFF_OTP[1:0]	VPRE high-side minimum off time in PFM $t_{PRE\_OFF\_MIN}$	2h	720 ns
1 to 0	VPRE_PFM_TON_OTP[1:0]	VPRE high-side minimum on time in PFM $t_{PRE\_ON\_MIN\_450K}$ / $t_{PRE\_ON\_MIN\_2M2}$	0h	900 ns / 440 ns
			1h	1000 ns / 500 ns
			2h	1125 ns / 550 ns
			3h	1250 ns / 600 ns

Go to main OTP configuration map

17.2.12 OTP_VPRE_VOLT1

Table 80. OTP_VPRE_VOLT1 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 0	VPRE_OTP[5:0]	VPRE output voltage in *normal mode* V_{PRE_PWM}	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V

Table 80. OTP_VPRE_VOLT1 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			2Bh	5.35 V
			2Ch	5.40 V
			2Dh	5.45 V
			2Eh	5.50 V
			2Fh	5.55 V
			30h	5.60 V
			31h	5.65 V
			32h	5.70 V
			33h	5.75 V
			34h	5.80 V
			35h	5.85 V
			36h	5.90 V
			37h	5.95 V
			38h	6.00 V
			39h	6.05 V
			3Ah	6.10 V
			3Bh	6.15 V
			3Ch	6.20 V
			3Dh	6.25 V
			3Eh	6.30 V
			3Fh	6.35 V

Go to main OTP configuration map

17.2.13 OTP_VPRE_VOLT2

Table 81. OTP_VPRE_VOLT2 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_LP_DVS_OTP[1:0]	VPRE DVS ramp rate $V_{PRE\_DVS\_DOWN}$	0h	22 mV/µs
			1h	11 mV/µs
			2h	5.5 mV/µs
			3h	2.75 mV/µs
5 to 0	VPRE_LP_OTP[5:0]	VPRE output voltage in *standby mode* V_{PRE_PFM}	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V

Table 81. OTP_VPRE_VOLT2 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			18h	4.40 V
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V

Go to main OTP configuration map

17.2.14 OTP_VPRE_VOLT3

Table 82. OTP_VPRE_VOLT3 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 6	VPRE_PDWN_DLY_OTP[1:0]	VPRE power down delay	0h	100 µs
			1h	1 ms
			2h	2 ms
			3h	5 ms
5 to 0	VPRE_BOS_OTP[5:0]	VPRE transition voltage	0Ah	3.70 V
			0Bh	3.75 V
			0Ch	3.80 V
			0Dh	3.85 V
			0Eh	3.90 V
			0Fh	3.95 V
			10h	4.00 V
			11h	4.05 V
			12h	4.10 V
			13h	4.15 V
			14h	4.20 V
			15h	4.25 V
			16h	4.30 V
			17h	4.35 V
			18h	4.40 V

Table 82. OTP_VPRE_VOLT3 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			19h	4.45 V
			1Ah	4.50 V
			1Bh	4.55 V
			1Ch	4.60 V
			1Dh	4.65 V
			1Eh	4.70 V
			1Fh	4.75 V
			20h	4.80 V
			21h	4.85 V
			22h	4.90 V
			23h	4.95 V
			24h	5.00 V
			25h	5.05 V
			26h	5.10 V
			27h	5.15 V
			28h	5.20 V
			29h	5.25 V
			2Ah	5.30 V
			2Bh	5.35 V

Go to main OTP configuration map

17.2.15 OTP_CORE_CFG1

Table 83. OTP_CORE_CFG1 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	COREHS_SR_OTP[1:0]	VCORE high-side slew rate t_{CORESW_HSSRR} / t_{CORESW_HSSRF}	0h	Rise = 5 V/ns; Fall = 2.2 V/ns
			1h	Rise = 4 V/ns; Fall = 0.6 V/ns
			2h	Rise = 4.5 V/ns; Fall = 1.2 V/ns
			3h	Rise = 5 V/ns; Fall = 2.2 V/ns
3 to 2	CORE_PH_OTP[1:0]	VCORE phase delay	0h	No delay
			1h	1 clock cycle
			2h	2 clock cycles
			3h	3 clock cycles
1 to 0	CORE_ILIM_OTP[1:0]	VCORE current limit $I_{CORE\_PEAK\_0A8}$ $I_{CORE\_PEAK\_1A65}$	0h	1.4 A
			1h	1.7 A
			2h	2.7 A
			3h	3.4 A

Go to main OTP configuration map

17.2.16 OTP_CORE_CFG2

Table 84. OTP_CORE_CFG2 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	CORE_RCOMP_OTP[1:0]	VCORE comp resistance	0h	150 kΩ
			1h	200 kΩ

Table 84. OTP_CORE_CFG2 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			2h	300 kΩ
			3h	450 kΩ
3 to 2	CORE_CCOMP_OTP[1:0]	VCORE comp capacitor	0h	50 pF
			1h	60 pF
			2h	90 pF
			3h	120 pF
1 to 0	CORE_GM_OTP[1:0]	VCORE transconductance amp	0h	26 µS
			1h	26 µS
			2h	53 µS
			3h	107 µS

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17.2.17 OTP_CORE_CFG3

Table 85. OTP_CORE_CFG3 register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	CORE_SS_OTP[1:0]	VCORE soft start V_{CORE_SS}	0h	2.5 mV/µs
			1h	5 mV/µs
			2h	10 mV/µs
			3h	20 mV/µs
2	CORE_CTRL_OTP	VCORE control type	0h	Valley mode control
			1h	Peak mode control
1 to 0	CORE_LSEL_OTP[1:0]	VCORE inductor L_{CORE}	0h	1 µH
			1h	1.5 µH
			2h	2.2 µH
			3h	2.2 µH

17.2.18 OTP_CORE_VOLT1

Table 86. OTP_CORE_VOLT1 register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	VCORE_OTP[7:0]	VCORE voltage LSB = 10 mV V_{CORE}	00h	0.80 V
			….	….
			FFh	3.35 V

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17.2.19 OTP_CORE_CFG5

Table 87. OTP_CORE_CFG5 register bit description

Bit	Bit Group Name	Description	Value	Settings
7	CORETSD_PD_OTP	VCORE TSD pull-down	0h	Pull-down enabled in TSD
			1h	Pull-down disabled in TSD
6	CORETDFS_OTP	VCORE TSD behavior Default value of CORETDFS	0h	VCORE disabled only
			1h	Go to DFS
2 to 0	CORE_SLOT_OTP[2:0]	VCORE power-up slot	0h	Slot 0

Table 87. OTP_CORE_CFG5 register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

Go to main OTP configuration map

17.2.20 OTP_LDO1_CFG

Table 88. OTP_LDO1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	LDO1TSD_PD_OTP	LDO1 TSD pull-down	0h	pull-down enabled in TSD
			1h	pull-down disabled in TSD
6	LDO1TDFS_OTP	LDO1 TSD behavior Default value of LDO1TDFS	0h	LDO1 disabled only
			1h	Go to DFS
5	LDO1_LP_EN_OTP	LDO1 in *standby mode*	0h	Disabled
			1h	Enabled
4	VLDO1_LP_OTP	LDO1 voltage in *standby mode*	0h	3.3 V
			1h	5.0 V
3	VLDO1_OTP	LDO1 voltage in *normal mode* V_{LDOx}	0h	3.3 V
			1h	5.0 V
2 to 0	LDO1_SLOT_OTP[2:0]	LDO1 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

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17.2.21 OTP_LDO2_CFG

Table 89. OTP_LDO2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	LDO2TSD_PD_OTP	LDO2 TSD pull-down	0h	pull-down enabled in TSD
			1h	pull-down disabled in TSD
6	LDO2TDFS_OTP	LDO2 TSD behavior Default value of LDO2TDFS	0h	LDO2 disabled only
			1h	Go to DFS
5	LDO2_LP_EN_OTP	LDO2 in *standby mode*	0h	Disabled
			1h	Enabled
4	VLDO2_LP_OTP	LDO2 voltage in *standby mode*	0h	3.3 V
			1h	5.0 V

Table 89. OTP_LDO2_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
3	VLDO2_OTP	LDO2 voltage in *normal mode* V_{LDOx}	0h	3.3 V
			1h	5.0 V
2 to 0	LDO2_SLOT_OTP[2:0]	LDO2 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

Go to main OTP configuration map

17.2.22 OTP_TRK1_CFG

Table 90. OTP_TRK1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	TRK1TSD_PD_OTP	TRK1 TSD pull-down	0h	pull-down enabled in TSD
			1h	pull-down disabled in TSD
6	TRK1TDFS_OTP	TRK1 TSD behavior Default value of TRK1TDFS	0h	TRK1 disabled only
			1h	Go to DFS
5 to 4	TRK1_SEL_OTP[1:0]	TRK1 input selection	0h	VREF
			1h	Internal LDO Reference
			2h	LDO2
			3h	VREF
2 to 0	TRK1_SLOT_OTP[2:0]	TRK1 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

Go to main OTP configuration map

17.2.23 OTP_TRK2_CFG

Table 91. OTP_TRK2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	TRK2TSD_PD_OTP	TRK2 TSD pull-down	0h	pull-down enabled in TSD
			1h	pull-down disabled in TSD
6	TRK2TDFS_OTP	TRK2 TSD behavior Default value of TRK2TDFS	0h	TRK2 disabled only
			1h	Go to DFS
5 to 4	TRK2_SEL_OTP[1:0]	TRK2 input selection	0h	VREF
			1h	Internal LDO reference
			2h	LDO2

Table 91. OTP_TRK2_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
			3h	VREF
2 to 0	TRK2_SLOT_OTP[2:0]	TRK2 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

Go to main OTP configuration map

17.2.24 OTP_VREF_CFG

Table 92. OTP_VREF_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
5 to 4	VLDO_REF_OTP[1:0]	Internal LDO reference	0h	1.2 V
			1h	1.8 V
			2h	3.3 V
			3h	5.0 V
3	VREF_OTP	VREF voltage	0h	3.3 V
			1h	5.0 V
2 to 0	VREF_SLOT_OTP[2:0]	VREF power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

Go to main OTP configuration map

17.2.25 OTP_GPIO1_CFG

Table 93. OTP_GPIO1_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	GPIO1TSD_PD_OTP	GPIO1 TSD pull-down R_{PD_GPIOx}	0h	Pull-down enabled in TSD
			1h	Pull-down disabled in TSD
6	GPIO1PD_OTP	GPIO1 pull-down R_{PD_GPIOx}	0h	Pull-down disabled
			1h	Pull-down enabled
5	GPIO1PU_OTP	GPIO1 pull-up R_{PU_GPIOx}	0h	Pull-up disabled
			1h	Pull-up enabled
4 to 3	GPIO1STAGE_OTP[1:0]	GPIO1 configuration	0h	Input configuration
			1h	Low-side driver
			2h	High-side driver
			3h	Push-pull driver

Table 93. OTP_GPIO1_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
2 to 0	GPIO1_SLOT_OTP[2:0]	GPIO1 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

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17.2.26 OTP_GPIO2_CFG

Table 94. OTP_GPIO2_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
6	GPIO2PD_OTP	GPIO2 pull-down R_{PD_GPIOx}	0h	Pull-down disabled
			1h	Pull-down enabled
5	GPIO2PU_OTP	GPIO2 pull-up R_{PU_GPIOx}	0h	Pull-up disabled
			1h	Pull-up enabled
4 to 3	GPIO2STAGE_OTP[1:0]	GPIO2 configuration	0h	Input configuration
			1h	Low-side driver
			2h	High-side driver
			3h	Push-pull driver
2 to 0	GPIO2_SLOT_OTP[2:0]	GPIO2 power-up slot	0h	Slot 0
			1h	Slot 1
			2h	Slot 2
			3h	Slot 3
			4h	Slot 4
			5h	Slot 5
			6h	Slot 6
			7h	Slot 7 / OFF

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17.2.27 OTP_INPUT_CFG

Table 95. OTP_INPUT_CFG register bit description

Bit	Bit Group Name	Description	Value	Settings
7	WK2PD_SEL_OTP	WAKE2 pull-down value selection R_{PD_WAKE}	0h	200 kΩ
			1h	10 kΩ
6	WK1PD_SEL_OTP	WAKE1 pull-down value selection R_{PD_WAKE}	0h	200 kΩ
			1h	10 kΩ
5	GPIO2TH_OTP	GPIO2 detection threshold V_{IL_GPIOx} / V_{IH_GPIOx}	0h	Low-voltage threshold
			1h	High-voltage threshold
4	GPIO1TH_OTP	GPIO1 detection threshold V_{IL_GPIOx} / V_{IH_GPIOx}	0h	Low-voltage threshold
			1h	High-voltage threshold

Table 95. OTP_INPUT_CFG register bit description*...continued*

Bit	Bit Group Name	Description	Value	Settings
3	WK2PD_OTP	WAKE2 pull-down R_{PD_WAKE}	0h	Disabled
			1h	Enabled
2	WK1PD_OTP	WAKE1 pull-down R_{PD_WAKE}	0h	Disabled
			1h	Enabled
1	WK2TH_OTP	WAKE2 detection threshold V_{IL_WAKEx} / V_{IH_WAKEx}	0h	Low-voltage threshold
			1h	High-voltage threshold
0	WK1TH_OTP	WAKE1 detection threshold V_{IL_WAKEx} / V_{IH_WAKEx}	0h	Low-voltage threshold
			1h	High-voltage threshold

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17.2.28 OTP_PROG_IDH

Table 96. OTP_PROG_IDH register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	PROG_IDH_OTP[7:0]	Program ID high decoding	00h	A
			01h	B
			02h	C
			03h	D
			04h	E
			05h	F
			06h	G
			07h	H
			08h	J
			09h	K
			0Ah	L
			0Bh	M
			0Ch	N
			0Dh	P
			0Eh	Q
			0Fh	R
			10h	S
			11h	T
			12h	U
			13h	V
			14h	W
			15h	X
			16h	Y
			17h	Z

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17.2.29 OTP_PROG_IDL

Table 97. OTP_PROG_IDL register bit description

Bit	Bit Group Name	Description	Value	Settings
7 to 0	PROG_IDL_OTP[7:0]	Program ID low decoding	00h	0
			01h	1
			02h	2
			03h	3
			04h	4
			05h	5
			06h	6
			07h	7
			08h	8
			09h	9
			0Ah	A
			0Bh	B
			0Ch	C
			0Dh	D
			0Eh	E
			0Fh	F
			10h	G
			11h	H
			12h	J
			13h	K
			14h	L
			15h	M
			16h	N
			17h	P
			18h	Q
			19h	R
			1Ah	S
			1Bh	T
			1Ch	U
			1Dh	V
			1Eh	W
			1Fh	X
			20h	Y
			21h	Z

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18 Power management

18.1 BOS: best of supply regulator for internal biasing

The BOS regulator manages the Best Of Supply (BOS) from VSUP or VPRE to efficiently generate 5.0 V output and to supply the internal biasing of the device. BOS supplies the high-side and low-side gate drivers of switching regulators.

The V_{BOS_UVL} detection threshold powers down the device.

When the device is starting up, BOS voltage, which is supplied by VSUP until *normal mode* state, needs to rise above the V_{BOS_UVH} threshold to move to *load fuse* state.

The BOS_IN_OTP[1:0] bits define the BOS supply voltage source when the device is in *normal mode* state:

- When the VPRE output voltage setting is above or equal to 5.0 V, it is recommended to BOS_IN_OTP[1:0] = 00 (auto transition). This setting will ensure an optimized power dissipation of the internal biasing.
- When the VPRE output voltage setting is below 5.0 V, it is recommended to have the BOS_IN_OTP[1:0] = 01 (force VBOS_IN = VSUP). This setting is not optimized for BOS power dissipation but will guarantee correct operation of all switching mode power supplies (SMPS).

Table 98. BOS electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BOS_NORM}	V_{BOS} voltage range in *normal mode* (V_{SUP} > 4.5 V and V_{PRE_PWM} > V_{PRE_UVBOS})	V_{PRE_UVBOS} - 0.2	5	5.5	V
V_{BOS_STBY}	V_{BOS} voltage range in *standby mode* (V_{SUP} > 4.5 V, 3.7 V < V_{PRE_PFM} < 35 V)	V_{PRE_PFM} - 0.2	—	V_{PRE_PFM}	V
V_{BOS_LPOFF}	V_{BOS} voltage range in *LPOFF mode* (V_{SUP} > 4.5 V)	2.9	4.5	5.5	V
V_{BOS_UVH}	V_{BOS} undervoltage threshold (rising edge)	3.8	4.0	4.2	V
V_{BOS_UVL}	V_{BOS} undervoltage threshold (falling edge)	3	3.2	3.4	V
V_{BOS_POR}	V_{BOS} power-on reset threshold	2.5	—	3.2	V
V_{DIG_POR}	V_{DIG} power-on reset threshold (POR_M condition)	1.35	—	1.54	V
$V_{DIG\_FS\_POR}$	V_{DIG_FS} power-on reset threshold (POR_FS condition)	1.35	—	1.54	V
External components					
C_{BOS_OUT}	BOS output capacitor at VBOS pin Nominal[1] value Effective[2] value	 4.7 3.3	 4.7 —	 4.7 6.1	µF
C_{DIG_OUT}	VDIG output capacitor Nominal[1] value Effective[2] value	 1 0.75	 1 —	 1 1.25	µF

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

18.2 VPRE: high-voltage buck regulator

The VPRE block is a high-voltage integrated synchronous buck. It operates in forced PWM or PFM modes, and uses internal FETs. The output voltage and the switching frequency (450 kHz or 2.25 MHz) are configurable by OTP. Compensation is ensured by internal circuitry.

VPRE can be used to supply VCORE, LDO1, LDO2, TRK1, TRK2, VREF, and the VBST. VPRE can also supply local loads inside the ECU.

At startup, VPRE soft start can be configured through VPRE_SS_OTP[1:0] bits. In case VPRE is supplied by a pre-regulator (not FS26 VBST), the slowest soft start must be used VPRE_SS_OTP[1:0] = 11.

VPRE operates in PWM (pulse width modulation) when the FS26 is in *normal mode* and in PFM (pulsed frequency modulation) when the FS26 is in *standby mode*. The transition from PWM mode to PFM mode is ensured by a controlled DVS down ramp configurable by OTP ($V_{PRE\_DVS\_DOWN}$).

The current in the inductor is sensed through both high-side and low-side switches. The output DC current is then deducted for internal treatment. When the current in the inductor is rising above the $I_{PRE\_OC\_FLAG}$ threshold, the SPI bit VPREOC_I is set. This overcurrent detection does not affect VPRE regulation.

VPRE has a DC current limitation protection feature I_{LIM_PRE}. When VPRE reaches its current limitation, it induces a duty cycle reduction and therefore an output voltage drop. If the overcurrent disappears before reaching V_{PRE_UVL}, the regulator restarts by doing a soft start toward its nominal output voltage.

To protect the circuitry that is supplied by the VPRE power rail, an additional overvoltage protection is integrated in the main domain. If $V_{PRE\_PWM} > V_{PRE\_OVP}$ for a time longer than t_{PRE_OVP}, the FS26 goes directly into the *Deep Fail Safe* state.

V_{PRE_IN} (V_{SUP_PWR}) must be above $V_{PRE\_PWM} + V_{PRE\_HDR}$ to guarantee VPRE output voltage regulation and its trip level. It can be configured through the VPRE_OC_OTP[2:0] bits.

A thermal shutdown protection is integrated to protect the internal MOSFETs from damage. In case of a TSD event, a pull-down resistor (R_{PRE_DIS}) is enabled to discharge VPRE output capacitors.

The transition from *normal mode* to *LPOFF mode* is ensured by a controlled DVS down ramp ($V_{PRE\_DVS\_DOWN}$) until VPRE is disabled. A power down delay can be configured through VPRE_PDWN_DLY_OTP[1:0] bit to avoid immediate restart. The delay is executed as soon as VPRE DVS down is completed. VPRE regulator is not intended to restart with residual voltage. Therefore, when VPRE is operating at 2.25 MHz, VPRE_PDWN_DLY_OTP[1:0] bit must be configured according to NXP recommendations, as shown in Table 99.

Table 99. VPRE power-down delay configuration when F_{PRE} = 2.25 MHz

ASIL level	VBST configuration	@VPRE_PDWN_DLY_OTP[1:0]
D	Front-end	—
	Back-end / not used	≥ 1 ms
B	Front-end	≥ 2 ms
	Back-end / not used	5 ms

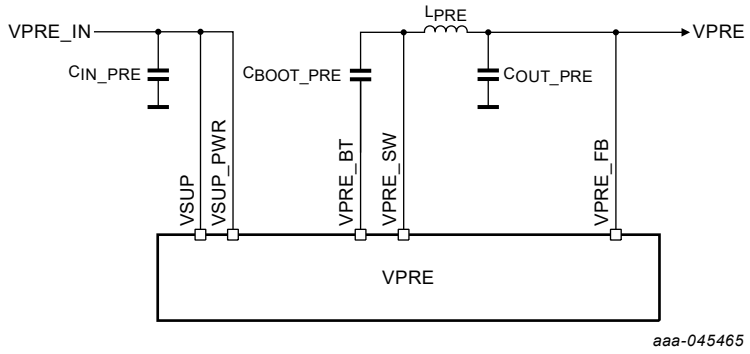

Figure 24. VPRE schematic with connection to V_{SUP}

18.2.1 VPRE electrical characteristics

Table 100. VPRE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static Electrical Characteristics					
V_{PRE_IN}	Input voltage range With I_{PRE_PWM} ≤ 1.5 A and V_{BOS} = 5 V	V_{PRE_PWM} + V_{PRE_HDR}	—	36	V
V_{PRE_HDR}	Input voltage headroom range, 600 mA < I_{PRE_PWM} ≤ 1.5 A	(Max R_{HS_PRE} + Max R_{DCR_LPRE}) x I_{PRE_PWM} x 1.25	—	—	V
	Input voltage headroom range, I_{PRE_PWM} ≤ 600 mA	400	—	—	mV
V_{PRE_PWM}	Output voltage in *normal mode* (VPRE_OTP[5:0] configuration, 50 mV step)	3.7	—	6.35	V
V_{PRE_PFM}	Output voltage in *standby mode* (VPRE_LP_OTP[5:0] configuration, 50 mV step)	3.7	—	5.35	V
$V_{PRE\_ACC\_PWM}$	Output voltage accuracy in PWM mode for I_{PRE_PWM} ≤ 1.5 A	-2	—	2	%
$V_{PRE\_ACC\_PFM\_150m}$ [1]	Output voltage accuracy in PFM mode 10 mA ≤ I_{PRE_PFM} ≤ 100 mA V_{SUP} = V_{SUP_PWR} = 12 V V_{PRE_PFM} = 3.7 V VPRE_PFM_TON_OTP[1:0] = 10 C_{OUT_PRE} ≥ 20 µF (effective value) L_{PRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{PRE} = 10 µH at F_{PRE} = 450 kHz	-4	—	4	%
$V_{PRE\_ACC\_PFM\_10m}$ [1]	Output voltage accuracy in PFM mode I_{PRE_PFM} ≤ 10 mA V_{SUP} = V_{SUP_PWR} = 12 V V_{PRE_PFM} = 5.05 V VPRE_PFM_TON_OTP[1:0] = 10 C_{OUT_PRE} ≥ 20 µF (effective value) L_{PRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{PRE} = 10 µH at F_{PRE} = 450 kHz	-1.5	—	1.5	%
I_{PRE_PWM}	Output current capability in PWM mode	—	—	1.5	A
I_{PRE_PFM}	Current capability in PFM mode (*standby mode* only)	—	—	150	mA
$\eta_{PRE\_PWM\_PEAK}$	Efficiency in PWM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ L_{PRE} = 10 µH with R_{DCR_LPRE} = 60 mΩ F_{PRE} = 450 kHz V_{SUP} = V_{SUP_PWR} = 12 V V_{PRE_PWM} = 5.4 V with I_{PRE_PWM} = 600 mA	—	95	—	%

Table 100. VPRE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$\eta_{PRE\_PWM\_PEAK}$[1]	Efficiency in PFM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{PRE} = 10 µH with R_{DCR_LPRE} = 60 mΩ, F_{PRE} = 450 kHz V_{SUP} = V_{SUP_PWR} = 12 V and 5.4 V V_{PRE_PFM} = 5.05 V with I_{PRE_PFM} = 1 mA VPRE_PFM_TON_OTP[1:0] = 10	—	90	—	%
R_{HS_PRE}	High-side on-resistance (V_{BOS} = 5 V, including bonding)	—	310	500	mΩ
R_{LS_PRE}	Low-side on-resistance (V_{BOS} = 5 V, including bonding)	—	170	300	mΩ
R_{PRE_DIS}	Discharge resistor (when VPRE is disabled – LPOFF)	20	40	60	Ω
TSD_{PRE}	Thermal shutdown threshold	175	—	—	°C
TSD_{PRE_HYST}	Thermal shutdown threshold hysteresis	5	—	12	°C
$I_{PRE\_OC\_FLAG}$[2]	DC overcurrent flag threshold in PWM mode (set VPREOC_I) VPRE_OC_OTP[2:0] = 000 VPRE_OC_OTP[2:0] = 001 VPRE_OC_OTP[2:0] = 010 VPRE_OC_OTP[2:0] = 011 VPRE_OC_OTP[2:0] = 100 VPRE_OC_OTP[2:0] = 101 VPRE_OC_OTP[2:0] = 110 VPRE_OC_OTP[2:0] = 111	 0.45 0.65 0.85 1.12 1.30 1.49 1.68 1.87	 0.66 0.88 1.1 1.32 1.54 1.76 1.98 2.2	 1.0 1.25 1.45 1.70 1.95 2.12 2.38 2.64	A
I_{LIM_PRE}	VPRE output DC current limitation threshold in PWM mode	1.95	2.42	2.9	A
V_{PRE_OVP}	Main overvoltage protection on VPRE output (relative to VPRE output voltage setting)	20	25	30	%
Dynamic electrical characteristics					
t_{PRE_OVP}	Overvoltage deglitch time	1	2	3	µs
t_{PRE_DEAD}	Dead time to avoid cross conduction	1	—	20	ns
t_{PRE_SS}	Soft start ramp from 0 % to 100 % defined at I_{PRE_PWM} = 0 A VPRE_SS_OTP[1:0] = 00 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_SS_OTP[1:0] = 01 VPRE_SS_OTP[1:0] = 10 VPRE_SS_OTP[1:0] = 11	 200 431 873 1753	 269 538 1077 2150	 410 645 1281 2547	µs
$V_{PRE\_DVS\_DOWN}$	DVS down ramp rate during low-power mode transition VPRE_LP_DVS_OTP[1:0] = 00 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_LP_DVS_OTP[1:0] = 01 VPRE_LP_DVS_OTP[1:0] = 10 VPRE_LP_DVS_OTP[1:0] = 11	 18 9 4.5 2.25	 22 11 5.5 2.75	 27 13.5 6.75 3.375	mV/µs
$V_{PRE\_LINE\_REG\_450K\_PWM}$	Transient line in PWM mode with F_{PRE} = 450 kHz V_{BAT} = 6 V - 18 V – 6 V and 14 V - 35 V - 14 V I_{PRE_PWM} = 0 A and 1.5 A for V_{PRE_PWM} = 3.3 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_450K\_DO}$	Transient line after drop out exit with F_{PRE} = 450 kHz V_{BAT} = V_{PRE_PWM} - 0.4 V to 14 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PWM}$	Transient load response in PWM mode with F_{PRE} = 450 kHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH	-3	—	3	%

Table 100. VPRE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{PRE\_LINE\_REG\_2M2\_PWM}$	Transient line in PWM mode with F_{PRE} = 2.25 MHz V_{BAT} = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{PRE_PWM} = 0 A and 1.5 A for V_{PRE_PWM} = 3.3 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_2M2\_DO}$	Transient line after drop out exit F_{PRE} = 2.25 MHz V_{BAT} = V_{PRE_PWM} - 0.4 V to 14 V I_{PRE_PWM} = 0 A and 0.6 A for V_{PRE_PWM} = 5.0 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PWM}$	Transient load response in PWM mode F_{PRE} = 2.25 MHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_HV}$[1]	Transient line in PFM mode with F_{PRE} = 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PWM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_LV}$[1]	Transient line in PFM mode with F_{PRE} = 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_DO}$[1]	Transient line after drop out exit with F_{PRE} = 450 kHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_150m}$[1]	Transient load response in PFM mode with F_{PRE} = 450 kHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 10	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_10m}$[1]	Transient load response in PFM mode with F_{PRE} = 450 kHz VSUP = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05 V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 10	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_2M2\_PFM\_HV}$[1]	Transient line in PFM mode with F_{PRE} = 2.25 MHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_2M2\_PFM\_LV}$[1]	Transient line in PFM mode with F_{PRE} = 2.25 MHz V_{BAT} = 6 V - 12 V – 6 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%

Table 100. VPRE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{PRE\_LINE\_REG\_2M2\_PFM\_DO}$[1]	Transient line after drop out exit with F_{PRE} = 2.25 MHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE_PFM} = 10 µA and 10 mA for V_{PRE_PFM} = 5.05 V dV/dt = 100 mV/µs, L_{PRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PFM\_100m}$[1]	Transient load response in PFM mode with F_{PRE} = 2.25 MHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 10	-3	—	3	%
$V_{PRE\_LOTR\_2M2\_PFM\_10m}$[1]	Transient load response in PFM mode with F_{PRE} = 2.25 MHz V_{SUP} = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05 V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{PRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 10	-1.5	—	1.5	%
F_{PRE}	Operating frequency in PWM mode VPRE_CLK_OTP = 0 VPRE_CLK_OTP = 1	 390 1.90	 450 2.25	 500 2.5	 kHz MHz
t_{PRESW_SLR}	Switching node rising and falling edge setting VPRE_SR_OTP = 0 VPRE_SR_OTP = 1	 — —	 — —	 2 4	 ns
$t_{PRE\_ON\_MIN\_450K}$	HS minimum ON time in PFM mode with F_{PRE} = 450 kHz VPRE_CLK_OTP = 0, V_{PRE_IN} = 12 V VPRE_PFM_TON_OTP[1:0] = 00 VPRE_PFM_TON_OTP[1:0] = 01 VPRE_PFM_TON_OTP[1:0] = 10 VPRE_PFM_TON_OTP[1:0] = 11	 715 800 875 975	 900 1000 1125 1250	 1080 1250 1375 1525	 ns
$t_{PRE\_ON\_MIN\_2M2}$	HS minimum ON time in PFM mode with F_{PRE} = 2.25 MHz VPRE_CLK_OTP = 1, V_{PRE_IN} = 12 V VPRE_PFM_TON_OTP[1:0] = 00 VPRE_PFM_TON_OTP[1:0] = 01 VPRE_PFM_TON_OTP[1:0] = 10 VPRE_PFM_TON_OTP[1:0] = 11	 350 385 420 470	 440 500 550 600	 530 620 690 755	 ns
$t_{PRE\_OFF\_MIN}$	HS minimum OFF time in PFM mode V_{PRE_IN} = 12 V VPRE_PFM_TOFF_OTP[1:0] = 10	 465	 720	 1035	 ns
External components					
L_{PRE}	Inductor value for F_{PRE} = 450 kHz Nominal[3] Effective[4]	 8.2 5.8	 10 —	 10 13	 µH
	Inductor value for F_{PRE} = 2.25 MHz Nominal[3] Effective[4]	 2.2 1.5	 2.2 —	 4.7 6.1	 µH
R_{DCR_LPRE}	Inductor DC resistance	—	60	—	mΩ
C_{IN_PRE}	Effective[4] input capacitor value	10	—	—	µF
C_{BOOT_PRE}	Nominal[3] bootstrap capacitor value	22	—	100	nF
C_{OUT_PRE}	Effective[4] output capacitor value with F_{PRE} = 450 kHz Effective[4] output capacitor value with F_{PRE} = 2.25 MHz	20 20	— —	100 50	µF

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] VPREOC_I flag is correctly reported when V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 18 V.
[3] For all regulators, the nominal value is the value normalized.

[4] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

18.2.2 VPRE efficiency in forced PWM mode

For information, VPRE efficiency versus current load measurement is given based on external components and configuration listed below. If the conditions are different, the new efficiency should be calculated using the FS26 power dissipation tool calculator.

Table 101. VPRE efficiency in forced PWM mode

Ext. C and L		
C_{IN_PRE}	20	µF
$C_{IN\_PRE\_ESR}$	5	mΩ
C_{OUT_PRE}	44	µF
$C_{OUT\_PRE\_ESR}$	2.5	mΩ
L_{VPRE_450kHz}	10	µH
$L_{VPRE\_DCR\_450kHz}$	75	mΩ
$L_{VPRE\_2.25MHz}$	2.2	µH
$L_{VPRE\_DCR\_2.25MHz}$	40	mΩ
$C_{BOOT\_PRE\_MIN}$	22	nF
Int. MOSFETs		
R_{HS_VPRE}	310	mΩ
Q_{HS}	0.8	nC
R_{LS_VPRE}	170	mΩ
Q_{LS}	1	nC
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{PRE_IN}	14	V
VPRE_SR_OTP[1:0]		00

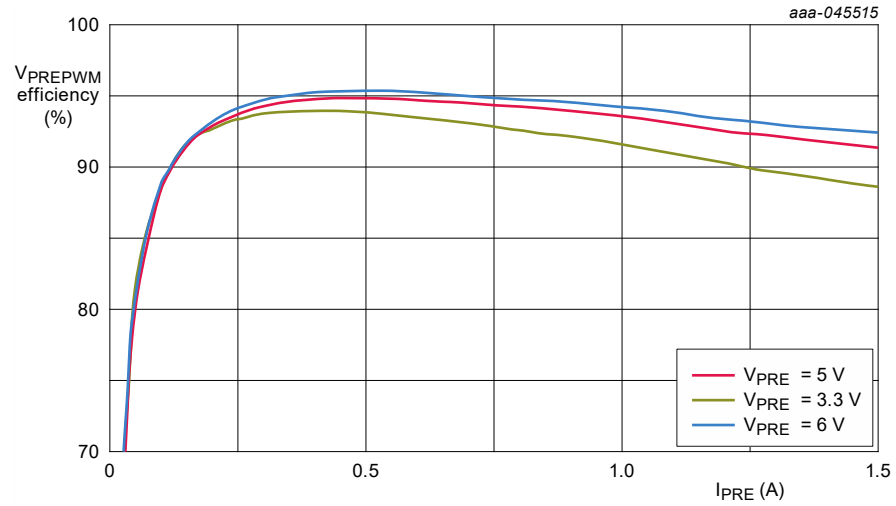

Figure 25. VPRE efficiency at VPRE_CLK_OTP = 0

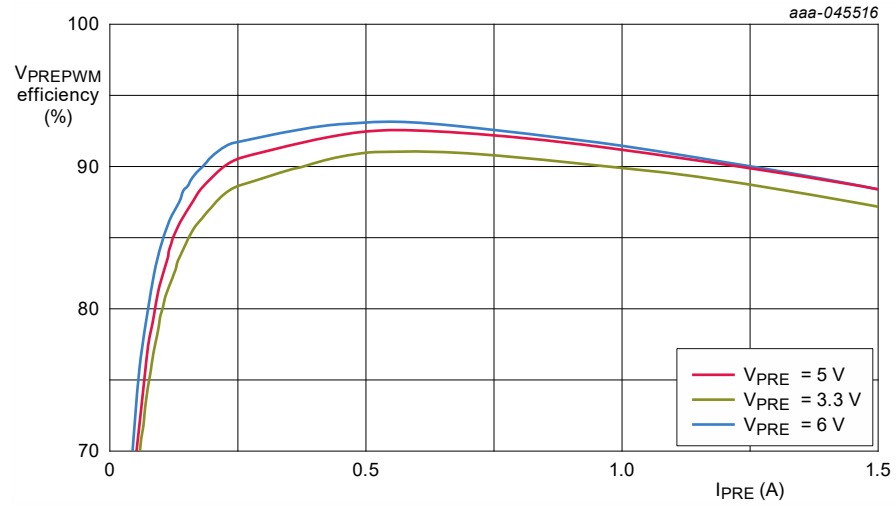

Figure 26. VPRE efficiency at VPRE_CLK_OTP = 1

18.3 VBST: boost controller

The VBST block is an asynchronous, current mode boost controller. VBST works in forced PWM mode. The output voltage is configurable by OTP and the switching frequency is 450 kHz. A peak overcurrent detection is implemented using the voltage sensed across R_{SNS_BST}. The overcurrent detection can be selected with VBST_ILIM_OTP[1:0] bitfield and the value is equal to $V_{BST\_ILIM\_TH}$ divided by R_{SNS_BST}.

When the VBST_FB pin is disconnected, by means of $V_{BST\_FB} < V_{BST\_UV\_TH}$, the boost controller is stopped after t_{BST_UVOV}. VBST will restart automatically when $V_{BST\_FB} > V_{BST\_UV\_TH}$.

A maximum duty cycle protection is implemented in order to protect the boost controller in case of bad component selection.

Two boost topologies (front-end and back-end) are supported:

1. **In front-end mode (VBST_CFG_OTP = 0):**
   When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation with $V_{SUP} > V_{BST}$, the boost controller stops switching and operates in Pass-Through mode. When V_{SUP} drops below the VBST regulation threshold, the boost controller will start switching to regulate the V_{SUP} node to V_{BST}.
   NXP recommends setting the V_{BST} output voltage between 6 V and 10 V maximum, to supply VPRE with enough headroom during cranking pulses. If a higher output voltage is required for the application, the boost should be used in back-end mode.
   In the front-end configuration, VBST_OV_OTP must be set to 0 (Auto-enable). In Auto-enable mode, VBST will stop switching automatically when $V_{BST} > V_{BST\_OV\_TH}$, and will resume switching when V_{BST} drops below V_{BST_OTP}.
   In the front-end configuration, the boost will be enabled only during cranking events. To avoid a latent fault, the VBST_TMD bit can be used to force VBST to regulate at 17 V, no matter what the battery voltage is. This allows verification of VBST availability using the VBST_S status flag.
   An open drain output pin called VBST_PG is available to indicate the boost controller activity. This open drain pin should be connected externally to the VDDIO voltage through a resistor. When VBST_PG is high (open drain OFF) it indicates that the boost controller is switching. When VBST is operating in pulse skipping mode, VBST_PG behavior may not be guaranteed. When VBST_PG is low (open drain ON) it indicates that the boost controller is not switching or disabled.
   The VBST current limitation is sensed at the input and therefore the current capability can be estimated depending on V_{BST_IN}, the VBST voltage configuration and the external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 102 summarizes the maximum current capability during a cranking operation using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.

Table 102. Maximum VBST output current in front-end configuration (DC_{BST_MAX} = 87.5 %, D_{BST} = 0.7 V, LS_{RDSON} = 50 mΩ, L_{BST_DCR} = 60 mΩ)

V_{BST_IN}	V_{BST}	$V_{BST\_ILIM\_TH}$ / R_{SNS_BST}	Maximum I_{BST}
2.7 V	6 V	180 mV / 20 mΩ	1.9 A
		150 mV / 20 mΩ	1.7 A
		120 mV / 20 mΩ	1.4 A
		60 mV / 20 mΩ	0.7 A
	7 V	180 mV / 20 mΩ	1.65 A
		150 mV / 20 mΩ	1.45 A
		120 mV / 20 mΩ	1.2 A
		60 mV / 20 mΩ	0.6 A
	8 V	180 mV / 20 mΩ	1.45 A
		150 mV / 20 mΩ	1.25 A
		120 mV / 20 mΩ	1.05 A
		60 mV / 20 mΩ	0.5 A

2. **In back-end mode or boost not used (VBST_CFG_OTP = 1):**
In the back-end configuration, VBST can be supplied by VPRE or by an external supply. When VBST is supplied by an external supply (VSUP, for example), the maximum duty cycle could limit the output current capability and/or the delta voltage between V_{BST_IN} and V_{BST}.
In the back-end configuration, the output voltage is set by VBST_OTP[4:0] and NXP recommends setting VBST_OV_OTP = 1 (overvoltage protection). In Overvoltage Protection mode, VBST will be disabled if an overvoltage is detected ($V_{BST} > V_{BST\_OV\_TH}$). An SPI command is needed to turn on VBST again.
VBST_PG is indicating a boost overload during soft start or in normal operation. The power good pin (VBST_PG) can be used to avoid an undervoltage cascading effect at the VBST input (VPRE) by opening the VBST current path. This overload protection feature will require the external circuitry described in the application note AN12995.
During a soft start, VBST_PG is at the high level (open drain OFF) to enable the external switch and propagate the output voltage to the load. If an overload condition is detected ($V_{BST} < V_{BST\_UV\_PG}$), while the minimum duty cycle is not reached, the VBST power good pin is asserted low to warn of the overload event. The BOOST controller remains enabled until completion of soft start.
In normal operation, VBST_PG is at the high level (open drain OFF) when the output voltage remains in an acceptable range and at the low level (open drain ON) when the output voltage is 25 % below its nominal voltage ($V_{BST} < V_{BST\_UV\_PG}$).
The VBST current limitation is sensed at the input, and therefore the current capability can be estimated depending on V_{BST_IN}, VBST voltage configuration and the external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 103 summarizes the maximum current capability for an input average current of 500 mA using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.
When the boost controller is not used in the application, VBST_CFG_OTP and VSUP_UVTH_OTP should both be set to 1. The unused pins should be handled as described in Connection of unused pins.

Table 103. Maximum V_{BST} output current in back-end configuration for an input average current of 500 mA (DC_{BST_MAX} = 87.5 %, Efficiency = 85 %)

V_{BST_IN}	V_{BST}	R_{SNS_BST}	Maximum I_{BST}
3.3 V	7 V	60 mΩ	200 mA
	10 V	40 mΩ	140 mA
	12 V	20 mΩ	115 mA
5 V	7 V	80 mΩ	300 mA
	10 V	60 mΩ	210 mA
	12 V	40 mΩ	175 mA
	15 V	20 mΩ	140 mA
6 V	7 V	100 mΩ	360 mA
	10 V	80 mΩ	250 mA
	12 V	60 mΩ	210 mA
	15 V	40 mΩ	170 mA
	18 V	20 mΩ	140 mA

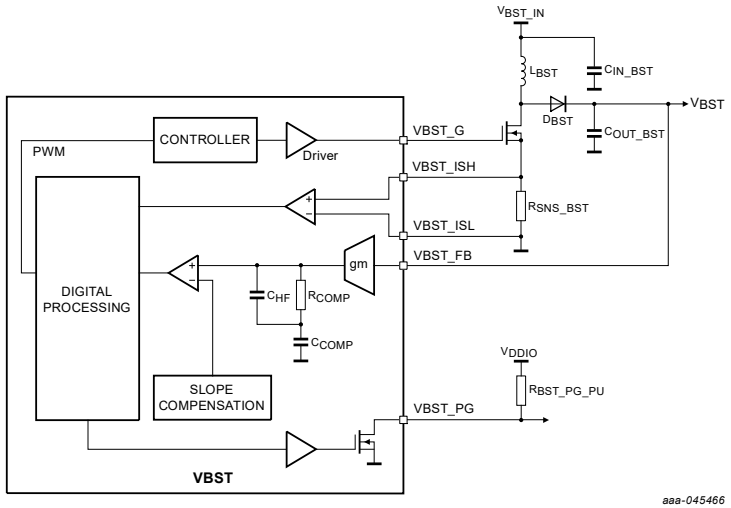

Figure 27. VBST schematic with configuration from VPRE

18.3.1 VBST electrical characteristics

Table 104. VBST electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BST_IN}	Input voltage range	2.7	—	40	V
V_{BST}	Output voltage (OTP configuration, 250 mV step)	5	—	18	V
V_{BST_ACC}	Output voltage accuracy	-3	—	3	%

Table 104. VBST electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
I_{BST}	Nominal output current in front-end VBST_CFG_OTP = 0 (VBST configured as front-end supply) V_{BST} ≤ 10 V and V_{BST_IN} ≥ 2.7 V	—	1	—	A
	Nominal output current in back-end VBST_CFG_OTP = 1 (VBST configured in back-end) V_{BST} ≤ 18 V and V_{BST_IN} ≥ 3.6 V (powered by VPRE)	—	—	0.5	A
$V_{BST\_ILIM\_TH}$	Voltage threshold to detect an inductor peak current limit condition Differential measurement at VBST_ISH pin and VBST_ISL pin VBST_ILIM_OTP[1:0] = 00 VBST_ILIM_OTP[1:0] = 01 VBST_ILIM_OTP[1:0] = 10 VBST_ILIM_OTP[1:0] = 11	 48 96 120 144	 60 120 150 180	 72 144 180 216	mV
$V_{BST\_OV\_TH}$	Overvoltage threshold range (sensed on VBST_FB pin)	105	110	115	%
V_{BSTG}	VBST_G driver output voltage	V_{PRE_UVBOS} - 0.2	V_{BOS}	5.5	V
R_{BSTG}	VBST_G driver pull-down (when VBST is disabled)	6	14.5	23	kΩ
I_{BSTG}	VBST_G current drive at V_{BOS} = 5 V and V_{BSTG} = V_{BOS} / 2 VBSTLS_SR_OTP = 0 VBSTLS_SR_OTP = 1	 0.7 0.9	 — —	 2.0 3.4	A
$V_{BST\_UV\_TH}$	Undervoltage threshold range (sensed on VBST_FB pin)	1.3	1.5	1.7	V
$V_{BST\_UV\_PG}$	VBST undervoltage threshold range to assert VBST_PG pin in back-end mode (sensed on VBST_FB pin)	72.5	75	77.5	%
$R_{BST\_PG\_PU}$	External pull-up resistor to VDDIO pin	5	10	20	kΩ
$V_{BST\_PG\_VOL}$	Low output level threshold (I_{BST_PG} = 2.0 mA)	—	—	0.4	V
$I_{BST\_PG\_LEAK}$	Input leakage current	—	—	1.0	µA
Dynamic electrical characteristics					
F_{BST}	Switching frequency range	380	450	500	kHz
t_{BST_UVOV}	$V_{BST\_UV\_TH}$, $V_{BST\_OV\_TH}$ filtering time	5	10	15	µs
DC_{BST_MAX}	Maximum duty cycle VBST_MAX_DC_OTP[1:0] = 00 VBST_MAX_DC_OTP[1:0] = 01 VBST_MAX_DC_OTP[1:0] = 10 VBST_MAX_DC_OTP[1:0] = 11	 — — — —	 72.5 77.5 82.5 87.5	 — — — —	%
t_{BST_SS}	Soft start from VBST enable to 90 % VBST_SS_OTP[1:0] = 00 VBST_SS_OTP[1:0] = 01 VBST_SS_OTP[1:0] = 10 VBST_SS_OTP[1:0] = 11	 —	 425 850 1700 3400	 600 1200 2400 4800	µs
$t_{BST\_SS\_DAC}$	Digital DAC soft start completion (delay from VBST enable in front-end to VPRE enable) VBST_SS_OTP[1:0] = 00 VBST_SS_OTP[1:0] = 01 VBST_SS_OTP[1:0] = 10 VBST_SS_OTP[1:0] = 11	 —	 1150 2300 4600 9200	 1250 2500 5000 10100	µs
$V_{BST\_LINE\_ON}$	VBST transient line in front end configuration always ON V_{BAT} = 3.2 V - 6.5 V - 3.2 V dV/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF	-5	—	5	%

Table 104. VBST electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{BST\_LINE\_OFF\_ON}$	VBST transient line in front end configuration with OFF/ON transition V_{BAT} = 12.5 V - 6.5 V dV/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF	-5	—	—	%
$V_{BST\_LINE\_ON\_OFF}$	VBST transient line in front end configuration with ON/OFF transition V_{BAT} = 6.5 V - 12.5 V dV/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF	—	—	1.5	V
$V_{BST\_LOTR\_FE}$	Transient load response in Front end mode 200 mA to 1 A step and 1 A to 200 mA step, di/dt = 800 mA/µs $C_{OUT\_BST\_FE}$ = 40 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_FE}$ = 20 µF 2.7 V ≤ V_{BST_IN} ≤ V_{BST} - 1 V, V_{BST} = 7 V	-10	—	10	%
$V_{BST\_LOTR\_BE}$	Transient load response in Back end mode 50 mA to 200 mA step and 200 mA to 50 mA step, di/dt = 150 mA/µs $C_{OUT\_BST\_BE}$ = 22 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_BE}$ = 44 µF V_{BST_IN} = 4.5 V, V_{BST} = 14 V	-5	—	5	%
t_{ON_MIN}	LS minimum ON time VBST_TON_MIN_OTP[1:0] = 00	153	200	235	ns
External components					
L_{BST}	Inductor value Nominal[1] Effective[2]	 4.7 3.3	 4.7 —	 4.7 6.1	µH
L_{BST_DCR}	Inductor DC resistance	—	60	—	mΩ
R_{SNS_BST}	Nominal[1] current sense resistor value (±1 %)	20	—	100	mΩ
D_{BST}	Diode forward voltage drop	—	0.4	—	V
LS_{RDSON}	Low-side MOSFET $R_{DS(on)}$	—	50	—	mΩ
$C_{IN\_BST\_FE}$	Effective[2] input capacitor value for VBST in front-end	10	—	—	µF
$C_{IN\_BST\_BE}$	Effective[2] input capacitor value for VBST in back-end (in addition to C_{OUT_PRE})	10	—	—	µF
$C_{OUT\_BST\_FE}$	Effective[2] output capacitor value for VBST in front-end	20	—	150	µF
$C_{OUT\_BST\_BE}$	Effective[2] output capacitor value for VBST in back-end	20	—	80	µF

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

18.3.2 VBST efficiency

VBST efficiency vs. current load measurement is shown in Table 105 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS26 power dissipation tool calculator.

Table 105. VBST efficiency measurement settings

Ext. Components		
$C_{IN\_BST\_BE}$	22	µF
$C_{IN\_BST\_BE\_ESR}$	2.5	mΩ
$C_{OUT\_BST\_BE}$	44	µF
$C_{OUT\_BST\_BE\_ESR}$	1	mΩ
L_{BST}	4.7	µH
L_{BST_DCR}	60	mΩ
R_{SNS_BST}	20	mΩ
D_{BST}	0.5	V

Table 105. VBST efficiency measurement settings*...continued*

Ext. Components		
Ext. MOSFET		
LS_{RDSON}	30	mΩ
Q_{LS}	7	nC
LS_{BODY_DIODE}	0.7	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{BST_IN}	6	V
F_{BST}	450	kHz
VBSTLS_SR_OTP		1
VBST_ILIM_OTP[1:0]		11
VBST_MAX_DC_OTP[1:0]		11

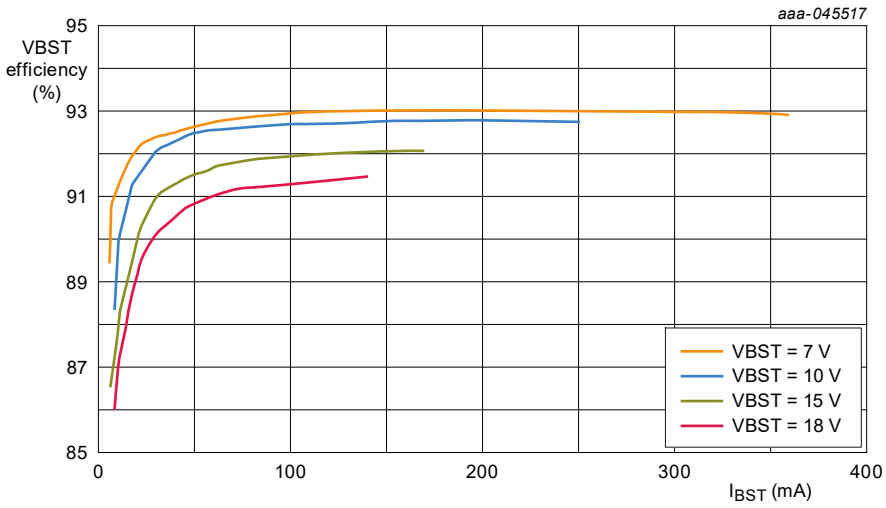

Figure 28. VBST efficiency in back-end mode

18.4 VCORE: low-voltage buck regulator

The VCORE block is a low-voltage integrated synchronous buck operating in forced PWM mode and using internal FETs. The output voltage is configurable by OTP in a range from 0.8 V to 3.35 V, and the switching frequency is 2.25 MHz. Compensation is ensured by internal circuitry.

A dynamic voltage scaling (DVS) feature is configurable by OTP, to control the ramp-up and ramp-down of the regulator. The passive pull-down resistor is enabled during the ramp down.

The current in the inductor is sensed via the internal FETs. A thermal shutdown is implemented to protect the internal FETs. When the current in the inductor rises above the I_{CORE_PEAK} threshold configured with the CORE_ILIM_OTP[1:0] bits, the SPI bit COREOC_I is set. This overcurrent detection does not turn OFF the VCORE but will induce a duty cycle reduction and therefore an output voltage drop.

During the overcurrent condition, the regulator switching frequency may be divided by 2. The regulator will be back to its nominal switching frequency when the overcurrent condition is removed. When the lower CORE_ILIM_OTP[1:0] setting is selected, it is recommended to select L_{CORE} at 1.5 µH or 2.2 µH.

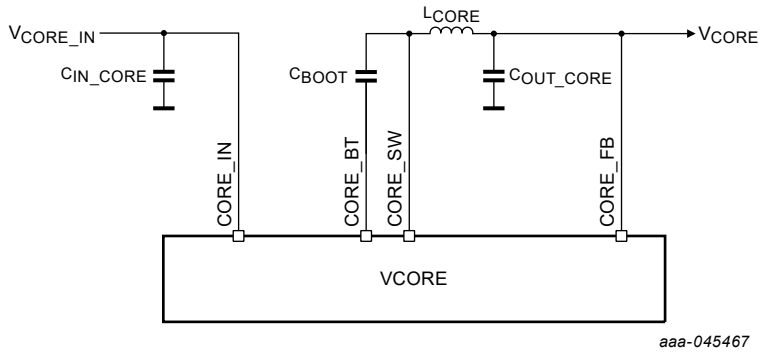

Figure 29. VCORE schematic

18.4.1 VCORE electrical characteristics

Table 106. VCORE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{CORE_IN}	Input voltage range	2.5	—	6.35	V
V_{CORE}	Output voltage (OTP configuration, 10 mV step)	0.8	—	3.35	V
I_{CORE}	Output current capability				
	FS260x and FS261x	—	—	0.8	A
	FS262x and FS263x	—	—	1.65	
V_{CORE_ACC}	Output voltage accuracy				
	I_{OUT} ≤ 1.5 A	-2	—	2	%
	1.5 A < I_{OUT} ≤ 1.65 A	-2.5	—	2.5	
V_{CORE_HDR}	Minimum headroom (V_{CORE_IN} – V_{CORE})				
	I_{CORE} ≤ 800 mA	400	—	—	mV
	I_{CORE} ≤ 1.5 A	800	—	—	
	I_{CORE} ≤ 1.65 A	900	—	—	
$I_{CORE\_PEAK\_0A8}$	Inductor peak current limitation for FS260x and FS261x				
	CORE_ILIM_OTP[1:0] = 00	0.9	1.4	1.9	A

Table 106. VCORE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	CORE_ILIM_OTP[1:0] = 01, 10 or 11	1.15	1.7	2.3	
$I_{CORE\_PEAK\_1A65}$	VCORE inductor peak current limitation for FS262x and FS263x CORE_ILIM_OTP[1:0] = 00 CORE_ILIM_OTP[1:0] = 01 CORE_ILIM_OTP[1:0] = 10 CORE_ILIM_OTP[1:0] = 11	 0.9 1.15 2.0 2.5	 1.4 1.7 2.7 3.4	 1.9 2.2 3.4 4.3	A
η_{CORE_PEAK}	Peak efficiency in PWM mode V_{PRE_PWM} = 5.5 V, V_{CORE} = 1.5 V, I_{CORE} = 800 mA L_{CORE} = 1 µH with DCR = 30 mΩ C_{OUT_CORE} = 20 µF (effective capacitance)	—	87	—	%
R_{HS_CORE}	High-side on-resistance (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{LS_CORE}	Low-side on-resistance (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{CORE_DIS}	Discharge resistor (when V_{CORE} is disabled – LP OFF)	50	100	200	Ω
TSD_{CORE}	Thermal shutdown threshold	175	—	—	°C
TSD_{CORE_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{VCORE_DEAD}	Dead time to avoid cross conduction COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP[1:0] = 00 or 11	 10 5 5	 — — —	 40 30 25	ns
t_{CORESW_HSSRR}[1]	Switching node slew rate (rising) COREHS_SR_OTP[1:0] = 00 COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP[1:0] = 11	 2.5 2 2.25 2.5	 5 4 4.5 5	 — — — —	V/ns
t_{CORESW_HSSRF}[1]	Switching node slew rate (falling) COREHS_SR_OTP[1:0] = 00 COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP[1:0] = 11	 1 0.25 0.5 1	 2.2 0.6 1.2 2.2	 — — — —	V/ns
V_{CORE_SS}	Soft start ramp rate from 10 % to 90 % (DVS up and down) CORE_SS_OTP[1:0] = 00 CORE_SS_OTP[1:0] = 01 CORE_SS_OTP[1:0] = 10 CORE_SS_OTP[1:0] = 11 (C_{OUT_CORE} < 80 µF nominal)	 2 4 8 16	 2.5 5 10 20	 3 6 12 24	mV/µs
V_{CORE_LOTR1}	Transient load response for V_{CORE} ≥ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/µs, C_{OUT_CORE} ≥ 22 µF, L_{CORE} = 1.0 µH	-3	—	3	%
V_{CORE_LOTR2}	Transient load response for VCORE ≤ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/µs, C_{OUT_CORE} ≥ 40 µF, L_{CORE} = 1.0 µH	-30	—	30	mV
F_{CORE}	Operating frequency in PWM mode	2.0	2.25	2.50	MHz
$t_{CORE\_ONOFF\_MIN\_P}$	HS minimum ON and OFF time in peak current mode	10	45	72	ns

Table 106. VCORE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	F_{OSC_HIGH} = 18 MHz (CLK_FREQ_OTP[1:0] = 10)				
$t_{CORE\_ONOFF\_MIN\_V}$	HS minimum ON and OFF time in valley current mode F_{OSC_HIGH} = 18 MHz (CLK_FREQ_OTP[1:0] = 10)	30	55	72	ns
External Components					
L_{CORE}	CORE_LSEL_OTP[1:0] = 00 Nominal[2] inductor value Effective[3] inductor value	 1 0.68	 1 —	 1 1.5	µH
	CORE_LSEL_OTP[1:0] = 01 Nominal[2] inductor value Effective[3] inductor value	 1.5 1	 1.5 —	 1.5 2	µH
	CORE_LSEL_OTP[1:0] = 10 or 11 Nominal[2] inductor value Effective[3] inductor value	 2.2 1.5	 2.2 —	 2.2 2.9	µH
R_{DCR_LCORE}	Inductor DC resistance	—	30	—	mΩ
C_{IN_CORE}	Effective[3] input capacitor value	2.2	—	—	µF
C_{BOOT_CORE}	Bootstrap capacitor Nominal[2] Effective[3]	 47 33	 47 —	 47 62	nF
C_{OUT_CORE}	Effective[3] output capacitor	20	—	100	µF

[1] Covered by characterization only, at I_{CORE} = 1 A, with KITFS26AEEVM.
[2] For all regulators, the nominal value is the value normalized.
[3] For all regulators, the effective value is the value after tolerance, temperature, DC bias and aging removal.

18.4.2 VCORE efficiency

VCORE efficiency vs. current load measurement is shown in Table 107 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS26 power dissipation tool calculator.

Table 107. VCORE efficiency measurement settings

Ext. C and L		
C_{IN_CORE}	10	µF
$C_{IN\_CORE\_ESR}$	2.5	mΩ
C_{OUT_CORE}	44	µF
$C_{OUT\_CORE\_ESR}$	2.5	mΩ
L_{CORE}	1	µH
L_{CORE_DCR}	50	mΩ
C_{BOOT_CORE}	47	nF
Internal MOSFETs		
R_{HS_CORE}	75	mΩ
Q_{HS}	1.2	nC

Table 107. VCORE efficiency measurement settings*...continued*

Ext. C and L		
R_{LS_CORE}	75	mΩ
Q_{LS}	0.7	nC
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{CORE_IN}	6	V
F_{CORE}	2.25	MHz
COREHS_SR_OTP[1:0]		0
CORE_CTRL_OTP		0

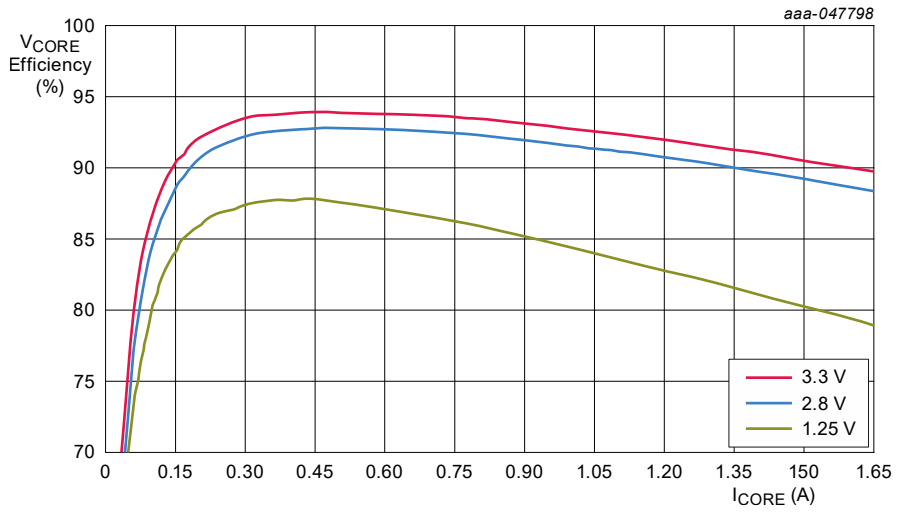

Figure 30. VCORE efficiency

18.5 LDO1 and LDO2: LDO regulators

LDO1 and LDO2 are linear voltage regulators with output voltage between 3.3 V and 5.0 V selectable via OTP, and with up to 400 mA output current capability.

The LDOIN pin is the input voltage supply for both LDO1 and LDO2, and it is intended to be connected to the VPRE output. An overcurrent detection and a thermal shutdown protection are integrated in each LDO.

These regulators are intended to supply microcontroller rails, CAN or FLEXRAY transceivers, as well as other integrated circuits within the ECU.

During *standby mode*, LDOs can be enabled (based on OTP configuration) with minimum additional power consumption.

When the output current rises above the I_{LIM_LDOx} threshold, the corresponding SPI bit LDOxOC_I is set. An overcurrent detection does not turn OFF the corresponding LDO, but will induce an output voltage drop.

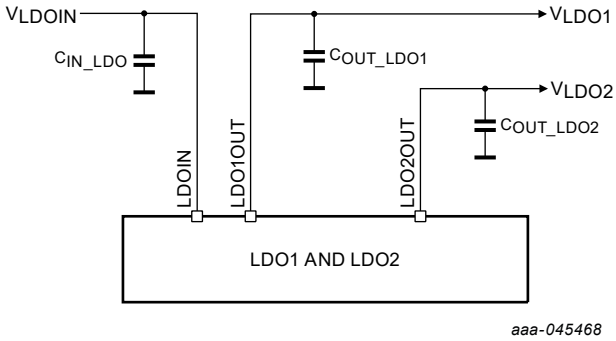

Figure 31. LDOx block diagram

Table 108. LDOx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDOIN}	Input voltage range	V_{LDOx} + $V_{LDOx\_HDR\_NORMAL}$	—	6.35	V
$V_{LDOx\_HDR\_NORMAL}$	Minimum headroom in *normal mode* (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 400 mA	350	—	—	mV
$V_{LDOx\_HDR\_STBY}$[1]	Minimum headroom in *standby mode* (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 10 mA	50	—	—	mV
V_{LDOx}	Output voltage in *normal mode* and in *standby mode* VLDOx_OTP = 0 VLDOx_OTP = 1	 — —	 3.3 5.0	 — —	V
$V_{LDOx\_ACC\_NORMAL}$	Output voltage accuracy in *normal mode* 0 mA ≤ I_{LDOx} ≤ 400 mA , $V_{LDOx\_HDR\_NORMAL}$ = 350 mV	-1.75	—	1.75	%
$V_{LDOx\_ACC\_STBY}$[1]	Output voltage accuracy in *standby mode* 0 mA ≤ I_{LDOx} ≤ 10 mA , $V_{LDOx\_HDR\_STBY}$ = 50 mV	-1	—	1	%
$V_{LDOx\_VREF\_MATCH}$	LDOx versus VREF matching factor in *normal mode* 0 mA ≤ I_{LDOx} ≤ 400 mA , 0 mA ≤ I_{REF} ≤ 30 mA	-1	—	1	%
I_{LDOx}	Nominal current at V_{LDOx} = 5 V V_{LDOx} = 3.3 V and V_{LDOIN} ≤ 5.5 V V_{LDOx} = 3.3 V and V_{LDOIN} > 5.5 V	 — — —	 — — —	 400 400 300	mA
I_{Q_LDOx}[1]	Quiescent current consumption in Low-power modes $V_{LDOx\_HDR\_STBY}$ = 50 mV or 350 mV	—	7	55	µA
I_{LIM_LDOx}	Current limitation threshold reported in LDOxOC_I	450		1750	mA
$PSRR_{LDOx\_450kHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 450 kHz	22	—	—	dB
$PSRR_{LDOx\_2.2MHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 2.25 MHz	32	—	—	dB
R_{LDOxOC_I}	Discharge resistance (when V_{LDOx} is disabled)	—	20	60	Ω
R_{ON_LDOx}	Dropout resistance including bounding			600	mΩ
TSD_{LDOx}	Thermal shutdown threshold	175	—	—	°C
TSD_{LDOx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{LDOx_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{LDOx_SS}	Soft start ramp rate	10	20	30	mV/µs

Table 108. LDOx Electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{LDOx_LOTR}	Transient load response I_{LDOx} = 10 mA to 200 mA step and 200 mA to 10 mA di/dt = 100 mA/µs C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-3	—	3	%
$V_{LDOx\_LOTR\_STBY\_HI}$	Transient load response in *standby mode* I_{LDOx} = 10 mA to 100 mA step and 100 mA to 10 mA di/dt = 100 mA/µs V_{PRE_PFM} = 5.35 V, V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-100	—	100	mV
$V_{LDOx\_LOTR\_STBY\_LO}$[1]	Transient load response in *standby mode* with reduced headroom I_{LDOx} = 10 µA to 10 mA step and 10 µA to 10 mA di/dt = 10 mA/µs V_{PRE_PFM} = 5.05 V , V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF , C_{IN_LDO} = 1 µF	-1.5	—	1.5	%
t_{ON_LDOx}	Turn on rise time (soft start ramp)	—	—	500	µs
External components					
C_{IN_LDO}	Effective[2] input capacitor (close to LDOIN pin)	0.5	—	—	µF
C_{OUT_LDOx}	Effective[2] output capacitance	2.35	4.7	15	µF

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

18.6 VREF: voltage reference

The VREF block is a high accuracy linear voltage regulator with 0.75 % accuracy over the device operating voltage and temperature range. The VREF output voltage is selectable between 3.3 V and 5.0 V via OTP, with 30 mA output current capability.

The TRKIN pin is the input voltage supply for VREF, and it is intended to be connected to the VPRE output. An overcurrent detection is integrated. When the output current rises above the I_{LIM_REF} threshold, the overcurrent detection does not turn OFF the VREF but will induce an output voltage drop.

VREF is intended to supply the microcontroller ADC reference, and to be the reference for the voltage tracking regulators (TRKx) in the FS26 device.

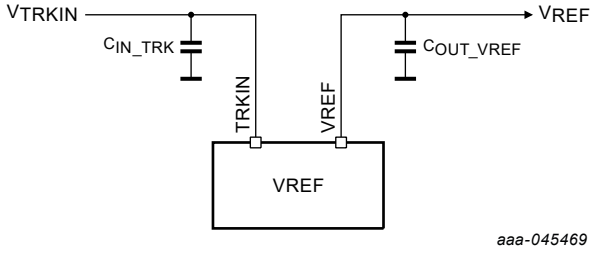

Figure 32. VREF block diagram

Table 109. VREF electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{TRKIN}	Input voltage range	V_{REF} + V_{REF_HDR}	—	6.35	V
V_{REF}	Output voltage VREF_OTP = 0 VREF_OTP = 1	 — —	 3.3 5.0	 — —	V
V_{REF_HDR}	Minimum headroom (V_{TRKIN} – V_{REF})	350	—	—	mV
V_{REF_ACC}	Output voltage accuracy, I_{REF} ≤ 30 mA	-0.75	—	0.75	%
I_{REF}	Nominal current capability	—	—	30	mA
I_{LIM_REF}	Output current limitation	38	—	95	mA
R_{REF_DIS}	Discharge resistor (when V_{REF} is disabled)	80	—	220	Ω
Dynamic electrical characteristics					
V_{REF_SS}	Soft start ramp rate from 10 % to 90 % V_{REF} = 3.3 V V_{REF} = 5.0 V	3.2	—	58	mV/µs
$PSRR_{VREF\_450kHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 450 kHz	25	—	—	dB
$PSRR_{VREF\_2.2MHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 2.25 MHz	35	—	—	dB

Table 109. VREF electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{REF_LOTR}	Transient load response I_{REF} = 100 µA to 10 mA step and 10 mA to 100 µA di/dt = 100 mA/µs	-0.5	—	0.5	%
External components					
C_{OUT_VREF}	V_{REF} effective[1] output capacitance	1.1	2.2	3.3	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

18.7 TRK1 and TRK2: voltage tracking regulators

TRK1 and TRK2 are linear voltage regulators following a known voltage reference. The output voltage of the tracking regulators can track either VREF, LDO2, or an internal LDO reference.

TRK1 and TRK2 are intended to supply sensors located outside the ECU, therefore each voltage tracker is independently protected against short circuit to ground and short circuit to battery. An overcurrent detection and a thermal shutdown protection are integrated in each tracker.

When the output current rises above the I_{LIM_TRKx} threshold, the corresponding SPI bit TRKxOC_I is set. An overcurrent detection does not turn OFF the corresponding tracker but will induce an output voltage drop.

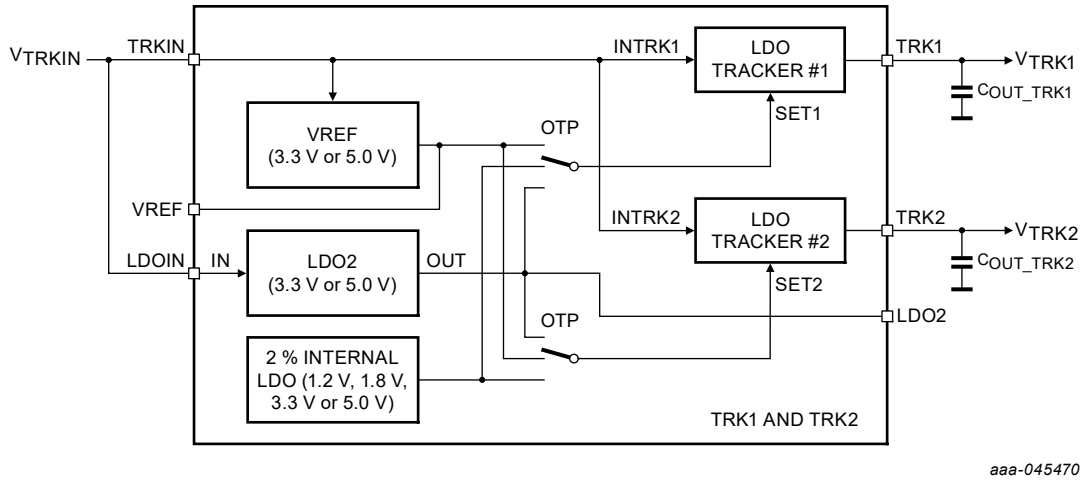

Figure 33. TRK1 and TRK2 block diagram

Table 110. TRKx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical conditions					
V_{TRKIN}	Input reference voltage range	V_{TRKx} + V_{TRKx_HDR}	—	6.35	V
$V_{TRKx\_HDR\_125}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 125 mA	350	—	—	mV
$V_{TRKx\_HDR\_150}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 150 mA	500	—	—	mV
V_{TRKx}	Output voltage				
	V_{SETx} = V_{REF} = 3.3 V	—	3.3	—	V
	V_{SETx} = V_{REF} = 5.0 V	—	5.0	—	
	V_{SETx} = Internal LDO = 1.2 V	—	1.2	—	
	V_{SETx} = Internal LDO = 1.8 V	—	1.8	—	
	V_{SETx} = Internal LDO = 3.3 V	—	3.3	—	
	V_{SETx} = Internal LDO = 5.0 V	—	5.0	—	
	V_{SETx} = V_{LDO2} = 3.3 V	—	3.3	—	
	V_{SETx} = V_{LDO2} = 5.0 V	—	5.0	—	
V_{TRKx_ACC}	Tracker output voltage accuracy when V_{SETx} = Internal LDO	-2	—	2	%
V_{TRKx_OFF}	Offset voltage between tracker output voltage and tracking reference (V_{TRKx} - V_{SETx}) V_{SETx} = V_{REF} or V_{LDO2} 0 mA < I_{TRKx} < 150 mA	-10	—	10	mV

Table 110. TRKx Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
I_{TRKx}	Output current capability V_{TRKx_HDR} = 500 mV, V_{TRKx} = 3.3 V or 5 V V_{TRKx_HDR} = 350 mV, V_{TRKx} = 3.3 V or 5 V V_{TRKx} = 1.2 V or 1.8 V	 — — —	 — — —	 150 125 65	mA
I_{LIM_TRKx}	Output current limitation	160	—	360	mA
I_{TRKx_LEAK}	Reverse current leakage (V_{TRKx} = 40 V). Valid when TRKx is disabled and also in *standby mode* and *LPOFF mode*.	—	—	1.7	mA
$PSRR_{TRKx\_450KHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 450 kHz C_{OUT_TRKx}[1] = 2.2 µF	20	—	—	dB
$PSRR_{TRKx\_2.2MHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 2.2 MHz C_{OUT_TRKx}[1] = 2.2 µF	25	—	—	dB
R_{TRKx_DIS}	Discharge resistance (when TRKx is disabled)	-	100	155	Ω
TSD_{TRKx}	Thermal shutdown threshold	175	—	—	°C
TSD_{TRKx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical conditions					
t_{TRKx_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{TRKx_SLR}	Output voltage ramp rate from 10 % to 90 %	6		15	mV/µs
V_{TRKx_LOTR}	Transient load response I_{TRKx} = 100 µA to 125 mA step and 125 mA to 100 µA di/dt = 125 mA/µs	-3	—	3	%
External components					
C_{IN_TRKx}	Effective[1] input capacitor (close to TRKIN pin)	0.5	—	—	µF
C_{OUT_TRKx}	Effective[1] output capacitance	1.1	2.2	10	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

19 System enhancement functions

19.1 Clock management of the Main domain

The main clock management block is comprised of one high-frequency oscillator, one low-frequency system oscillator, and multiple dividers to generate clocking for the internal main digital state machine, for the low power clock, and for the switching regulators.

The low-frequency oscillator runs at 98 kHz. This oscillator is used for the Long Duration Timer (LDT) and remains ON in Low-power modes to filter the wake-up sources.

The high-frequency oscillator runs at 18 MHz by default. The frequency and the spread spectrum can be configured by SPI to reduce the emission of the oscillator fundamental frequency. The oscillator is used for the SMPS regulators and all the main domain timings. This oscillator is OFF in Low-power modes to reduce the current consumption.

Two frequency dividers provide lower frequency clocks for the switching regulators:

- CLK1 is set at the high-frequency oscillator divided by 8.
- CLK2 is set at the high-frequency oscillator divided by 40.

The frequency of the switching voltage regulators is assigned as shown in Table 111.

Table 111. Switching clock assignment

Regulator	CLK1	CLK2
VBST	No	Yes
VCORE	Yes	No
VPRE	VPRE_CLK_OTP = 1	VPRE_CLK_OTP = 0

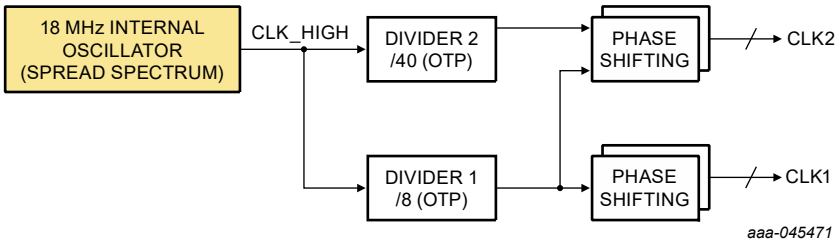

Figure 34. Clock management block diagram

19.1.1 Manual frequency tuning

The internal oscillator frequency runs at 18 MHz by default, and it is configurable via OTP from 16 MHz to 19 MHz with a 1 MHz frequency step. NXP recommends using 18 MHz as a reference value.

Table 112. Manual frequency tuning configuration

CLK_FREQ_OTP[1:0]	High-frequency oscillator	CLK1	CLK2
00	16 MHz	2.000 MHz	400 kHz
01	17 MHz	2.125 MHz	425 kHz
10 (default)	**18 MHz**	**2.250 MHz**	**450 kHz**
11	19 MHz	2.375 MHz	475 kHz

19.1.2 Phase shifting

The clocks of the switching regulators VPRE, VCORE, and VBST can be delayed to keep all the regulators from turning ON at once. This can reduce peak current and improve EMC performance. Each regulator's clock can be shifted from 1 to 3 clock cycles of the high-frequency clock (configurable by OTP).

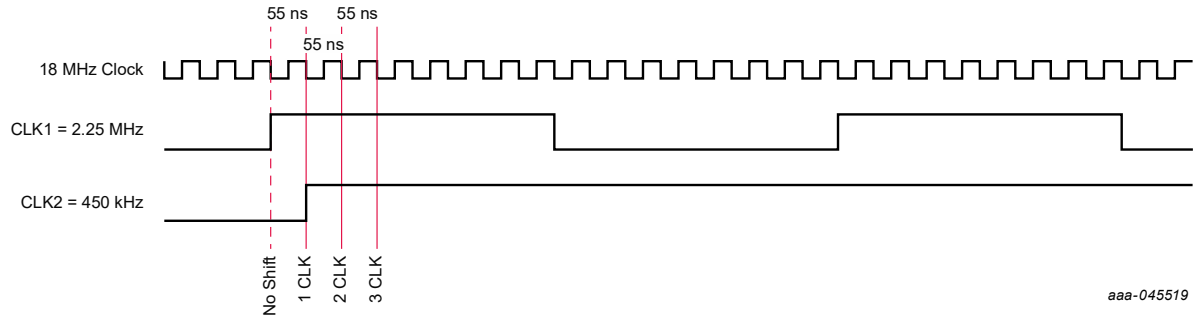

Figure 35. Clock phase shifting examples

19.1.3 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz, with a ±6 % deviation range around the oscillator frequency. The spread spectrum feature and the carrier frequency can be selected by SPI. The FSS_EN bit enables the spread spectrum feature and the FSS_FMOD bit selects high- or low-frequency modulation. These two bits are in the M_SYS_CFG SPI register. By default, the spread spectrum feature is disabled.

The main purpose of the spread spectrum feature is to improve EMC performance by spreading out the energy of the internal oscillator and VPRE frequency. Because of this, NXP recommends enabling spread spectrum and selecting the 23 kHz carrier frequency as the default for both VPRE switching frequencies.

Table 113. Clock management electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Internal oscillator					
F_{OSC_HIGH}	High-frequency oscillator (OTP programmable)				MHz
	CLK_FREQ_OTP[1:0] = 00	—	16	—	
	CLK_FREQ_OTP[1:0] = 01	—	17	—	
	CLK_FREQ_OTP[1:0] = 10	—	**18**	—	
	CLK_FREQ_OTP[1:0] = 11	—	19	—	
$F_{OSC\_HIGH\_ACC}$	High-frequency oscillator accuracy	-6	—	6	%
F_{OSC_LOW}	Low-frequency oscillator	—	98	—	kHz
$F_{OSC\_LOW\_ACC}$	Low-frequency oscillator accuracy	-5	—	5	%
Spread spectrum					
F_{OSC_MOD}	Spread spectrum frequency modulation for 450 kHz				kHz
	CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 0, FSS_EN = 1)	19.5	20.8	22.1	
	CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 0, FSS_EN = 1)	20.8	22.1	23.5	
	CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 0, FSS_EN = 1)	22.1	23.4	24.9	
	CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 0, FSS_EN = 1)	23.3	24.7	26.3	
	Spread spectrum frequency modulation for 2.25 MHz				kHz
	CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 1, FSS_EN = 1)	78.4	83.3	88.4	
	CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 1, FSS_EN = 1)	83.3	88.5	93.9	
	CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 1, FSS_EN = 1)	88.2	93.8	99.4	
	CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 1, FSS_EN = 1)	93.1	99	105	

Table 113. Clock management electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$F_{OSC\_MOD\_RANGE}$	Spread spectrum range (around the nominal frequency)	-6	—	6	%

19.2 Analog multiplexer: AMUX

Various internal and application voltages can be monitored through the AMUX pin. Examples include critical FS26 parameters and system level safety parameters. The channel to be monitored can be selected via the SPI. The maximum AMUX output voltage range is V_{DDIO}.

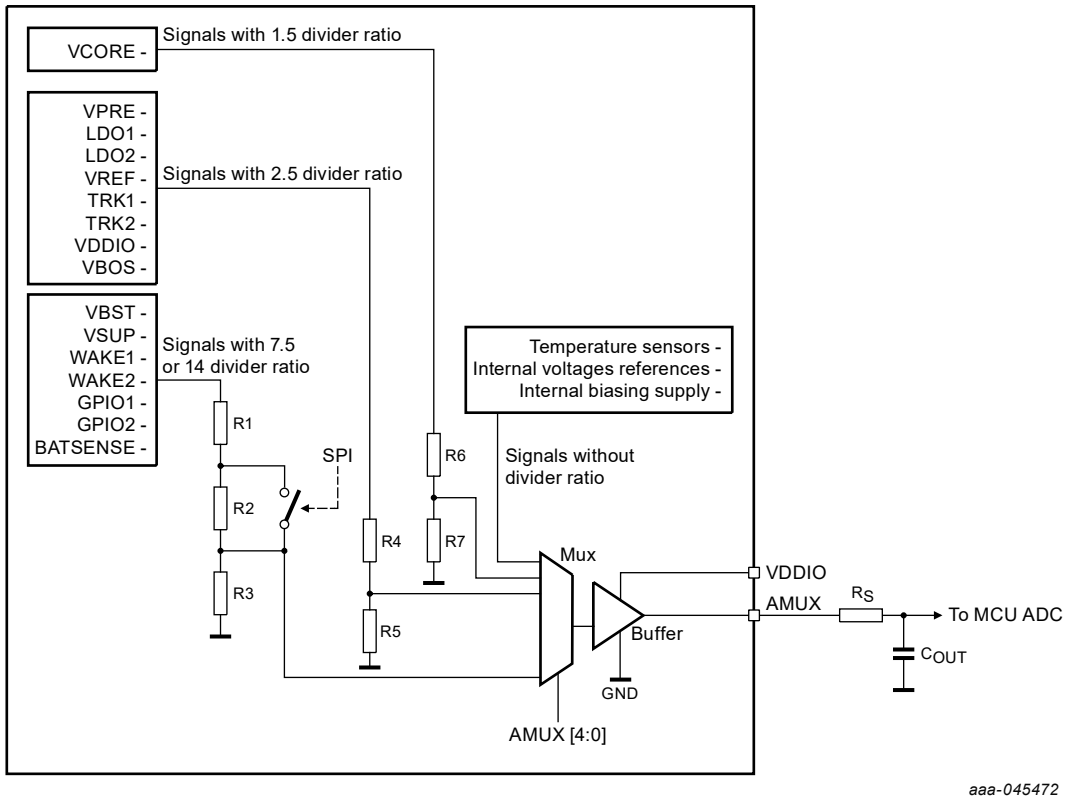

Figure 36. AMUX block diagram

19.2.1 AMUX channel selection

Table 114. AMUX output selection

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
0	xxxxx	Disabled with AMUX pin pulled to ground	N/A	N/A
1	**00000 (default)**	**Disabled with AMUX pin in Hi-Z**	N/A	N/A
1	00001	Low power bandgap for main domain (1.0 V ± 0.5 %)	1	1
1	00010	Bandgap for main domain (1.0 V ± 0.5 %)	1	1
1	00011	Bandgap for fail-safe domain (1.0 V ± 0.5 %)	1	1
1	00100	Analog voltage supply for main domain (1.6 V ± 50 mV)	1	1

Table 114. AMUX output selection*...continued*

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
1	00101	Digital voltage supply for main domain (1.6 V ± 50 mV)	1	1
1	00110	Digital voltage supply for fail-safe domain (1.6 V ± 50 mV)	1	1
1	00111	VCORE voltage	1.5	1.5
1	01000	VPRE voltage	2.5	2.5
1	01001	LDO1 voltage	2.5	2.5
1	01010	LDO2 voltage	2.5	2.5
1	01011	VREF voltage	2.5	2.5
1	01100	TRK1 voltage	2.5	2.5
1	01101	TRK2 voltage	2.5	2.5
1	01110	VDDIO voltage	2.5	2.5
1	01111	VBOS internal voltage	2.5	2.5
1	10000	VBST voltage (divider ratio configurable by SPI)	7.5	14
1	10001	VSUP voltage (divider ratio configurable by SPI)	7.5	14
1	10010	WAKE1 voltage (divider ratio configurable by SPI)	7.5	14
1	10011	WAKE2 voltage (divider ratio configurable by SPI)	7.5	14
1	10100	GPIO1 voltage (divider ratio configurable by SPI)	7.5	14
1	10101	GPIO2 voltage (divider ratio configurable by SPI)	7.5	14
1	10110	BATSENSE pin voltage (divider ratio configurable by SPI)	7.5	14
1	10111	Central die temperature sensor.[1]	1	1
1	11000	VCORE temperature sensor.[1]	1	1
1	11001	VPRE temperature sensor.[1]	1	1
1	11010	LDO1 temperature sensor.[1]	1	1
1	11011	LDO2 temperature sensor.[1]	1	1
1	11100	TRK1 temperature sensor.[1]	1	1
1	11101	TRK2 temperature sensor.[1]	1	1
1	11110	GPIO1 temperature sensor.[1]	1	1
1	11111	Reserved	N/A	N/A

[1] Temp (°C) = (V_{AMUX_OUT} – V_{TEMP25}) / V_{TEMP_COEFF} + 25

Table 115. AMUX Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{AMUX_VDDIO}	VDDIO operating voltage range	3.0	—	5.5	V
V_{AMUX_OUT}	Output voltage range	0.3	—	3.0	V
V_{AMUX_IN}	Input voltage range for VSUP, BATSENSE, VBST, WAKE1, WAKE2, GPIO1, GPIO2 Ratio 7.5 Ratio 14	 2.5 4.2	—	 21 36	V
I_{AMUX}	Output buffer current capability	—	—	1	mA

Table 115. AMUX Electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{AMUX_OFF}	Offset voltage (I_{AMUX} = 1 mA)	-7	—	7	mV
V_{AMUX_RATIO}	Ratio accuracy				%
	Ratio 1	-0.5	—	0.5	
	Ratio 1.5	-1.5	—	1.5	
	Ratio 2.5	-1.5	—	1.5	
	Ratio 7.5	-1.5	—	1.5	
	Ratio 14	-1.5	—	1.5	
R_{AMUX_DIV}	Analog multiplexer total bridge resistance for BATSENSE, VSUP, VBST, WAKE1, WAKE2, GPIO1, GPIO2	0.75	1.5	3	MΩ
R_{AMUX_PD}	Analog multiplexer internal pull-down resistance	5	10	20	kΩ
V_{TEMP25}	Temperature sensor voltage at 25 °C	2.01	2.055	2.1	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-6.25	-5.88	-5.5	mV/°C
T_{AMUX_SET}	Settling time (from 10 % to 90 % of V_{DDIO}, R_S = 220 Ω, C_{OUT} = 10 nF)	—	—	10	µs
External components					
R_S	Nominal output resistor (±10 %)	—	220	—	Ω
C_{OUT}	Nominal[1] output capacitance	2.2	2.2	10	nF
	Effective[2] output capacitance	1.1	—	15	

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

19.3 System I/O pins

19.3.1 WAKE1 and WAKE2: wake-up inputs

WAKE1 pin and WAKE2 pin are programmable inputs used to detect wake-up events on either high or low levels. Both WAKEx pins are protected up to 40 V and are suitable to connect to a wake-up signal outside the ECU.

For each pin, an internal pull-down can be enabled with WKxPD_OTP and its value chosen with WKxPD_SEL_OTP.

Additionally, the VIL / VIH theresholds V_{IL_WAKEx} / V_{IH_WAKEx} can be chosen with WKxTH_OTP and status is reported on WKx_S.

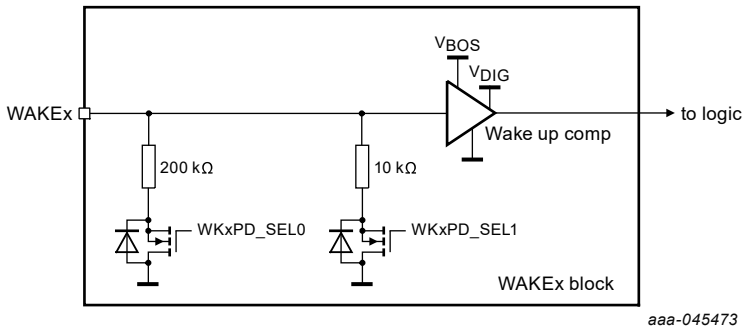

Figure 37. WAKEx pin block diagram

Table 116. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IL_WAKEx}	Low input voltage detection Low voltage detection (WKxTH_OTP = 0) High-voltage detection (WKxTH_OTP = 1)	 — —	 — —	 0.8 0.3 * V_{BOS}	V
V_{IH_WAKEx}	High input voltage detection threshold Low input threshold (WKxTH_OTP = 0) High input threshold (WKxTH_OTP = 1)	 2 0.7 * V_{BOS}	 — —	 — —	V
V_{IN_HYS}	Threshold hysteresis	50	120	500	mV
I_{IN_WAKE}	Input current on WAKEx pins[1]	—	5	10	µA
t_{WAKE}	Wake-up filtering time	50	70	100	µs
R_{PD_WAKE}	Pull-down resistor on WAKE1 and WAKE2 pins WKxPD_SEL_OTP = 0 WKxPD_SEL_OTP = 1	 100 5	 200 10	 320 15	kΩ

[1] No pull-down resistor, wake-up enabled.

19.3.2 GPIO1 and GPIO2: general purpose input/output

GPIO1 pin and GPIO2 pin are general purpose input/output. They can be configured to operate as wake-up inputs, as high-side drivers with up to 20 mA capability, or as low-side drivers with up to 2 mA capability, for use within the ECU. GPIOx configuration can be selected with the GPIOxSTAGE_OTP[1:0] bits.

GPIO1 and GPIO2 low-side drivers can be configured to be either active high or active low with the GPIOx_MODE_OTP bit. Active Low mode can be used to directly drive a PMOS gate without inverting the command.

A thermal shutdown protection is implemented on GPIO1. When a thermal shutdown is triggered, GPIO1 is automatically disabled and will remain disabled until the TSD is present (GPIO1TSD_I = 1). When the TSD is gone (GPIO1TSD_I = 0), a SPI command is mandatory to re-enable GPIO1.

Table 117. GPIO mode configuration

GPIOxSTAGE_OTP[1:0]		GPIOx_MODE_OTP		GPIO Configuration
00	Input configuration	x	—	Output disabled
01	Low-side driver	0	Active High mode	Low-side driver (Active High)
		1	Active Low mode	Low-side driver (Active Low)
10	High-side driver	x	—	High-side driver (Active High)
11	Push-pull	x	—	Push-pull (Active High)

An internal pull-up or pull-down can be enabled by OTP for each GPIO, depending on the GPIOxSTAGE_OTP[1:0] configuration.. The pull-up resistor is always connected to V_{DDIO}.

GPIO1 can be configured to keep its state in *LPOFF mode* or in *standby mode* with GPIO1LP_ON SPI bit. GPIO2 can be configured to keep its state in *standby mode* with the GPIO2LP_ON bit.

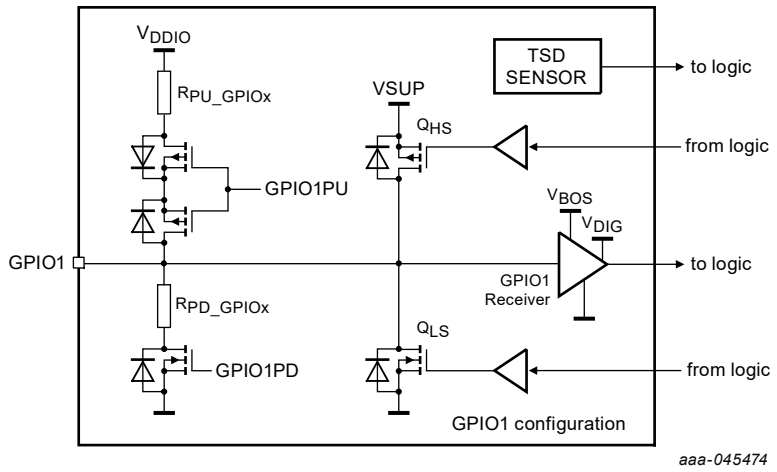

Figure 38. GPIO1 block diagram

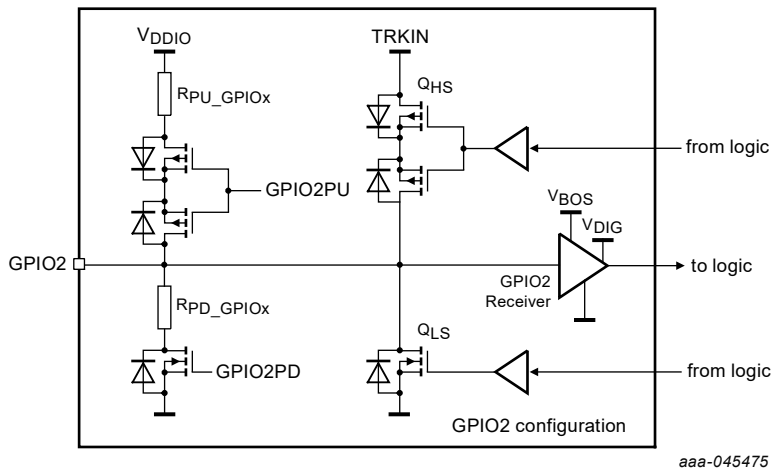

Figure 39. GPIO2 block diagram

19.3.2.1 GPIO input configuration

When GPIOx is set as input configuration, the pin is set to Hi-Z or Low depending on the GPIOxPD_OTP bit. The internal pull-up is disabled regardless of the GPIOxPD_OTP bit.

GPIOx pins are protected up to 40 V, and are suitable to connect a wake-up signal outside the ECU.

When a GPIO is used as a global input pin, an RC protection network is required to protect the input. When a GPIO is used as local input pin, a capacitor is required for immunity. Each GPIO voltage can be sensed through the analog multiplexer.

19.3.2.2 GPIO active high mode

When GPIOx is set as active high, as soon as the OTP is loaded, the pin is set to Hi-Z or Low, depending on the GPIOxPD_OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains Hi-Z or Low until it reaches the selected slot. Once the selected slot is reached, the GPIOx is asserted high.

In *normal mode*, the internal pull-down resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver.

If the internal pull-down is enabled by OTP, the resistor remains enabled in Low-power modes to avoid floating nodes. The internal pull-up resistor should be disabled if the GPIOx is used as a high-side or push-pull driver. Table 118 describes the GPIOx behavior based on the OTP configuration.

Table 118. GPIO Active High mode behavior summary

Configuration	GPIOx PU_OTP	GPIOx PD_OTP	Default state after OTP loaded			*Normal mode*			*Standby mode* GPIOxLP_ON = 0			*LPOFF mode / Deep Fail Safe* GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side driver	0	0	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
	1	1	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
High-side driver	-	0	Hi-Z	OFF	OFF	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	OFF	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF
Push-pull driver	-	0	Low	OFF	ON	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	ON	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF

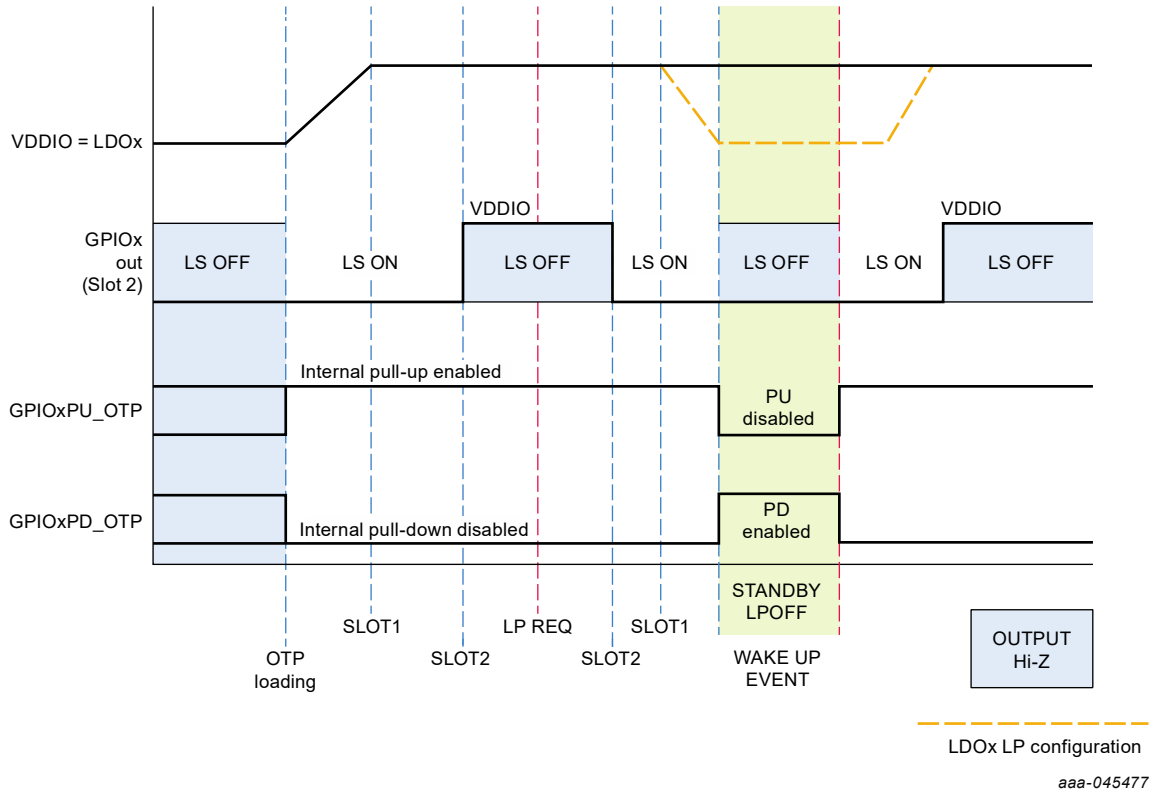

Figure 40. GPIO low-side active high operation. GPIOx_MODE_OTP = 0

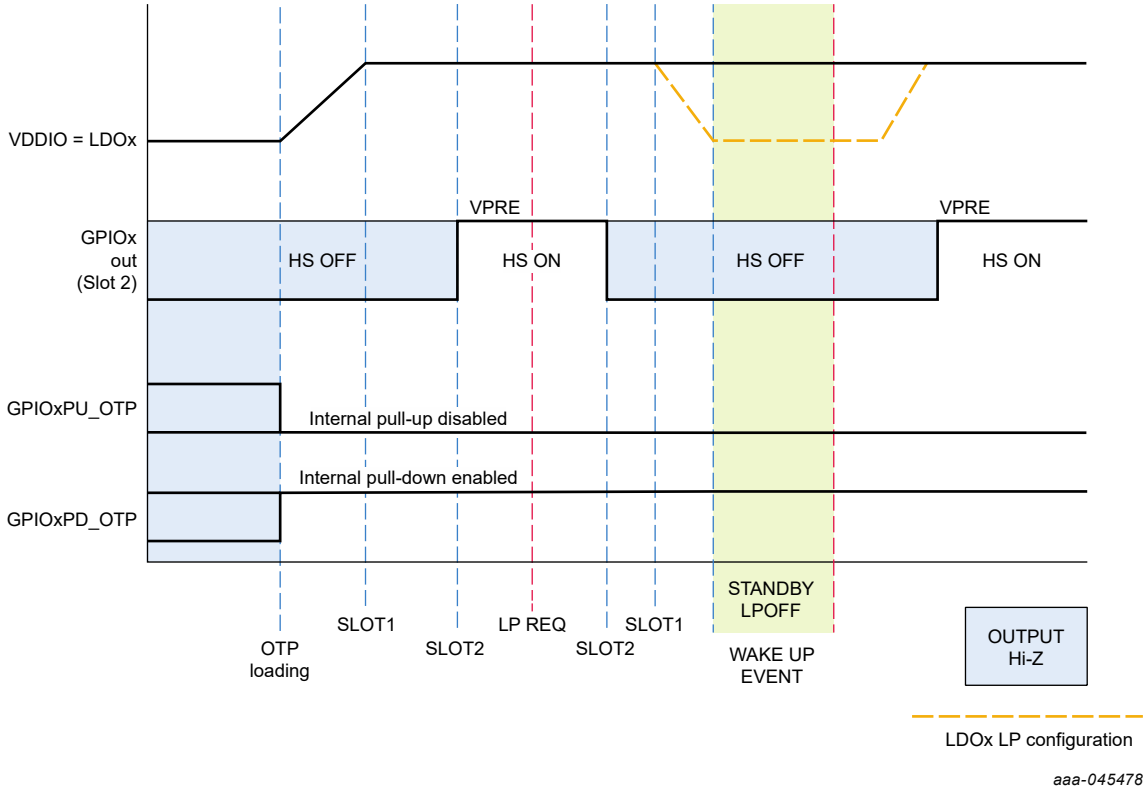

Figure 41. GPIO High-side Active High operation. GPIOx_MODE_OTP = 0

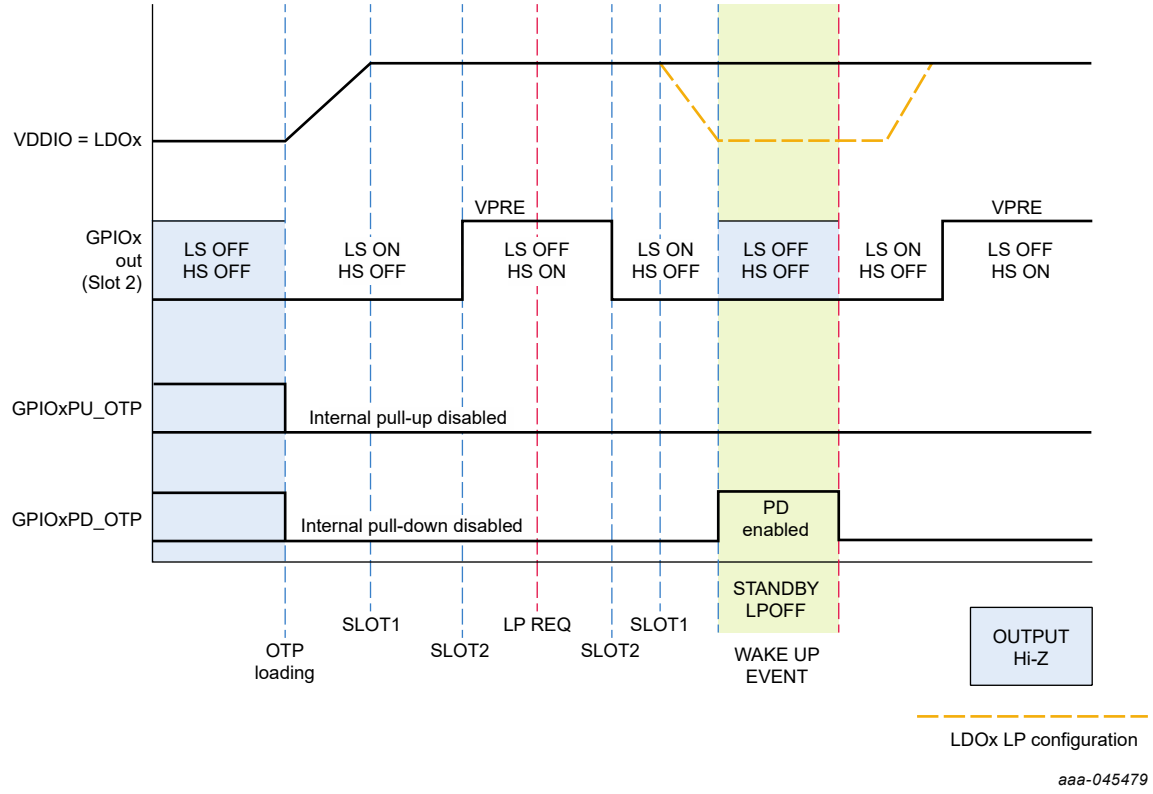

Figure 42. GPIO Push-pull Active High operation. GPIOx_MODE_OTP = 0

19.3.2.3 GPIO active low mode

The active low mode is available only when the GPIOx is configured as a low-side driver.

When GPIOx is set as Active Low, as soon as the OTP is loaded, the pin is set to Hi-Z or High, depending on the GPIOxPU_OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains High or Hi-Z until it reaches the selected slot. Once the selected slot is reached, the GPIOx low-side driver is asserted low.

In *normal mode*, the internal pull-down resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver. If the internal pull-down is enabled by OTP, the resistor remains enabled in Low-power modes, except in *standby mode*, to avoid floating nodes.

Table 119. GPIO Active Low mode behavior summary

Configuration	GPIOx PU_OTP	GPIOx PD_OTP	Default state after OTP loaded			*Normal mode*			*Standby mode* GPIOxLP_ON = 0			*LPOFF mode / Deep Fail Safe* GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side driver	0	0	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF
	1	1	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF

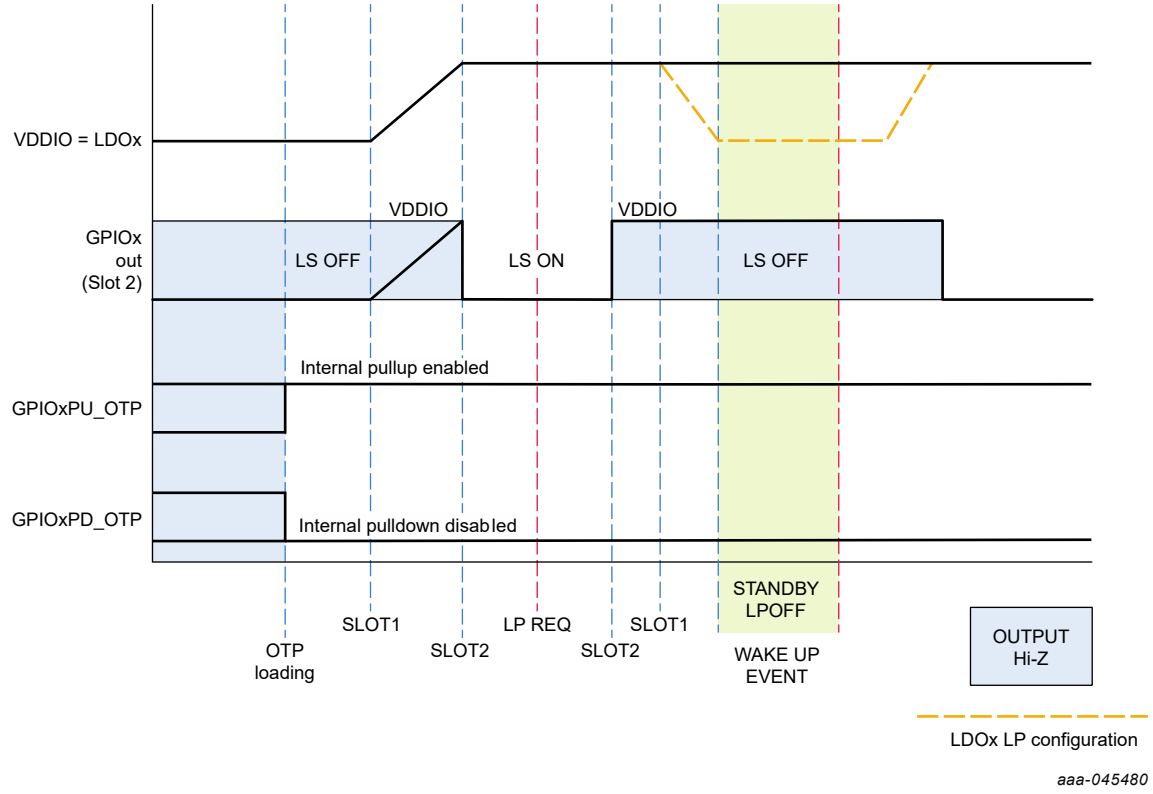

Figure 43. GPIO low-side driver Active Low operation. GPIOx_MODE_OTP = 1

19.3.2.4 VCORE_PGOOD: VCORE power good status

GPIO2 can be used to generate a power good signal from VMON_CORE monitoring to drive an external N-type MOSFET to be able to start with a pre-biased voltage.

NXP recommends using an external load switch between FS26 VCORE and the MCU input supply to prevent reverse current flow from the MCU to the VCORE regulator during *low-power mode*. The VCORE power good feature can be enabled by OTP using the GPIO2_VCORE_PGOOD_OTP bit.

When GPIO2 is used as VCORE_PGOOD, the HS switch (connected internally to VPRE) is used to close the external N-type MOSFET. The power good signal is released as soon as VMON_CORE crosses its undervoltage threshold. VCORE_PGOOD is asserted low when VCORE is disabled, or when an error is reported from VMON_CORE voltage monitoring (undervoltage or overvoltage). Therefore, VCORE_PGOOD will be asserted low when entering Low power mode, setting the CORE_UV flag as soon as the Fail-safe state machine disables VMON_CORE voltage monitoring block, despite VCORE being still up and running.

An external pulldown is mandatory to assert the pin low when the high-side switch is turned off.

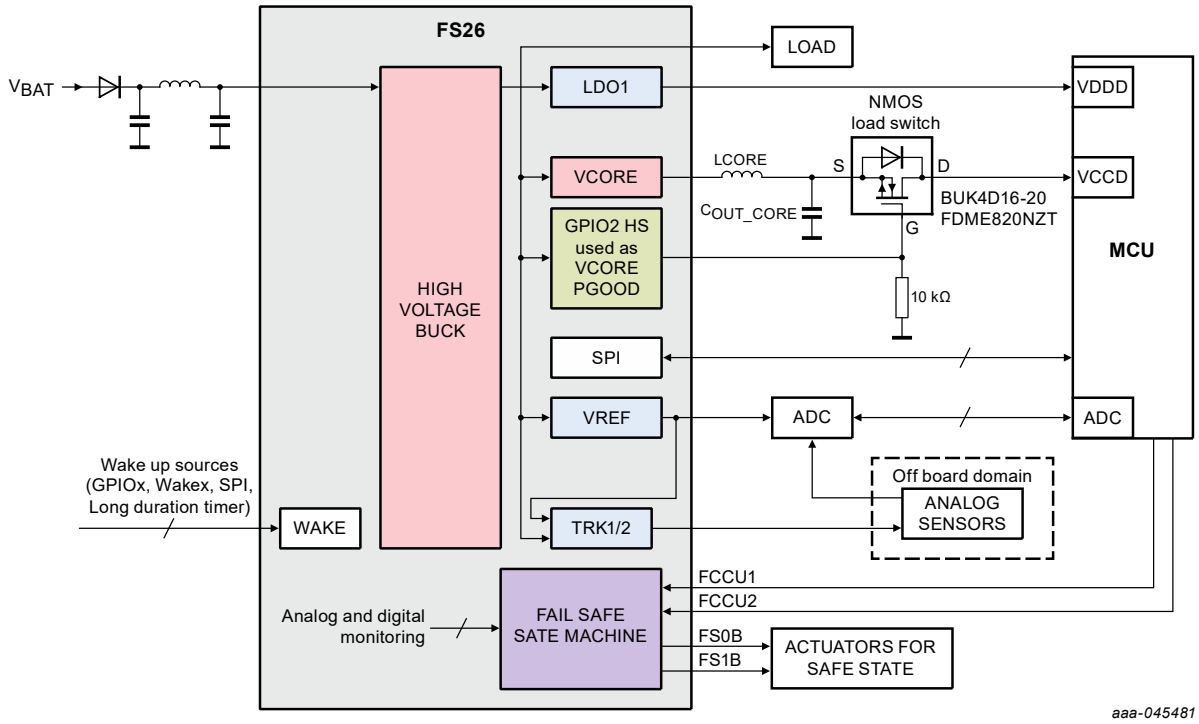

Figure 44. VCORE PGOOD load switch

19.3.2.5 GPIO electrical characteristics

Table 120. GPIO electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IL_GPIOx}	Low input voltage detection Low voltage detection (GPIOxTH_OTP = 0) High-voltage detection (GPIOxTH_OTP = 1)	 — —	 — —	 0.8 0.3 * V_{BOS}	V
V_{IH_GPIOx}	High input voltage detection threshold Low input threshold (GPIOxTH_OTP = 0) High input threshold (GPIOxTH_OTP = 1)	 2 0.7 * V_{BOS}	 — —	 — —	V
V_{IN_HYS}	Threshold hysteresis	50	120	500	mV
t_{WAKE}	Wake-up filtering time	50	70	100	µs
I_{HS_GPIOx}	High-side drive current capability	—	—	20	mA
I_{HS_ILIM}	High-side current limitation threshold	25	50	75	mA
I_{LS_GPIOx}	Low-side drive current capability	—	—	2	mA
I_{LS_ILIM}	Low-side current limitation threshold	3	5	7.5	mA
I_{LEAK_GPIOx}	Input current leakage HS and LS disabled, PU and PD disabled	-10	—	10	µA
R_{PU_GPIOx}	Internal pull-up resistor value	100	200	320	kΩ
R_{PD_GPIOx}	Internal pull-down resistor value	100	200	320	kΩ

Table 120. GPIO electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{DROP_GPIO}	Drop voltage I = 20 mA high-side source I = 2 mA low-side sink	 — —	 0.2 0.2	 0.6 0.4	V
TSD_{GPIO1}	Thermal shutdown threshold for GPIO1	175	—	—	°C
TSD_{GPIO1_HYS}	Thermal shutdown threshold hysteresis for GPIO1	5	—	12	°C

19.3.3 INTB: interrupt output

INTB is an open drain output pin with an internal pull-up to VDDIO. When an internal interrupt occurs, this pin generates a pulse to inform the microcontroller.

Main interrupts, listed in Table 121, generate a pulse on INTB, if the flag is cleared, and fail-safe interrupts, listed in Table 122, generate a pulse on INTB even if the flag is already set. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in the M_xxx_MASK and FS_INTB_MASK registers.

When the RSTB pin is asserted, interrupts are no longer sent to the MCU until the product goes back to the *initialization phase*.

Table 121 and Table 122 list all interrupt sources that can generate a pulse on the INTB pin.

Table 121. List of Interrupt sources from Main logic

SPI flag	Interrupt mask	Interrupt flag	Corresponding event description
TSD_G	TWARN_M	TWARN_I	Central Temp sensor has crossed the thermal warning threshold on the rising edge
	GPIO1TSD_M	GPIO1TSD_I	GPIO1 thermal shutdown event occurred
	VPRETSD_M	VPRETSD_I	VPRE thermal shutdown event occurred
	TRK2TSD_M	TRK2TSD_I	TRK2 thermal shutdown event occurred
	TRK1TSD_M	TRK1TSD_I	TRK1 thermal shutdown event occurred
	CORETSD_M	CORETSD_I	VCORE thermal shutdown event occurred
	LDO2TSD_M	LDO2TSD_I	LDO2 thermal shutdown event occurred
	LDO1TSD_M	LDO1TSD_I	LDO1 thermal shutdown event occurred
REG_G	VBSTOV_M	VBSTOV_I	V_{BST} has crossed $V_{BST\_OV\_TH}$ on the rising edge
	VPREUVH_M	VPREUVH_I	V_{PRE} has crossed V_{PRE_UVH} on the falling edge
	VBSTOC_M	VBSTOC_I	VBST overcurrent event occurred
	VPREOC_M	VPREOC_I	VPRE overcurrent event occurred
	TRK2OC_M	TRK2OC_I	TRK2 overcurrent event occurred
	TRK1OC_M	TRK1OC_I	TRK1 overcurrent event occurred
	COREOC_M	COREOC_I	VCORE overcurrent event occurred
	LDO2OC_M	LDO2OC_I	LDO2 overcurrent event occurred
	LDO1OC_M	LDO1OC_I	LDO1 overcurrent event occurred
VSUP_G	VBOSUVH_M	VBOSUVH_I	V_{BOS} has crossed V_{BOS_UVH} on the falling edge
	VSUPOV_M	VSUPOV_I	V_{SUP} has crossed V_{SUP_OV} on the rising edge
	VSUPUV6_M	VSUPUV6_I	V_{SUP} has crossed V_{SUP_UV6} on the falling edge
	VSUPUVH_M	VSUPUVH_I	V_{SUP} has crossed V_{SUP_UVH} on the falling edge

Table 121. List of Interrupt sources from Main logic*...continued*

SPI flag	Interrupt mask	Interrupt flag	Corresponding event description
WIO_G	LDT_M	LDT_I	LDT event occurred (Function 1 only)
	GPIO2_M	GPIO2_I	GPIO2 event occurred
	GPIO1_M	GPIO1_I	GPIO1 event occurred
	WK2_M	WK2_I	WAKE2 event occurred
	WK1_M	WK1_I	WAKE1 event occurred
	—	WUEVENT[3:0]	Wake-up event occurred
COM_G	MSPI_CRC_M	MSPI_CRC_I	Main SPI CRC calculation is incorrect
	MSPI_CLK_M	MSPI_CLK_I	Main SPI clock provided wrong number of clock pulses
	MSPI_REQ_M	MSPI_REQ_I	MCU writes to an invalid register in the Main domain
—	—	—	Main state machine entered in *normal mode*

Table 122. List of Interrupt sources from the fail-safe domain

SPI flag	Interrupt global flag	Interrupt mask	Interrupt flag	Corresponding event description
FS_G	FS_REG_OVUV_G	VPRE_M	VPRE_OV	An overvoltage event occurred on VMON_PRE monitoring
			VPRE_UV	An undervoltage event occurred on VMON_PRE monitoring
		CORE_M	CORE_OV	An overvoltage event occurred on VMON_CORE monitoring
			CORE_UV	An undervoltage event occurred on VMON_CORE monitoring
		LDO1_M	LDO1_OV	An overvoltage event occurred on VMON_LDO1 monitoring
			LDO1_UV	An undervoltage event occurred on VMON_LDO1 monitoring
		LDO2_M	LDO2_OV	An overvoltage event occurred on VMON_LDO2 monitoring
			LDO2_UV	An undervoltage event occurred on VMON_LDO2 monitoring
		TRK1_M	TRK1_OV	An overvoltage event occurred on VMON_TRK1 monitoring
			TRK1_UV	An undervoltage event occurred on VMON_TRK1 monitoring
		TRK2_M	TRK2_OV	An overvoltage event occurred on VMON_TRK2 monitoring
			TRK2_UV	An undervoltage event occurred on VMON_TRK2 monitoring
		REF_M	REF_OV	An overvoltage event occurred on VMON_REF monitoring
			REF_UV	An undervoltage event occurred on VMON_REF monitoring
		EXT_M	EXT_OV	An overvoltage event occurred on VMON_EXT monitoring
			EXT_UV	An undervoltage event occurred on VMON_EXT monitoring
	—	FCCU1_M / FCCU2_M	FCCU12	An event occurred on FCCU1 monitoring
		FCCU1_M	FCCU1 bit	An event occurred on FCCU1 monitoring
		FCCU2_M	FCCU2 bit	An event occurred on FCCU2 monitoring
		ERRMON_M	ERRMON bit	An event occurred on external IC monitoring
FS_G / COM_G	FS_WD_G	BAD_WD_M	BAD_WD_DATA	A bad watchdog data refresh occurred
			BAD_WD_TIMING	A bad watchdog timing refresh occurred
—	—	—	—	Fail-safe state machine entered in *initialization phase*

Table 123. INTB Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
R_{INTB_PU}	Internal pull-up resistor to V_{DDIO}	5	10	20	kΩ
V_{INTB_VOL}	Low output level threshold I_{INTB} = 2.0 mA	—	—	0.4	V
I_{NTB_LEAK}	Input leakage current V_{DDIO} = 5.5 V	—	—	1.0	µA
I_{INTB_ILIM}	INTB current limitation	4	—	20	mA
t_{INTB_PULSE}	Interrupt pulse duration Short pulse (INT_PWIDTH = 0) Long pulse (INT_PWIDTH = 1)	 17.5 70	 25 100	 32.5 130	µs

19.4 LDT: long duration timer

The FS26 features a long duration timer (LDT) with an integrated oscillator. The timer is configurable by the SPI and can operate in *normal mode* and in Low-power modes. It provides several functions and offers a wide range of configurable counting periods, as well as a calibration mechanism for internal oscillator compensation (function1).

The timer is not part of the safety circuitry and is not covered by LBIST (logic built-in self-test). It can be activated in *normal mode*, though, and all prescaler options can be selected to allow timer circuitry verification. The timer is based on a 24 bit counter, with a 32768 Hz oscillator, allowing a 1.0 second time base.

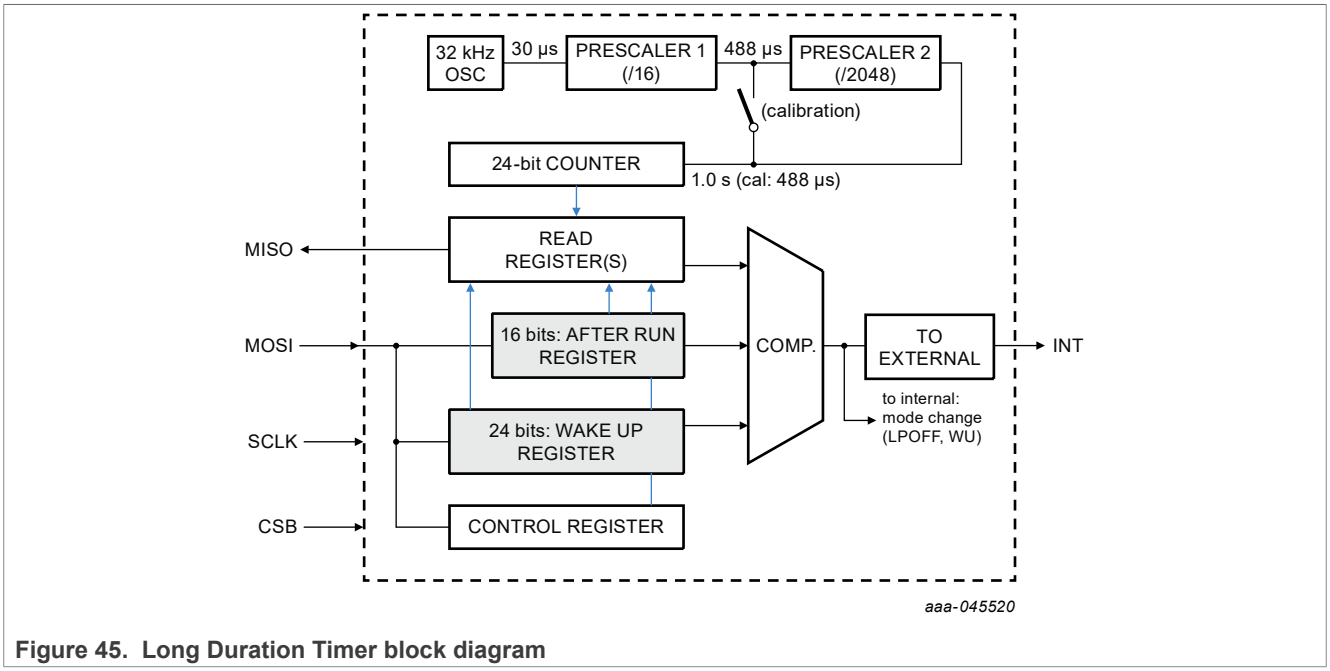

Figure 45. Long Duration Timer block diagram

19.4.1 LDT characteristics

In normal operation, the timer can count up to 194 days, with a 1 second resolution. In short count mode, the prescaler 2 is bypassed and the timer can count up to 2.28 hours, with a 488 µs resolution.

Table 124. long duration timer characteristics

	Oscillator frequency	Oscillator period	Prescaler	Counter resolution	Max count	
Long count	32.768 kHz	30.52 µs	16 x 2048	1 s	4660 hours	194 days
Short count	32.768 kHz	30.52 µs	16	488 µs	8192 s	2.28 hours

The LDT has two modes of operation, based on the prescaler used during the count:

- When LDT_MODE = 0, the LDT is set in Long Count mode.
- When LDT_MODE = 1, the LDT is set in Short Count mode, suitable for calibration.

The LDT_AFTER_RUN[15:0] bits is used to set or to read the after run target value in *normal mode*.

The LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits is used to set or to read the wake-up target value, in combination with the LDT_SEL bit:

- LDT_WUP_H[7:0] contains the 8 most significant bits of the wake-up target value.
- LDT_WUP_L[15:0] contains the 16 least significant bits of the wake-up target value.

The LDT_SEL bit allows the MCU to either set/read the wake-up target value or to read the current value of the 24 bit LDT counter in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.

- When LDT_SEL = 0, the MCU can read or write the wake-up target value in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.
- When LDT_SEL = 1, the MCU can read the counter current value (running or not).

The LDT_EN bit is provided to start the LDT timer operation:

- When LDT_EN = 0, the LDT is disabled.
- When LDT_EN = 1, the LDT starts counting as defined in the M_LDT_CTRL and M_LDT_CFGx registers.

The LDT_LPSEL[7:0] bits indicate the appropriate Low-power mode. The LDT_LPSEL[7:0] bits reset to 0 every time the device enters the *normal mode*. When timer function 2 or 3 is selected, the MCU must first write the safe key value on the LDT_LPSEL[7:0] bits to confirm that the device will go into the corresponding Low-power mode after the run timer has expired.

- When LDT_LPSEL[7:0] = AAh, the device goes into *standby mode* after the run timer expires.
- When LDT_LPSEL[7:0] = A5h, the device goes into *LPOFF mode* after the run timer expires.
- When timer function 4 or 5 is selected and LDT_EN = 1, the LDT does not start any count until the device enters the corresponding Low-power mode.

19.4.2 Calibration procedure

The calibration procedure consists of activating the counter for a specific duration and comparing the result with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back its final value to compare with its own accurate time of activation and to calculate a time offset.

NXP recommends performing the calibration between -20 °C and 85 °C. Calibration example:

- Select the timer function 1 and set the after run value to 65535 (~32 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 20 s (must be less than 30 s with ±5.0 % oscillator accuracy).
- If the oscillator period is at exact typical value (absolutely no deviation error), expected reading is 40960.
- The exact reading calculates the error correction factor ECF = exact_reading/expected_reading.
- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.
- After calibration, the new after run or wake-up values to set the counter are "after run x ECF" and "wake-up x ECF".

19.4.3 LDT functions

Table 125. Long Duration Timer functions

LDT_FNCT[2:0]	Long Duration Timer Function
0h	**Function 1:** In *normal mode*, count and generate a flag or an interrupt when the counter reaches the after run value.
1h	**Function 2:** In *normal mode*, count until the counter reaches the after run value and enters Low-power mode.
2h	**Function 3:** In *normal mode*, count until the counter reaches the after run value and enters low power mode. Once in Low-power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
3h	**Function 4:** In Low-power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
4h	**Function 5:** In Low-power mode, count and do not wake up unless the counter overflow occurs or if the device wakes up by another wake-up input source.

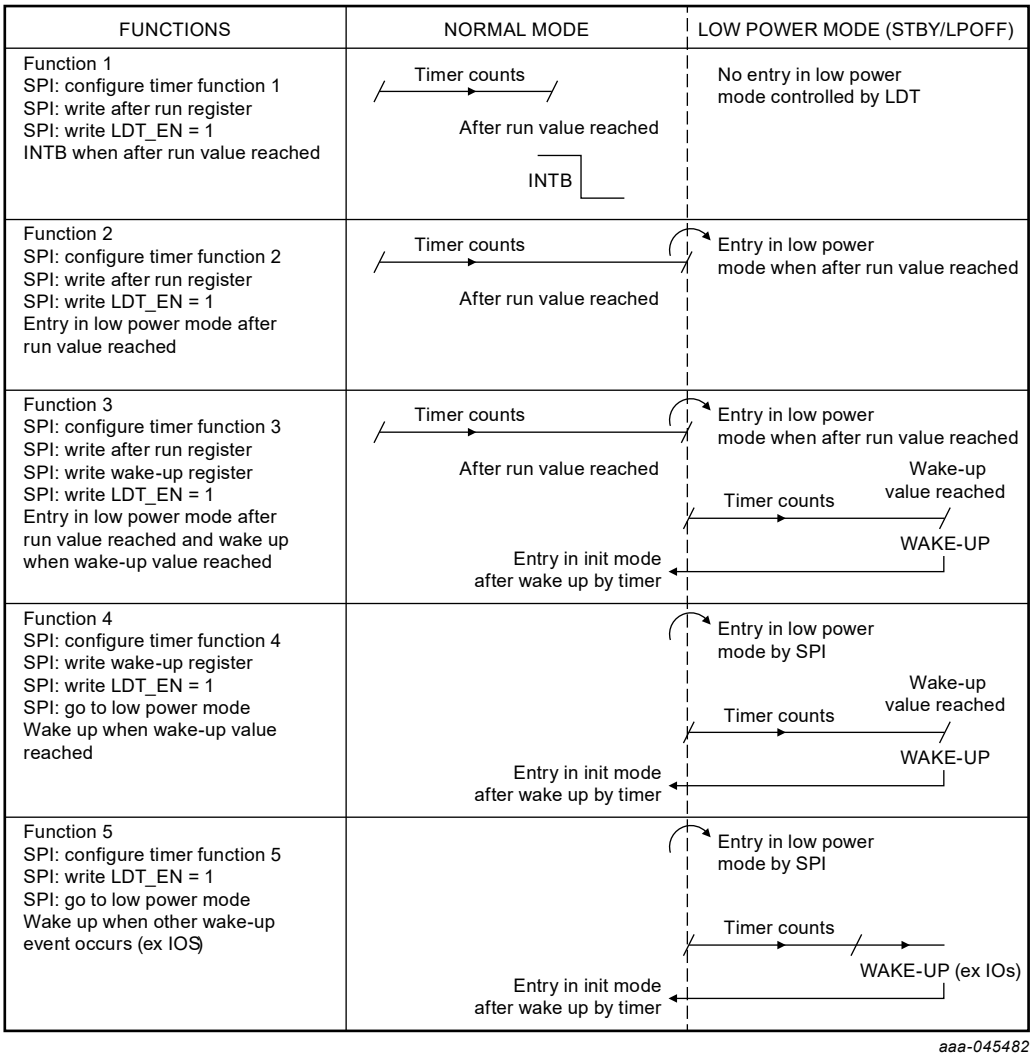

Figure 46. Long Duration Timer functions

19.4.4 LDT operation

The timer is configured and operates with the M_LDT_CFG1, M_LDT_CFG2, M_LDT_CFG3 and M_LDT_CTRL registers.

The 16-bit after-run value is configured and read with M_LDT_CFG1 register and the 24-bit wake-up value is configured and read in the corresponding M_LDT_CFG2 and M_LDT_CFG3 registers.

Figure 47 describes the independent state machine for the long duration timer (LDT). After a POR_M of the device, the LDT is in idle mode waiting for configuration. The after-run timer function starts when the LDT_EN bit is set by SPI. The wake-up timer function starts when the device enters Low-power mode.

The LDT counter keeps the last count until the LDT is enabled again, that is, the LDT counter is reset when LDT_EN goes from 0 to 1.

- When function 1 is selected and the counter is launched, once the after run value is reached (EOT: End of timer) an interrupt is generated and the counter is stopped
- When function 2 is selected and the counter is launched, once the after run value is reached (EOT) the device goes to Low-power mode and the counter is stopped.

- When function 3 is selected and the counter is launched, once the after run value is reached (EOT) the device goes to Low-power mode. The counter is reset and restarts. When the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. If the device is awakened by another wake-up source, the counter is stopped.
- When function 4 is selected and the counter is launched, once the wake-up value is reached (EOT) the device wakes up and the counter is stopped. If the device is awakened by another wake-up source, the counter is stopped.
- When function 5 is selected and the counter reaches its maximum value (FFFFFFh), the device wakes up and the counter is stopped. The counter is not stopped if a wake-up event is trigged while counting. The counter must be disabled (LDT_EN = 0) before reading its value.

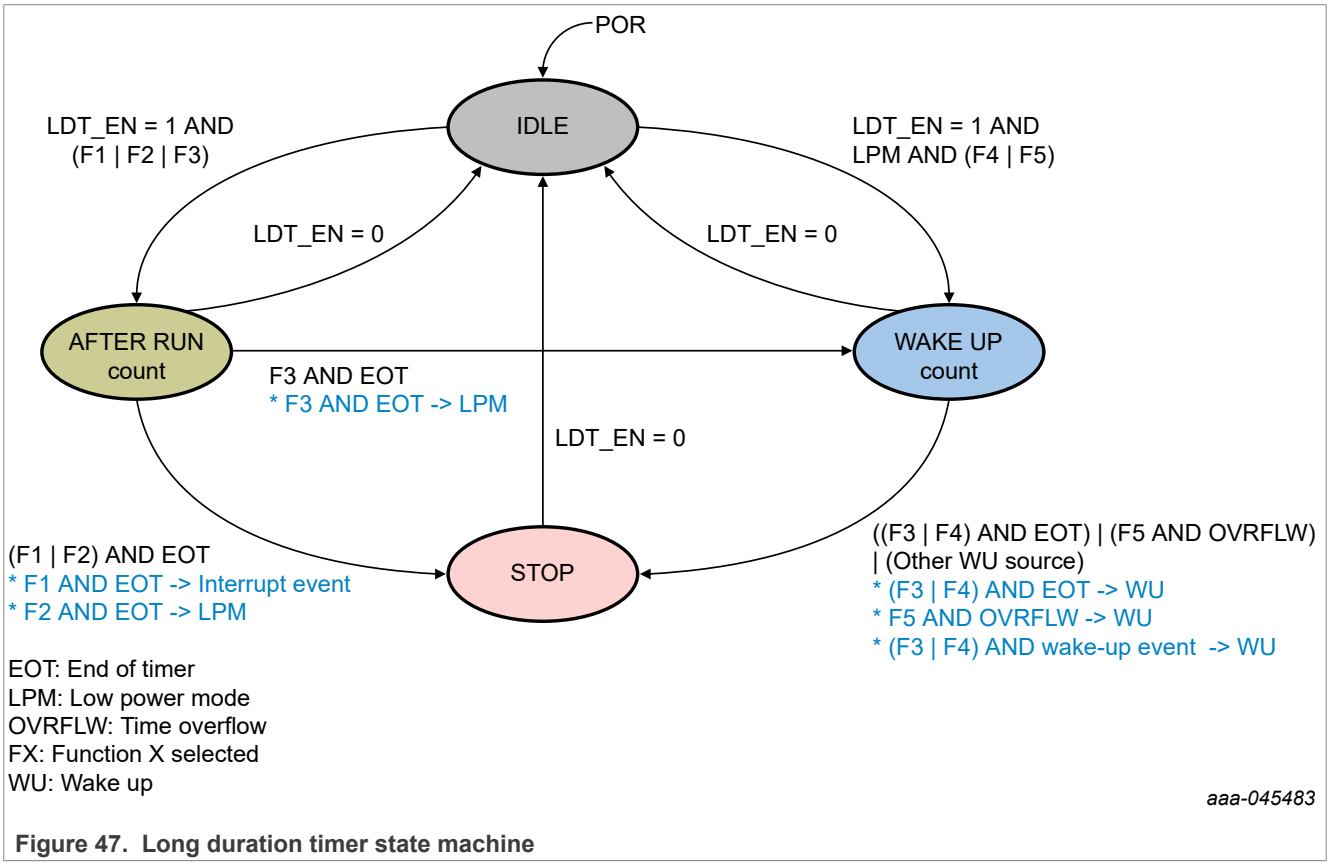

Figure 47. Long duration timer state machine

20 OTP and Debug mode

OTP emulation and programming performed by the customer is allowed during engineering development using OTP mode with NXP's latest graphical user interface and socketed evaluation board.

Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

When an OTP configuration is emulated, the configuration remains available until the POR_M / POR_FS of the digital circuitry. The fail-safe configuration is lost in low power mode (*LPOFF mode* and *standby mode*) since the fail-safe digital is OFF in these modes.

The main digital configuration is lost when VSUP is removed, which means $V_{BOS} < V_{BOS\_POR}$. When an OTP configuration is programmed, the device will start with the programmed OTP configuration by default. A programmed part cannot be re-programmed, but can be emulated. To enter OTP mode, the voltage at the DEBUG pin must be set to V_{OTP} prior to applying VSUP voltage.

During the power-up sequence, the main and the fail-safe state machines will stop prior to starting the regulators, waiting for SPI communication to send an OTP configuration to the device. When the OTP configuration is complete, the fail-safe state machine will start in Debug mode when the voltage at the DEBUG pin is below V_{NORM_MAX} (NXP recommends applying 0 V or ground).

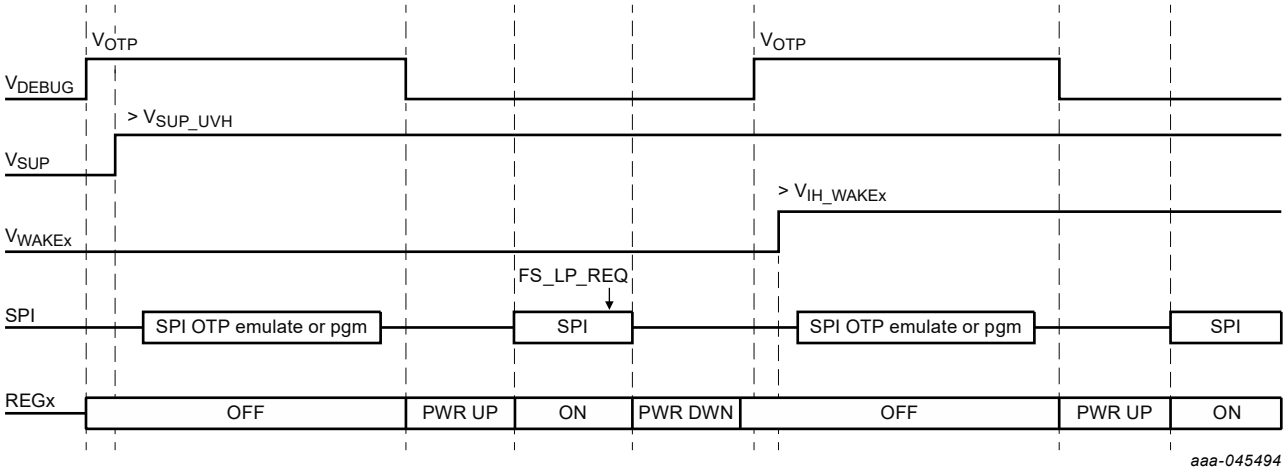

Figure 48. OTP mode time chart

Debug mode is intended for software debugging or first MCU programming during ECU assembly. To enter Debug mode without first entering OTP mode, the voltage at the DEBUG pin must be set to V_{DBG} prior to applying the VSUP voltage. During the power-up sequence, the fail-safe state machine will start in Debug mode and reach the *initialization phase*.

In Debug mode, the watchdog window is infinite opened, the RSTB 8 s counter is disabled, FS0B is maintained low and cannot be released. The *Deep Fail Safe* is deactivated. The Debug mode status is reported by the DBG_MODE bit in FS_STATES register (latched information) or by VDBG_VOLT_S in M_STATUS (real time information). To exit Debug mode, write to the EXIT_DBG_MODE bit in the FS_STATES register.

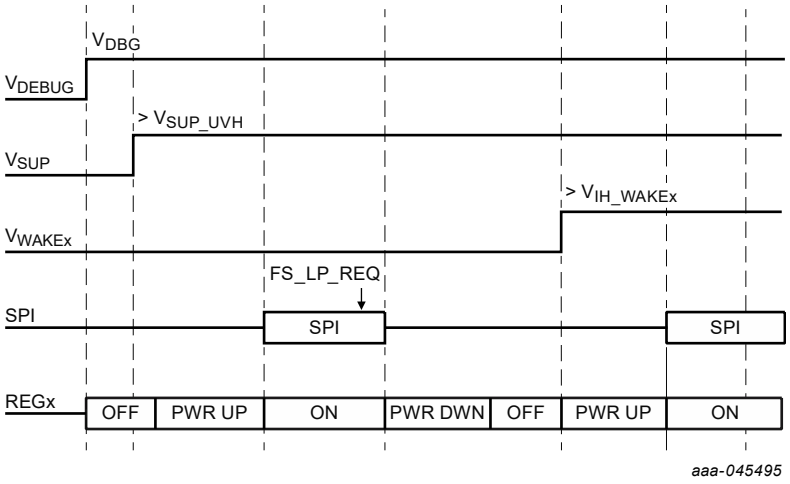

Figure 49. Debug mode time chart

Table 126. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < V_{SUP} < 36 V, V_{PRE_PWM} + V_{PRE_HDR} < V_{SUP_PWR} < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{NORM}	Voltage to apply at DEBUG pin to exit OTP mode and to start in *normal mode*	0	—	1.8	V
V_{OTP}	Voltage to apply at DEBUG pin to enter OTP mode (State machines stopped for OTP emulation/ programming)	7.4	—	8.4	V
V_{DBG}	Voltage to apply at DEBUG pin to enter *debug mode* (Automatic start in Debug mode with watchdog disabled)	2.5	—	6	V
t_{OTP_DBG}	DEBUG pin filtering time to enter OTP mode or *debug mode*	4	6	8	µs

20.1 OTP mode flowchart

The diagram in Figure 50 explains the steps to enter OTP mode, emulate or program an OTP configuration, start the fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

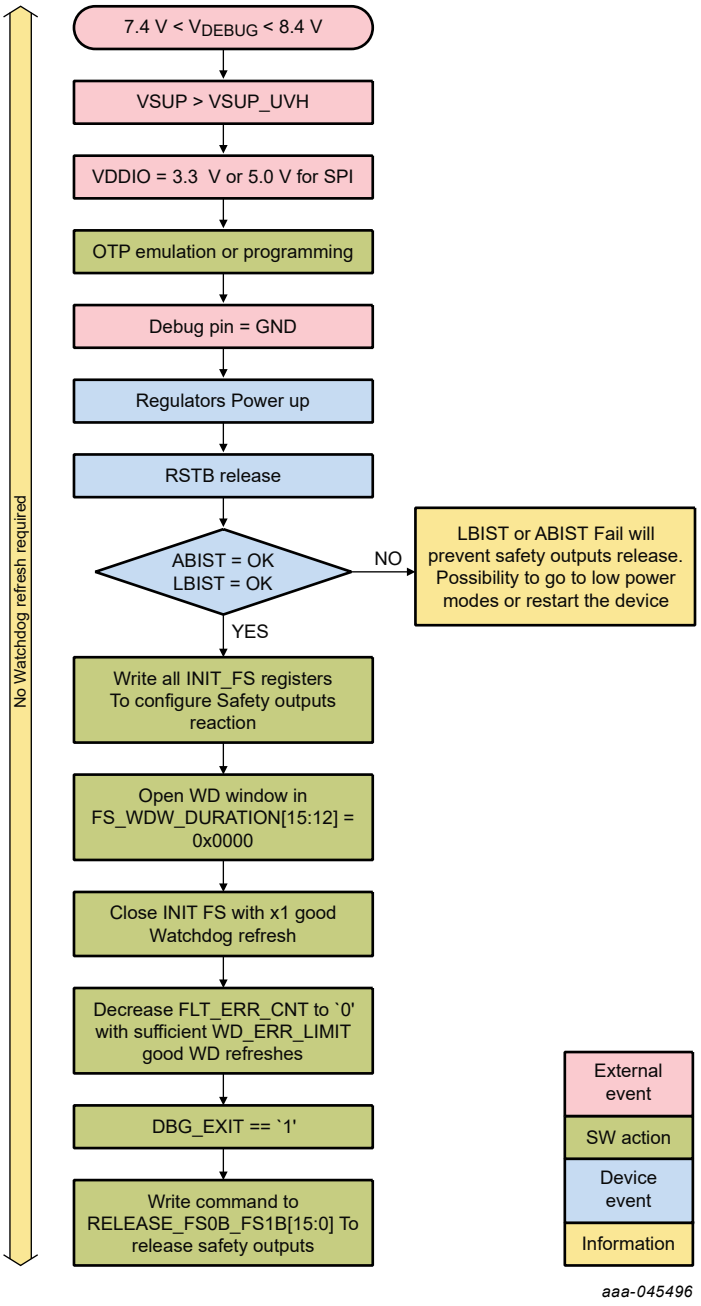

Figure 50. OTP mode flowchart until safety outputs release

20.2 Debug mode flowchart

The diagram in Figure 51 explains the steps to enter Debug mode without first entering OTP mode, start the fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

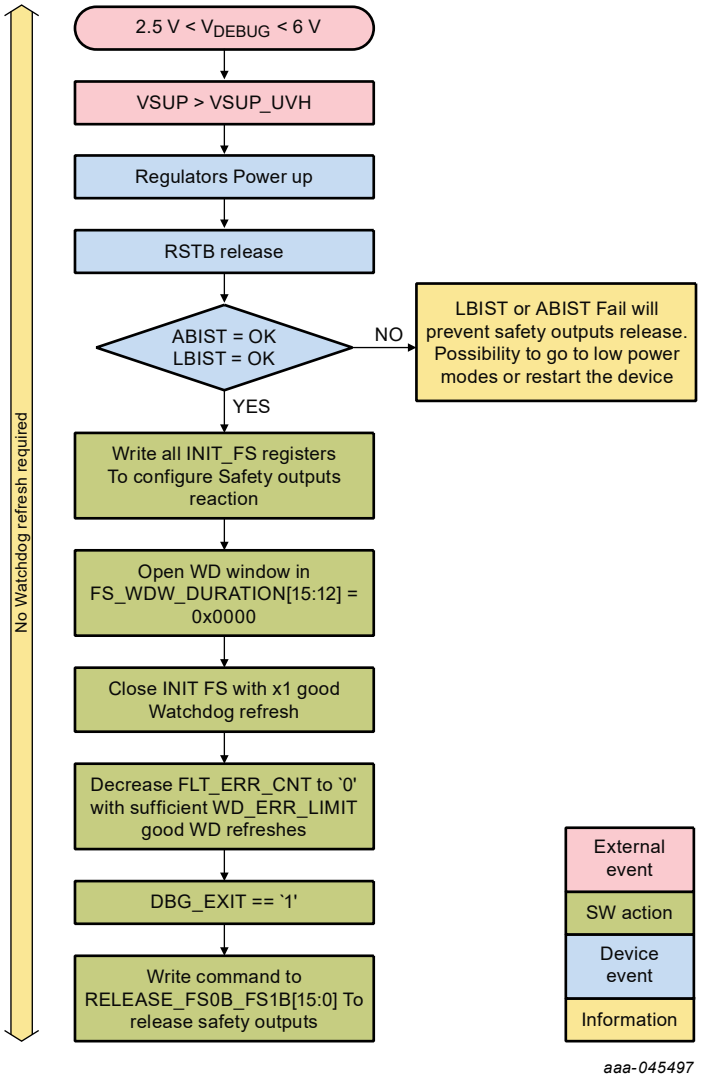

Figure 51. Debug mode flowchart until safety outputs release

21 Application schematics

Refer to AN12995 for further information.

21.1 Front-end configuration

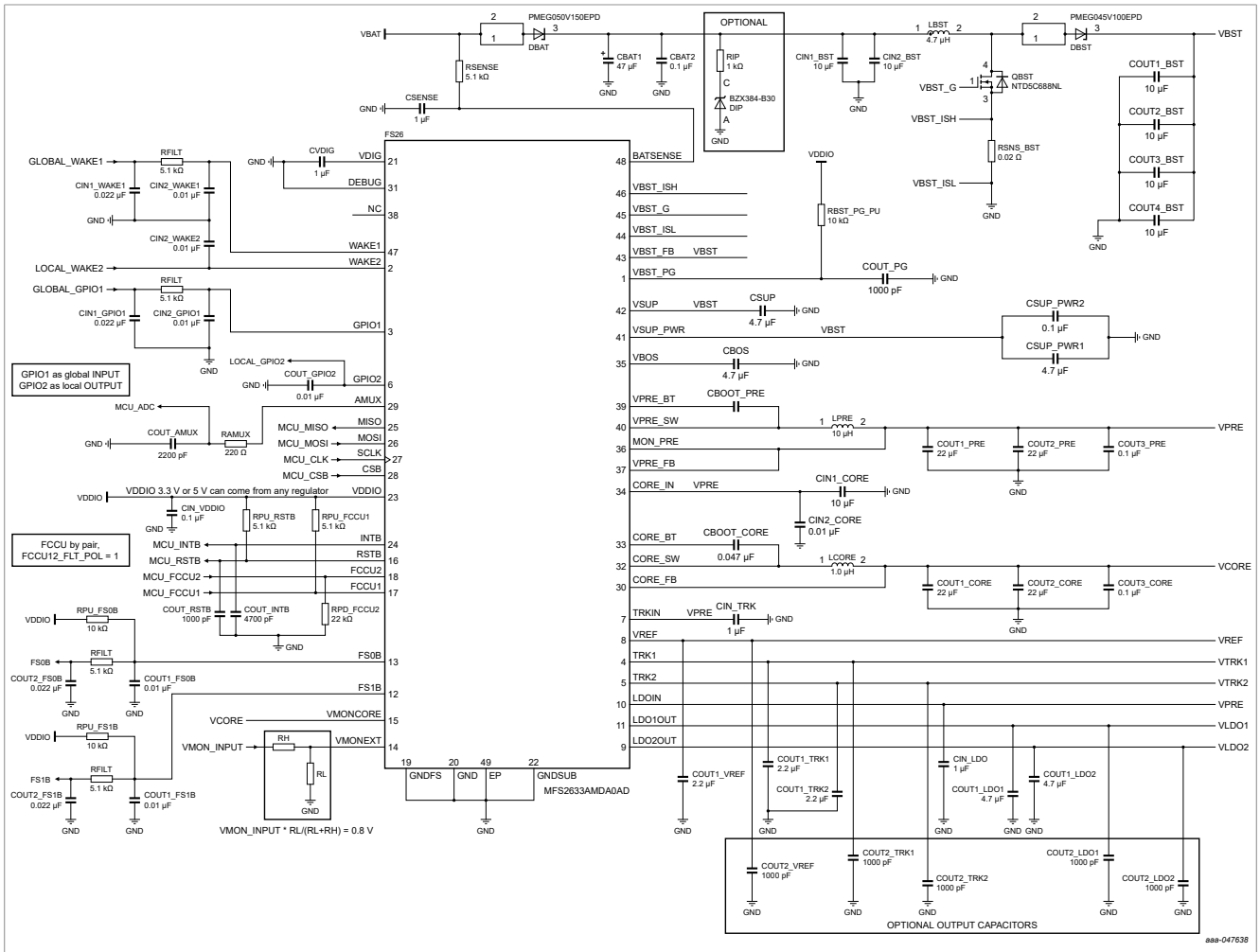

Figure 52. Application schematic in front-end configuration for F_{PRE} = 450 kHz

21.2 Back-end configuration

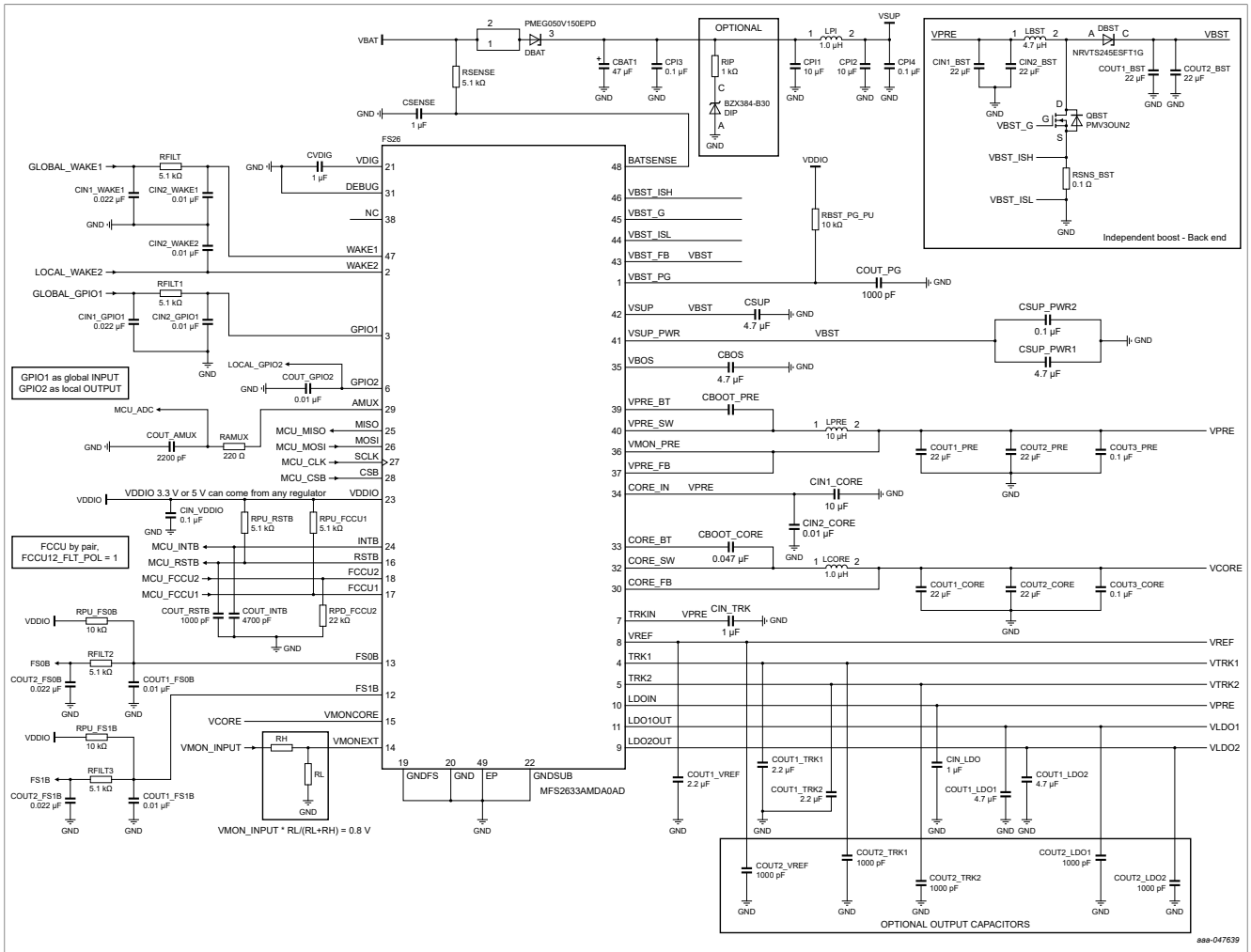

Figure 53. Application schematic in back-end configuration for F_{PRE} = 450 kHz

22 OTP configurations

Table 127. OTP configurations

	Register bitfield	Register description	MFS2613AMDA2AD	MFS2613AMDA3AD	MFS2613AMDA4AD	MFS2613AMDA6AD	MFS2621AMDABAD	MFS2613AMDDCAD
System configuration	VSUP_UVTH_OTP	VSUP UV threshold	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V
	WK1DFS_DIS_OTP	Exit DFS on WAKE1 event	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled	DFS exit on WAKE1 event enabled
	RETRY_DIS_OTP	Auto-retry power-up from DFS	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled	Auto-retry enabled
	RETRY_MODE_OTP	Auto-retry mode	Infinite retry	Infinite retry	Limited retry	Limited retry	Infinite retry	Limited retry
	RETRY_MSK_OTP[3:0]	Auto-retry timer limit	800 ms	800 ms	800 ms	800 ms	1600 ms	800 ms
	CLK_FREQ_OTP[1:0]	Clock frequency selection	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz
	BOS_IN_OTP[1:0]	VBOS input selection	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}
Power-up sequence	TSLOT_OTP[1:0]	Power-up slot time	250 µs	250 µs	250 µs	250 µs	1000 µs	250 µs
	SLOT_BYP_OTP[2:0]	Power-up slot bypass	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled	Bypass disabled
	CORE_SLOT_OTP[2:0]	VCORE power-up slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 6	Slot 0
	LDO1_SLOT_OTP[2:0]	LDO1 power-up slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0
	LDO2_SLOT_OTP[2:0]	LDO2 power-up slot	Slot 0	Slot 1	Slot 0	Slot 0	Slot 0	Slot 0
	TRK1_SLOT_OTP[2:0]	TRK1 power-up slot	Slot 2	Slot 2	Slot 2	Slot 0	Slot 0	Slot 2
	TRK2_SLOT_OTP[2:0]	TRK2 power-up slot	Slot 3	Slot 3	Slot 3	Slot 0	OFF	Slot 3
	VREF_SLOT_OTP[2:0]	VREF power-up slot	Slot 1	Slot 0	Slot 1	Slot 0	Slot 0	Slot 1
	GPIO1_SLOT_OTP[2:0]	GPIO1 power-up slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
	GPIO2_SLOT_OTP[2:0]	GPIO2 power-up slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
I/O configuration	GPIO1STAGE_OTP[1:0]	GPIO configuration	GPIO configured as an input	Push-pull driver	GPIO configured as an input	GPIO configured as an input	Low-side Driver	GPIO configured as an input
	GPIO1_MODE_OTP	GPIO low-side polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO1PU_OTP	GPIO1 pull-up	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled
	GPIO1PD_OTP	GPIO1 pull-down	Pull-down enabled	Pull-down disabled	Pull-down disabled	Pull-down enabled	Pull-down enabled	Pull-down disabled
	GPIO1TH_OTP	GPIO1 detection threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold
	GPIO1TSD_PD_OTP	GPIO1 TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
	GPIO2STAGE_OTP[1:0]	GPIO configuration	Low-side driver	Push-pull driver	GPIO configured as an input	GPIO configured as an input	Low-side driver	GPIO configured as an input
	GPIO2_MODE_OTP	GPIO low-side polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO2_VCORE_PGOOD_OTP	GPIO2 VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD
	GPIO2PU_OTP	GPIO2 pull-up	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled	Pull-up disabled
	GPIO2PD_OTP	GPIO2 pull-down	Pull-down disabled	Pull-down disabled	Pull-down disabled	Pull-down enabled	Pull-down enabled	Pull-down disabled
	GPIO2TH_OTP	GPIO2 detection threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold
	WK1TH_OTP	WAKE1 detection threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	High-voltage threshold
	WK2TH_OTP	WAKE2 detection threshold	High-voltage threshold	High-voltage threshold	High-voltage threshold	Low-voltage threshold	High-voltage threshold	High-voltage threshold

Table 127. OTP configurations*...continued*

	WK1PD_OTP	WAKE1 pull-down	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled
	WK2PD_OTP	WAKE2 pull-down	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled	Pull-down enabled
	WK1PD_SEL_OTP	WAKE1 pull-down selection	200 kΩ	200 kΩ	200 kΩ	10 kΩ	200 kΩ	200 kΩ
	WK2PD_SEL_OTP	WAKE2 pull-down selection	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ
VPRE configuration	VPRE_OTP[5:0]	VPRE in *normal mode*	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VPRE_LP_OTP[5:0]	VPRE in *standby mode*	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	VPRE_LP_DVS_OTP[1:0]	DVS ramp rate	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs	22 mV/µs
	VPRE_OC_OTP[2:0]	VPRE overcurrent flag	2.2 A	1.54 A	2.2 A	1.54 A	2.2 A	2.2 A
	VPRE_OC_DGLT_OTP[1:0]	Overcurrent deglitch	2000 µs	250 µs	2000 µs	250 µs	2000 µs	2000 µs
	VPRE_SS_OTP[1:0]	Soft-start ramp	2150 µs	538 µs	2150 µs	269 µs	2150 µs	2150 µs
	VPRE_PDWN_DLY_OTP[1:0]	VPRE power-down delay	100 µs	100 µs	100 µs	100 µs	100 µs	100 µs
	VPRE_BOS_OTP[5:0]	VPRE transition voltage	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	VPRE_PH_OTP[1:0]	VPRE phase delay	No delay	No delay	No delay	No delay	No delay	No delay
	VPRE_SR_OTP	VPRE SW slew rate	Fast mode	Fast mode	Slow mode	Fast mode	Fast mode	Slow mode
	VPRE_GM_OTP[1:0]	Transconductance amp	15 µS	15 µS	15 µS	15 µS	15 µS	15 µS
	VPRE_CCOMP_OTP[1:0]	Comp capacitance	12.0 pF	23.0 pF	12.0 pF	12.0 pF	12.0 pF	12.0 pF
	VPRE_RCOMP_OTP[2:0]	Comp resistance	1300 kΩ	1137 kΩ	1300 kΩ	1300 kΩ	1300 kΩ	1300 kΩ
	VPRE_SC_OTP[5:0]	Slope compensation	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs	266 mV/µs
	VPRE_PFM_TON_OTP[1:0]	HS minimum ON in PFM mode	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns
	VPRE_PFM_TOFF_OTP[1:0]	HS minimum OFF in PFM mode	720 ns	720 ns	720 ns	720 ns	720 ns	720 ns
	VPRE_CLK_OTP	VPRE clock selection	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40
	VPRETDFS_OTP	TSD behavior	Go to DFS	VPRE disabled only	Go to DFS	VPRE disabled only	Go to DFS	Go to DFS
	VPRETSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
VBST configuration	VBST_OTP[4:0]	VBST voltage	8.00 V	7.00 V	8.00 V	8.00 V	8.00 V	8.00 V
	VBST_CFG_OTP	VBST configuration	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost
	VBST_OV_OTP	VBST_FB overvoltage monitor mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode
	VBST_PH_OTP[1:0]	Phase delay	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle
	VBSTLS_SR_OTP	Low-side slew rate	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 2 Ω / PD = 1.7 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω
	VBST_TON_MIN_OTP[1:0]	Minimum ON time	200 ns	200 ns	200 ns	200 ns	200 ns	200 ns
	VBST_SS_OTP[1:0]	VBST soft-start	425 µs	850 µs	425 µs	425 µs	425 µs	425 µs
	VBST_MAX_DC_OTP[1:0]	Max duty cycle	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %
	VBST_CCOMP_OTP[1:0]	Comp capacitance	200 pF	200 pF	200 pF	200 pF	200 pF	200 pF
	VBST_GMCOMP_OTP[1:0]	Comp transconductance	3.9 µS	5.1 µS	3.9 µS	3.9 µS	3.9 µS	3.9 µS
	VBST_RCOMP_OTP[1:0]	Comp resistance	740 kΩ	500 kΩ	500 kΩ	740 kΩ	740 kΩ	500 kΩ
	VBST_ILIM_OTP[1:0]	Current limit	180 mV/RSNS	120 mV/RSNS	150 mV/RSNS	120 mV/RSNS	180 mV/RSNS	150 mV/RSNS
	VBST_SC_OTP[5:0]	Slope compensation	155 mV/µs	127 mV/µs	169 mV/µs	155 mV/µs	155 mV/µs	169 mV/µs

Table 127. OTP configurations*...continued*

VCORE configuration	VCORE_OTP[7:0]	VCORE voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	CORE_CTRL_OTP	Control type	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control
	-	VCORE operating mode	CCM only	CCM only	CCM only	CCM only	CCM only	CCM only
	CORE_SS_OTP[1:0]	Soft-start	5 mV/µs	10 mV/µs	10 mV/µs	5 mV/µs	5 mV/µs	20 mV/µs
	CORE_ILIM_OTP[1:0]	VCORE current limit	2.7 A	2.7 A	1.7 A	1.7 A	2.7 A	1.7 A
	CORE_PH_OTP[1:0]	Phase delay	2 Clock Cycles	3 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles
	COREHS_SR_OTP[1:0]	High-side slew rate	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.0 V/ns Fall = 0.6 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns
	CORE_GM_OTP[1:0]	Transconductance amp	53 µS	53 µS	26 µS	26 µS	53 µS	26 µS
	CORE_CCOMP_OTP[1:0]	Comp capacitance	50 pF	50 pF	50 pF	50 pF	50 pF	50 pF
	CORE_RCOMP_OTP[1:0]	Comp resistance	200 kΩ	150 kΩ	200 kΩ	200 kΩ	150 kΩ	200 kΩ
	CORE_LSEL_OTP[1:0]	VCORE inductor	1 µH	1 µH	1 µH	1 µH	1 µH	1 µH
	CORETDFS_OTP	TSD behavior	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS
	CORETSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
LDO1 configuration	VLDO1_OTP	LDO1 voltage in *normal mode*	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	VLDO1_LP_OTP	LDO1 voltage in *standby mode*	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	LDO1_LP_EN_OTP	LDO1 in *standby mode*	LDO1 enabled	LDO1 disabled	LDO1 enabled	LDO1 enabled	LDO1 enabled	LDO1 enabled
	LDO1TDFS_OTP	TSD behavior	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only
	LDO1TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
LDO2 configuration	VLDO2_OTP	LDO2 voltage in *normal mode*	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	VLDO2_LP_OTP	LDO2 voltage in *standby mode*	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	LDO2_LP_EN_OTP	LDO2 in *standby mode*	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled	LDO2 enabled
	LDO2TDFS_OTP	TSD behavior	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only
	LDO2TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
TRK1 configuration	TRK1_SEL_OTP[1:0]	TRK1 input selection	VREF	LDO2	Internal LDO_REF	VREF	VREF	Internal LDO_REF
	TRK1TDFS_OTP	TSD behavior	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only
	TRK1TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
TRK2 configuration	TRK2_SEL_OTP[1:0]	TRK2 input selection	LDO2	LDO2	Internal LDO_REF	LDO2	VREF	Internal LDO_REF
	TRK2TDFS_OTP	TSD behavior	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only
	TRK2TSD_PD_OTP	TSD pull-down	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD	Pull-down enabled in TSD
VREF configuration	VREF_OTP	VREF voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	VLDO_REF_OTP[1:0]	Internal LDO reference	1.2 V	3.3 V	5.0 V	3.3 V	1.2 V	3.3 V
VMON_PRE configuration	VPRE_V_OTP[5:0]	VMON_PRE monitoring voltage	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VMON_PRE_OVTH_OTP[3:0]	VMON_PRE overvoltage threshold	110.5 %	110.5 %	110 %	110 %	110 %	110 %
	VMON_PRE_UVTH_OTP[3:0]	VMON_PRE undervoltage threshold	90 %	94 %	90 %	90 %	90 %	90 %

Table 127. OTP configurations*...continued*

	VMON_PRE_OVDGLT_OTP	VMON_PRE overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_PRE_UVDGLT_OTP[1:0]	VMON_PRE undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_CORE configuration	VCORE_V_OTP[7:0]	VMON_CORE monitoring voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	VMON_CORE_OVTH_OTP[3:0]	VMON_CORE overvoltage threshold	104.5 %	108.00 %	106 %	106 %	106 %	106 %
	VMON_CORE_UVTH_OTP[3:0]	VMON_CORE undervoltage threshold	95.5 %	95.5 %	94.00 %	94.00 %	94.00%	94.00 %
	VMON_CORE_OVDGLT_OTP	VMON_CORE overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_CORE_UVDGLT_OTP[1:0]	VMON_CORE undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_LDO1 configuration	LDO1_V_OTP	VMON_LDO1 monitoring voltage	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	VMON_LDO1_OVTH_OTP[3:0]	VMON_LDO1 overvoltage threshold	106.00 %	108.00 %	107.50 %	107.50 %	106.00 %	107.50 %
	VMON_LDO1_UVTH_OTP[3:0]	VMON_LDO1 undervoltage threshold	94.00 %	91.00 %	92.50 %	93.00 %	94.00 %	92.50 %
	VMON_LDO1_UVDTH_OTP	VMON_LDO1 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMON_LDO1_OVDGLT_OTP	VMON_LDO1 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_LDO1_UVDGLT_OTP[1:0]	VMON_LDO1 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
	LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled
VMON_LDO2 configuration	LDO2_V_OTP	VMON_LDO2 monitoring voltage	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	VMON_LDO2_OVTH_OTP[3:0]	VMON_LDO2 overvoltage threshold	106.00 %	104.5 %	106.00 %	106.00 %	106.00 %	106.00 %
	VMON_LDO2_UVTH_OTP[3:0]	VMON_LDO2 undervoltage threshold	94.00 %	95.5 %	94.00 %	94.00 %	94.00 %	94.00 %
	VMON_LDO2_UVDTH_OTP	VMON_LDO2 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMON_LDO2_OVDGLT_OTP	VMON_LDO2 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_LDO2_UVDGLT_OTP[1:0]	VMON_LDO2 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
	LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled
VMON_TRK1 configuration	TRK1_V_OTP[1:0]	VMON_TRK1 monitoring voltage	5.0 V	5.0 V	5.0 V	5.0 V	3.3 V	3.3 V
	VMON_TRK1_OVTH_OTP[3:0]	VMON_TRK1 overvoltage threshold	104.5 %	108.00 %	106 %	107.50 %	106.00 %	106 %
	VMON_TRK1_UVTH_OTP[3:0]	VMON_TRK1 undervoltage threshold	95.5 %	92.00 %	94 %	93.00 %	94 %	94 %
	VMON_TRK1_OVDGLT_OTP	VMON_TRK1 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_TRK1_UVDGLT_OTP[1:0]	VMON_TRK1 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_TRK2 configuration	TRK2_V_OTP[1:0]	VMON_TRK2 monitoring voltage	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V	3.3 V
	VMON_TRK2_OVTH_OTP[3:0]	VMON_TRK2 overvoltage threshold	104.5 %	108.00 %	106 %	106 %	104.50 %	106 %
	VMON_TRK2_UVTH_OTP[3:0]	VMON_TRK2 undervoltage threshold	95.5 %	92.00 %	94.00 %	94.00 %	95.50 %	94.00 %
	VMON_TRK2_OVDGLT_OTP	VMON_TRK2 overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_TRK2_UVDGLT_OTP[1:0]	VMON_TRK2 undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
VMON_REF configuration	VREF_V_OTP	VMON_VREF monitoring voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	VMON_VREF_OVTH_OTP[3:0]	VMON_VREF overvoltage threshold	104.50 %	105.00 %	104.50 %	105.00 %	105.00 %	104.50 %
	VMON_VREF_UVTH_OTP[3:0]	VMON_VREF undervoltage threshold	95.50 %	95.00 %	95.50 %	95.00 %	95.00 %	95.50 %
	VMON_VREF_OVDGLT_OTP	VMON_REF overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_VREF_UVDGLT_OTP[1:0]	VMON_REF undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs

Table 127. OTP configurations*...continued*

	VREF_PLIFT_DIS_OTP	VREF pin lift detection	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled
VMON_EXT configuration	VMON_EXT_OVTH_OTP[3:0]	VMON_EXT overvoltage threshold	104.50 %	110.00 %	110.00 %	105.00 %	105.00 %	110.00 %
	VMON_EXT_UVTH_OTP[3:0]	VMON_EXT undervoltage threshold	95.50 %	95.00 %	90 %	95.00 %	95.00 %	90 %
	VMON_EXT_OVDGLT_OTP	VMON_EXT overvoltage deglitch	45 µs	45 µs	45 µs	45 µs	45 µs	45 µs
	VMON_EXT_UVDGLT_OTP[1:0]	VMON_EXT undervoltage deglitch	40 µs	40 µs	40 µs	25 µs	40 µs	40 µs
ABIST1 configuration	ABIST1_VPRE_EN_OTP	ABIST1 on VMON_PRE	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_VCORE_EN_OTP	ABIST1 on VMON_CORE	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_LDO1_EN_OTP	ABIST1 on VMON_LDO1	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_LDO2_EN_OTP	ABIST1 on VMON_LDO2	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_TRK1_EN_OTP	ABIST1 on VMON_TRK1	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_TRK2_EN_OTP	ABIST1 on VMON_TRK2	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 disabled	ABIST1 enabled
	ABIST1_VREF_EN_OTP	ABIST1 on VMON_REF	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled
	ABIST1_EXT_EN_OTP	ABIST1 on VMON_EXT	ABIST1 disabled	ABIST1 enabled	ABIST1 enabled	ABIST1 enabled	ABIST1 disabled	ABIST1 enabled
System safety configuration	FAULT_DFS_EN_OTP	DFS entry mode	Go to DFS when FLT_ERR_CNT = max	Go to DFS when FLT_ERR_CNT = max	Go to DFS when FLT_ERR_CNT = max	Go to DFS when FLT_ERR_CNT = max	Go to DFS when FLT_ERR_CNT = max	Go to DFS when FLT_ERR_CNT = max
	FS1B_FS0B_EN_OTP	FS1B assertion mode	Delayed assertion disabled	Delayed assertion enabled	Delayed assertion enabled	Delayed assertion enabled	Delayed assertion disabled	Delayed assertion enabled
	PRE_RSTB_DLY_EN_OTP	RSTB delay from FS0B	0 µs	100 µs	0 µs	100 µs	0 µs	0 µs
	DIS8S_DIS_OTP	RSTB low detection timer	Timer disabled	8 second timer enabled	8 second timer enabled	8 second timer enabled	8 second timer enabled	8 second timer enabled
	WD_DIS_OTP	Watchdog timer	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled	Watchdog timer enabled
	LBIST_STDBY_OTP[7:0]	Bypass LBIST from *standby mode*	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST
	MDFS_DIS_OTP	Main DFS availability	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available
	DFS_DIS_OTP	Deep Fail Safe state availability	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available	Deep Fail Safe available
OTP ID	PROG_IDH_OTP[7:0]	Program ID high	A	A	A	A	A	D
	PROG_IDL_OTP[7:0]	Program ID low	2	3	4	6	B	C
FS versioning bits	VMON_EXT_DIS_VOTP	External monitor	VMON disabled	VMON enabled	VMON enabled	VMON enabled	VMON enabled	VMON enabled
	FCCU_DIS_VOTP	FCCU function	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available
	ERRMON_DIS_VOTP	ERRMON function	ERRMON not available	ERRMON available	ERRMON not available	ERRMON available	ERRMON not available	ERRMON not available

23 Packaging

23.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

Table 128. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

23.2 Package outline

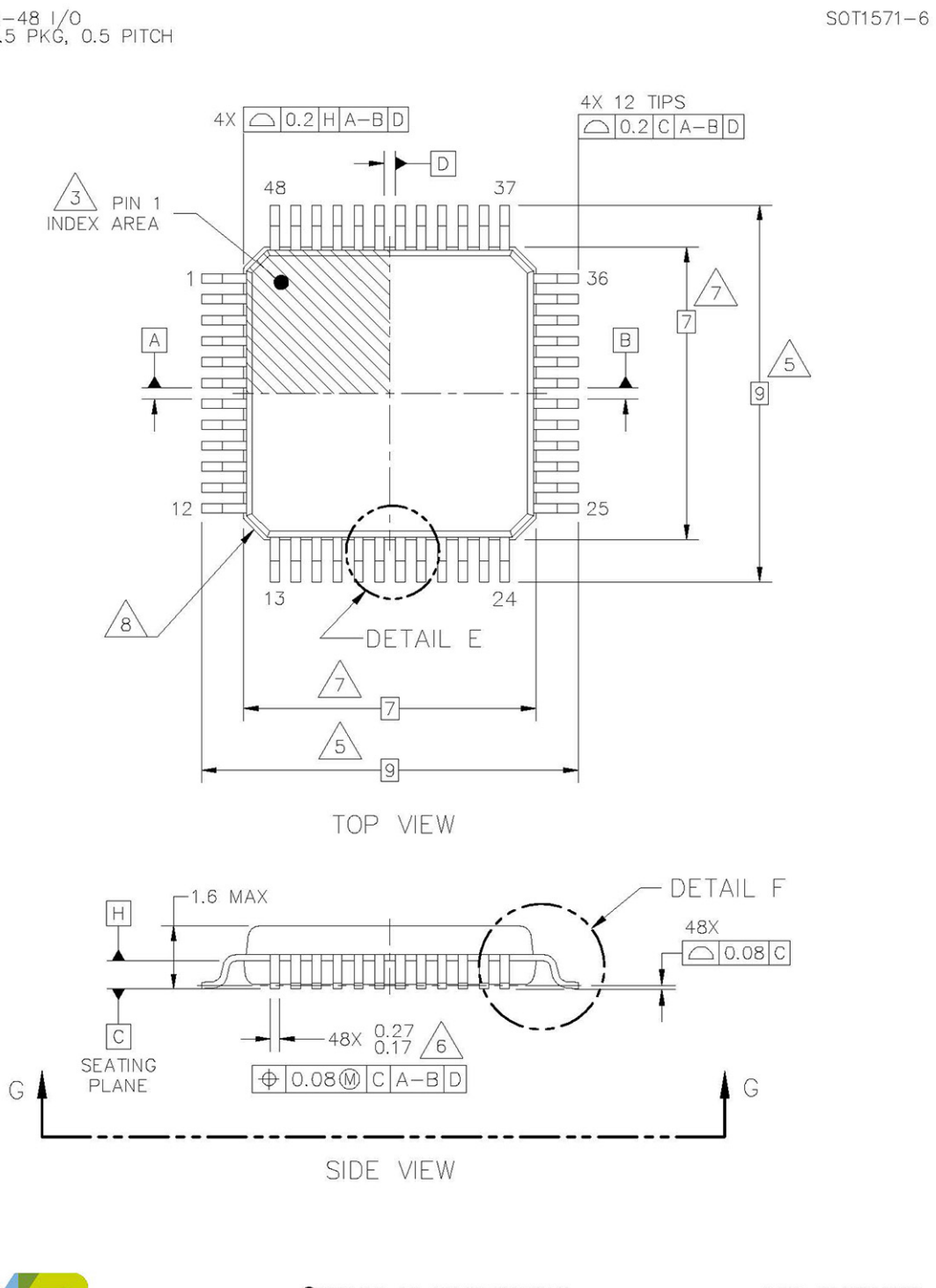

Figure 54. SOT1571-6

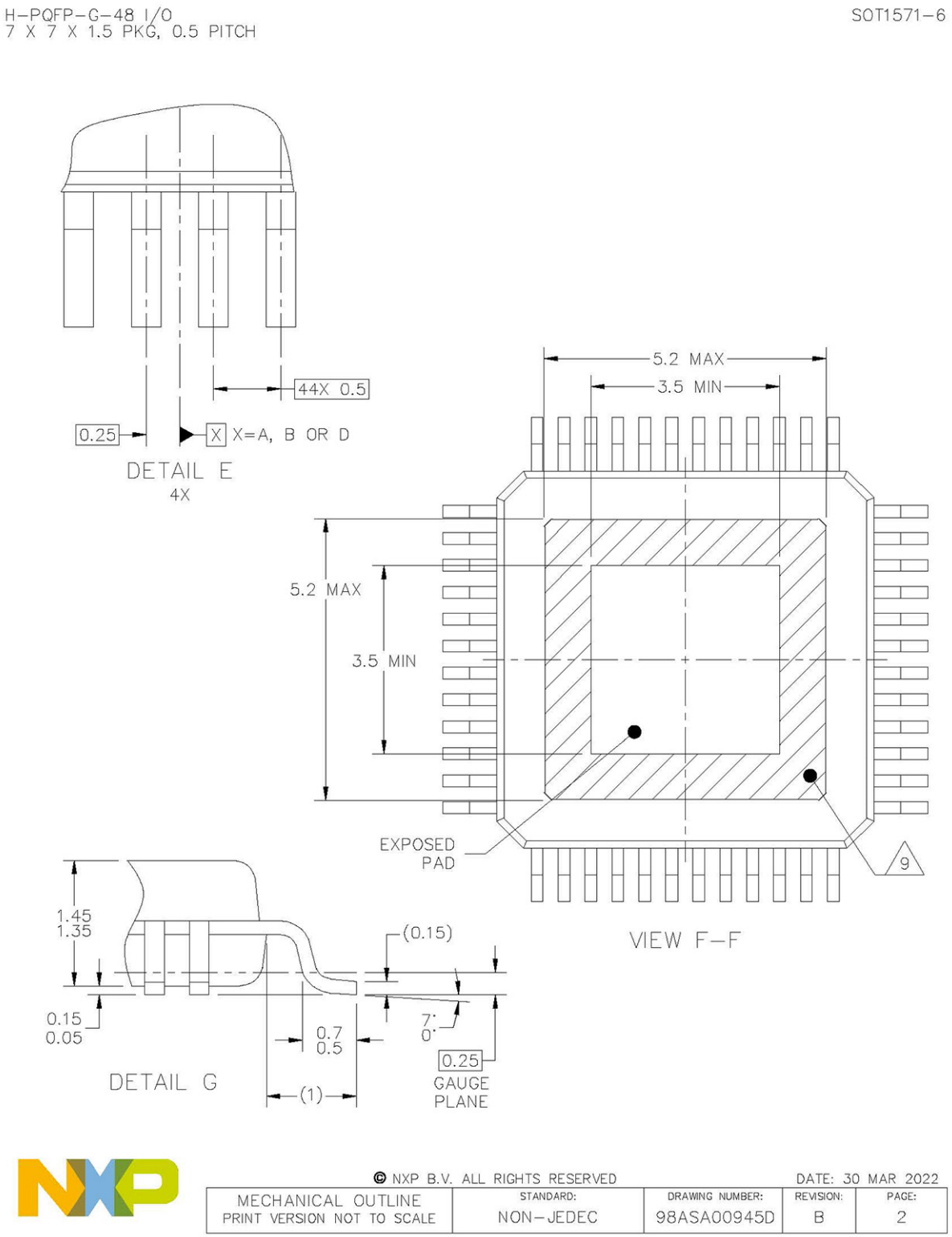

Figure 55. Package outline details (SOT1571-6)

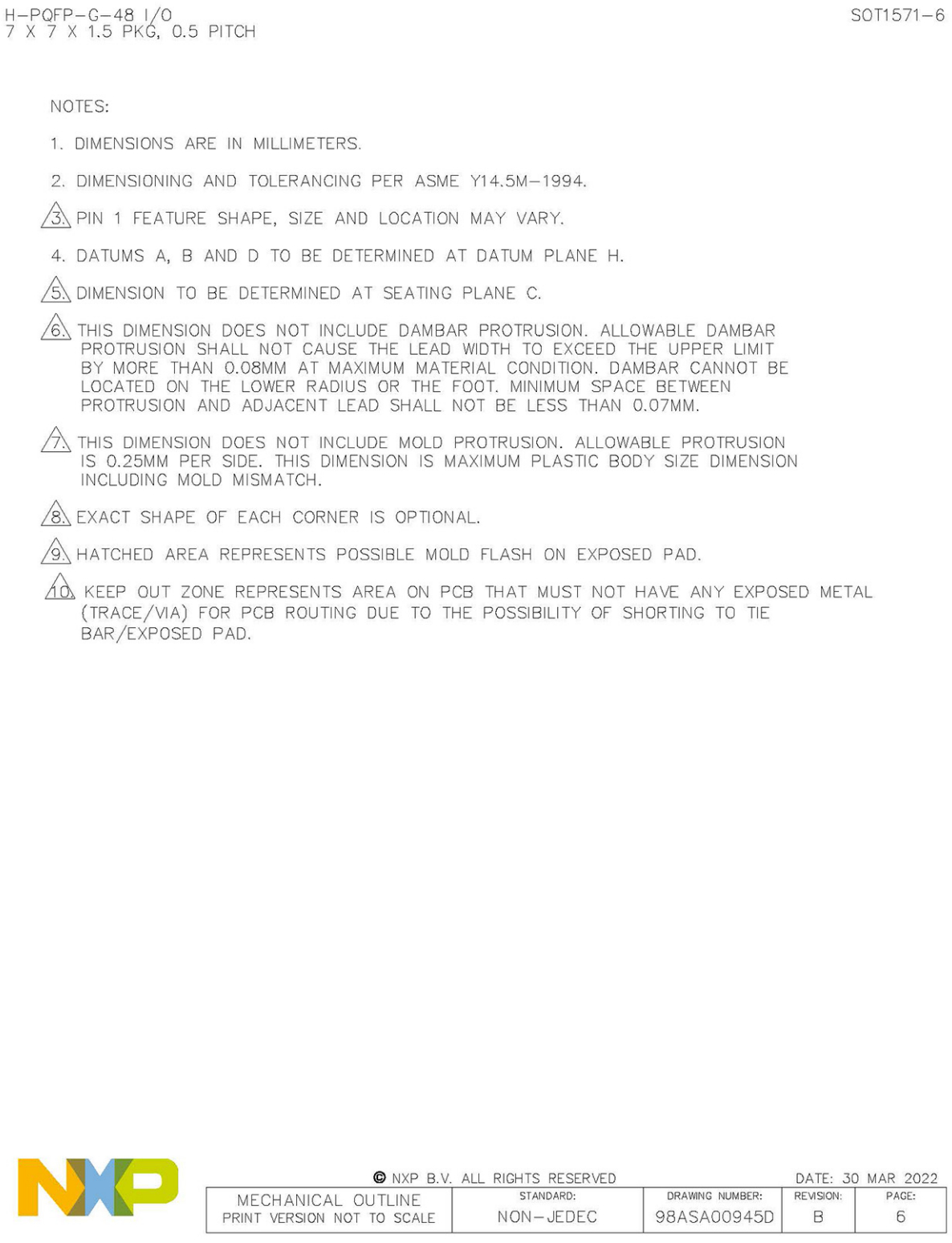

Figure 56. Package outline notes (SOT1571-6)

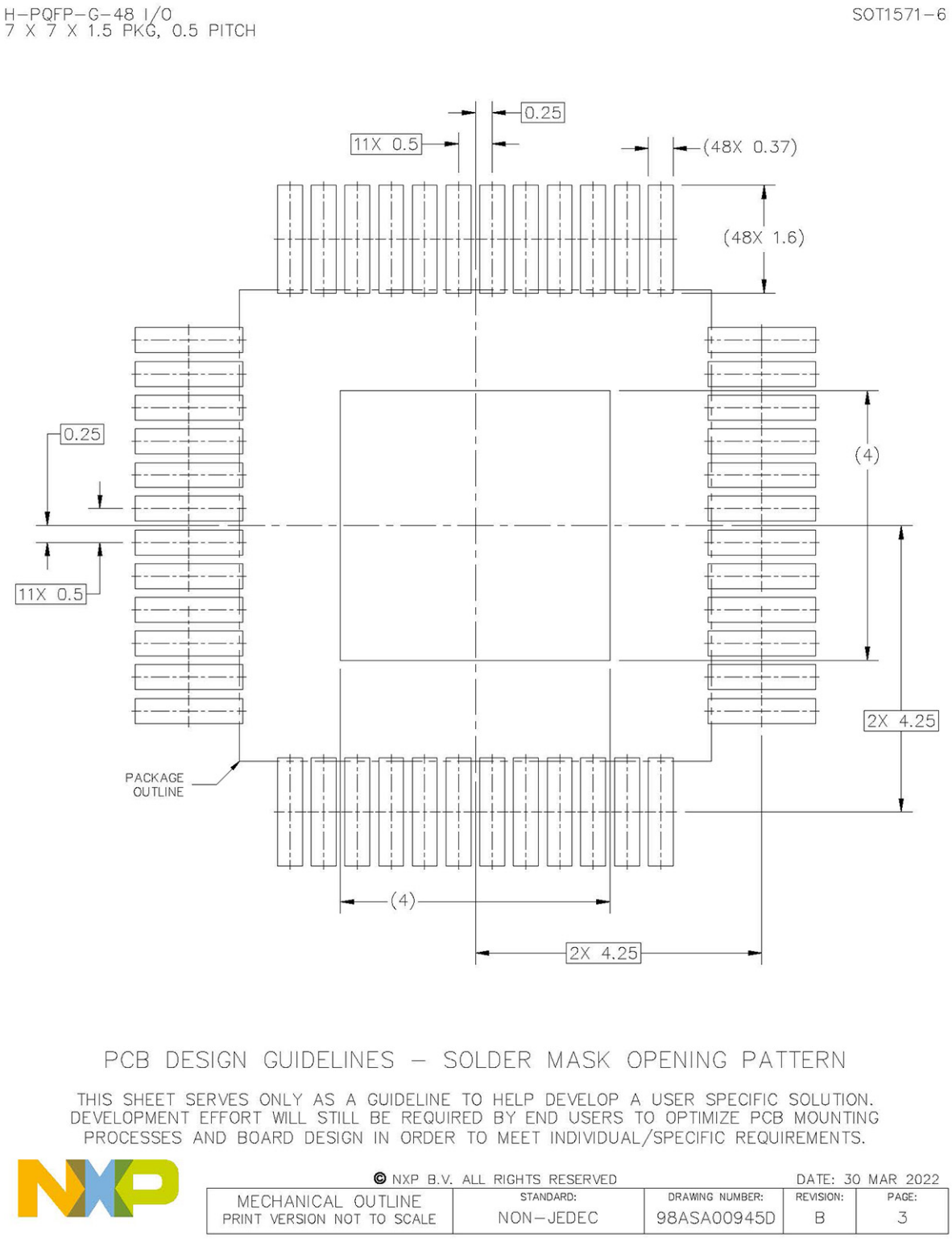

Figure 57. PCB design guidelines - solder mask opening pattern (SOT1571-6)

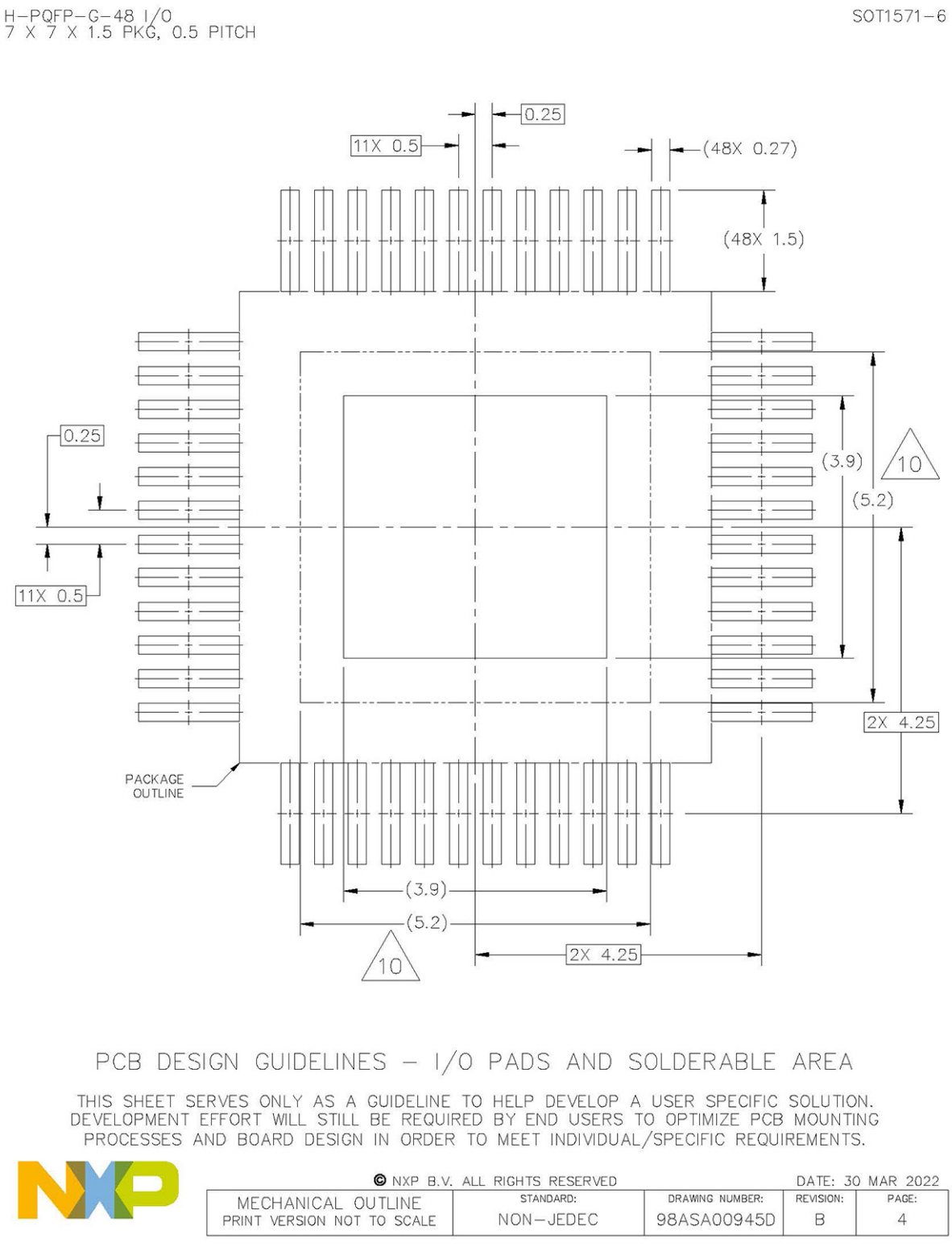

Figure 58. PCB design guidelines - I/O pads and solderable area (SOT1571-6)

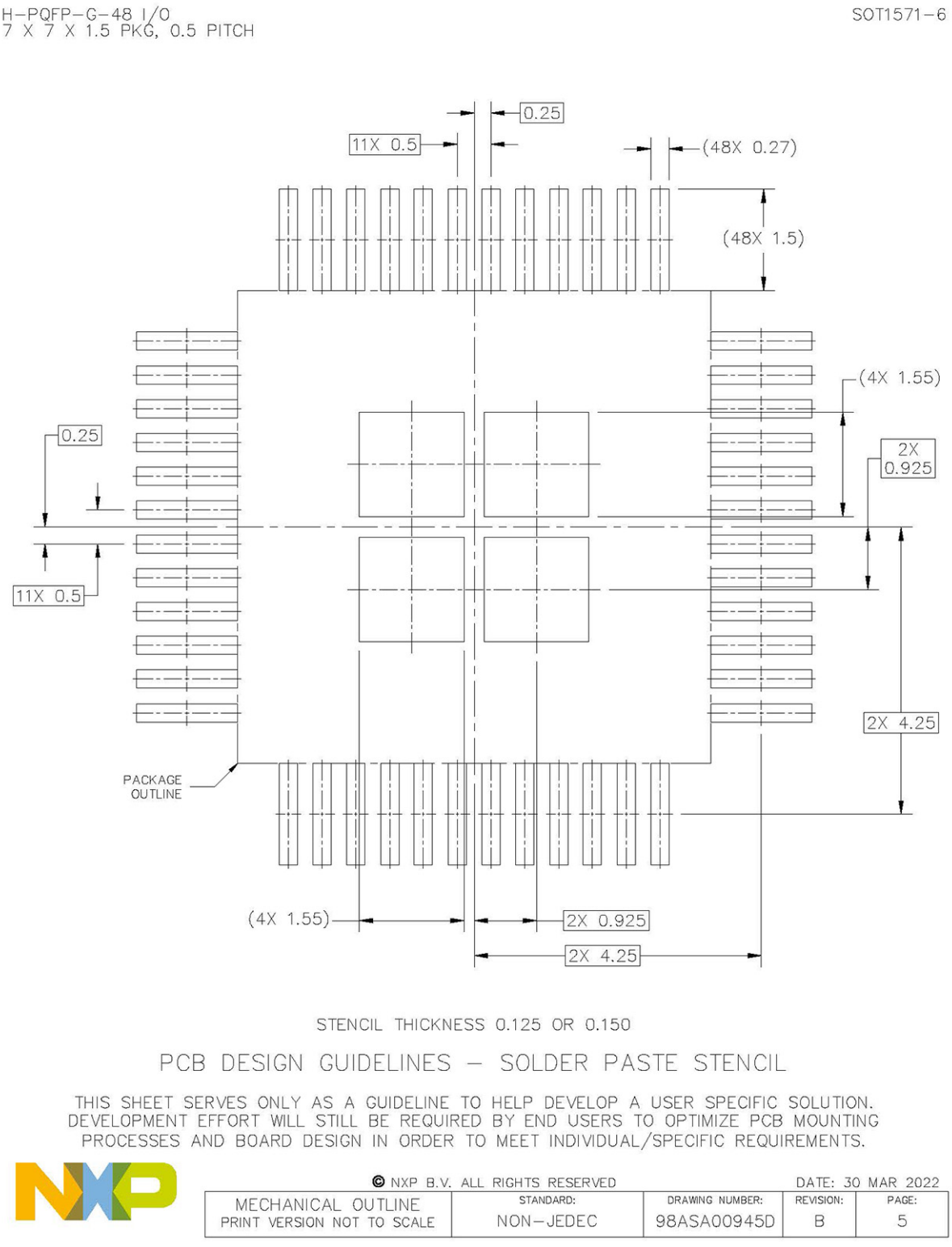

Figure 59. PCB design guidelines - solder paste stencil (SOT1571-6)

24 References

Table 129. References

Documents, Tools, Enablement	URL
FS26 Functional Safety Manual	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Dynamic FMEDA	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
AN12995 - FS26 Product Guidelines	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
AN13850 - FS26 implementation and behaviors	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26_SMPS_Calculator.xls	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 SMPS Simplis models	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Graphical User Interface • To create an OTP configuration • To interface an EVB KIT with a computer	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Power Dissipation Tool Calculator	https://www.nxp.com/products/power-management/pmics-andsbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-powerfit-for-asil-d:FS26
FS26 Product Overview	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
KITFS26AEEVM: FS26 Evaluation Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-evaluation-board:KITFS26AEEVM
KITFS26SKTEVM: FS26 Socket Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-programming-socket-board:KITFS26SKTEVM

25 Revision history

Table 130. Revision history

Document ID	Release date	Description
FS26_SDS v. 6.0	12 Dec. 2025	• Product data sheet • Changed document ID from FS26_PB to FS26_SDS • Global: transformed this document into a subset of the full data sheet that contains most of the data sheet information. • Revised Section 1 to mention that this is a subset of the full data sheet and access to the full data sheet requires an NDA

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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