BMA6402; BMI6402

Battery management communication gateway

Rev. 1.0 — 14 April 2025 Short data sheet

1 Product profile

1.1 General description

The BMx6402 is a general-purpose battery management wired communication gateway and transport protocol link (TPL) transceiver. The TPL is the proprietary bidirectional isolated daisy chain protocol of NXP via a single twisted-pair cable. The BMx6402 forwards requests from a standard microcontroller communication interface (MCU interface) to the TPL ports. Messages from the TPL ports are routed back to the MCU interface. Supported MCU communication types are serial peripheral interface (SPI) or controller area network flexible data rate (CAN FD).

The BMx6402S communicates directly to the MCU by using SPI. The BMx6402C powers an external CAN transceiver to be a part of a CAN bus. The standard communication protocols ensure compatibility with most microcontrollers available in the market.

The BMx6402 provides two TPL daisy chain ports to communicate with other BMS devices in the daisy chain. Each daisy chain port supports capacitive and inductive isolated communication.

The two daisy chain ports use the same protocol and ensure interoperability with NXP battery management devices like MC33774AT, BMA7118, and MC33775A or battery monitoring devices like MC33777.

The BMx6402 supports the ASIL D compliant communication protocol and is AEC-Q100 grade 1 qualified (only BMA6402).

1.2 Features and benefits

- MCU host interface supporting SPI or CAN (FD)
  - SPI (BMx6402S)
    - Single or dual SPI mode
    - Up to 10 Mbit/s data rate
  - CAN (FD) (BMx6402C)
    - CAN with up to 1 Mbit/s data rate
    - CAN FD with up to 1 Mbit/s arbitration and up to 5 Mbit/s data rate
  - Selectable I/O voltage of 5 V or 3.3 V
- Serial interfaces to control external devices, for example, EEPROMs and security ICs
  - SPI controller interface with up to 4 or 6 configurable chip select outputs
  - I^2C-bus controller interface
- Message buffering
  - Configurable response and request buffers
  - Status/handshake signals for data flow control
- Communication management unit
  - Error detection and reporting
- Multiport TPL interface
  - Two independent TPL daisy chain ports with integrated transceiver
  - Automatic message routing based on address of TPL message

  - Protocol supporting up to six TPL daisy chains and 62 nodes per chain
  - Each daisy chain features
    - 2 Mbit/s data rate (typ.)
    - Two-wire daisy chain supporting capacitive or inductive isolation
    - Loopback support
    - Support for broadcast messages toward multiple chains
  - Compatible with TPL3 based products (for example MC33774A, MC33777, BMA7118, or MC33775A)
- Power supply
  - Supply via external 5 V regulator or integrated 5 V regulator
  - Integrated 5 V regulator with operating range 5.5 V to 18 V
  - Power mode management of the external CAN (FD) transceiver
- Operation modes
  - Active mode
  - Sleep mode (25 µA typ.)
- Wake-up of the device by
  - TPL daisy chain (reverse wake-up)
  - MCU communication
  - Wake-up input (for example, external sensor information)
- Internal oscillator and external clock reference (external crystal or external clock signal) supported
- General-purpose inputs/outputs (GPIOs) with assignable status and events
- Unique device ID
- AEC-Q100 grade 1 qualified: −40 °C to +125 °C ambient temperature range (only BMA6402)
- Supports ASIL D compliant protocol of NXP due to end-to-end communication protection

2 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BMA6402S	LQFP48	plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body	SOT1571-1
BMI6402S	LQFP48	plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body	SOT1571-1
BMA6402C	LQFP48	plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body	SOT1571-1
BMI6402C	LQFP48	plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body	SOT1571-1

3 Block diagram

Figure 1 and Figure 2 show the general architecture of the BMx6402 versions.

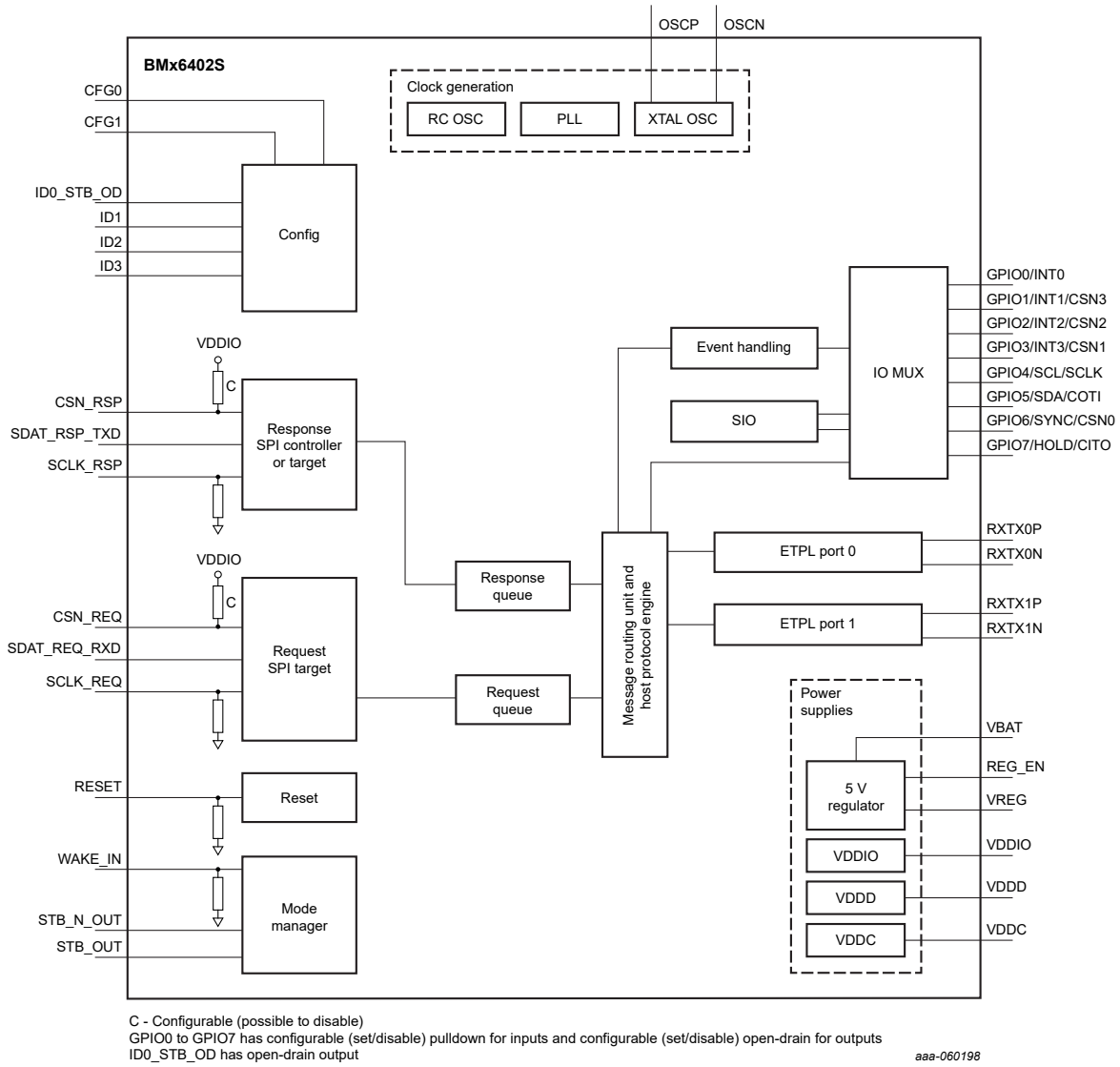

Figure 1. Block diagram of BMx6402S

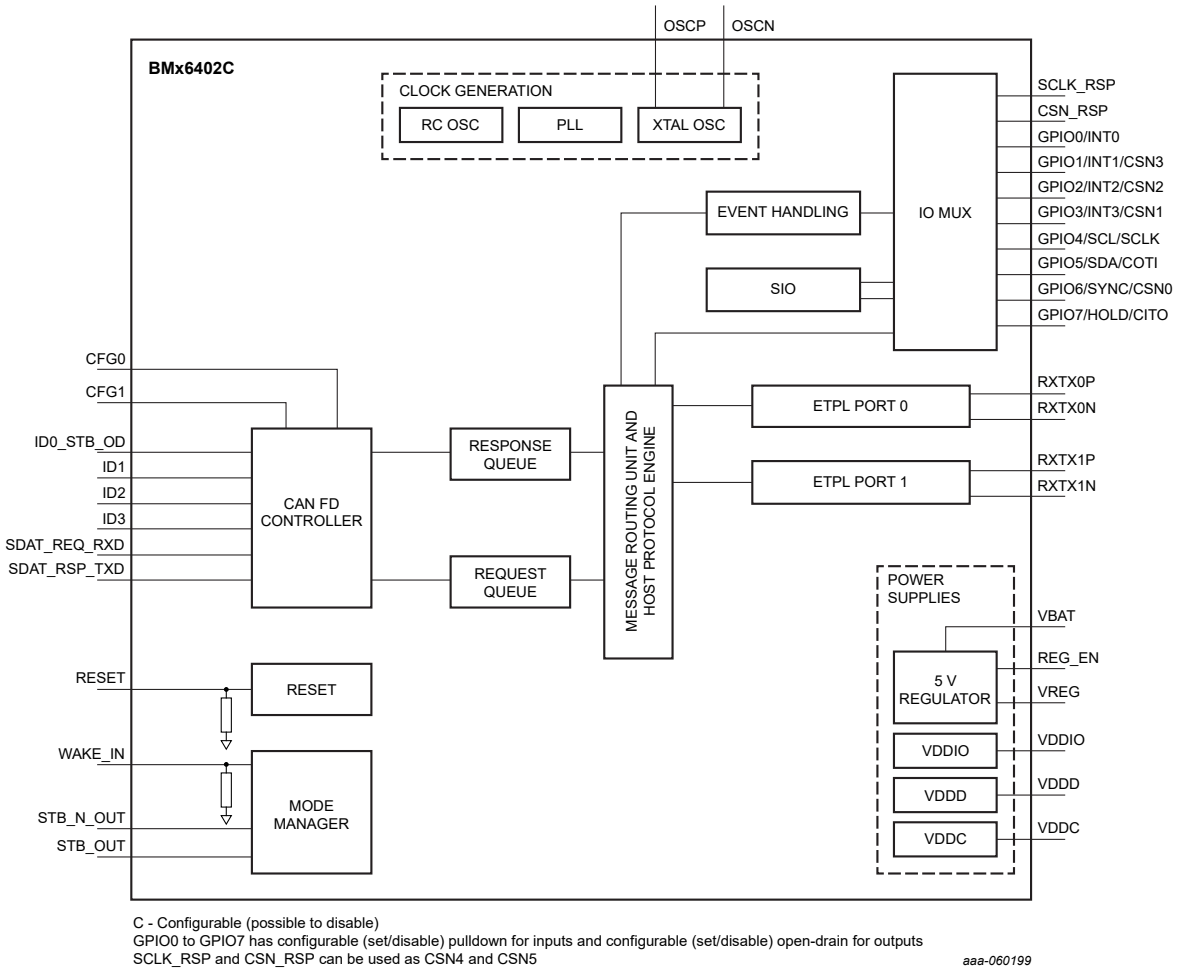

Figure 2. Block diagram of BMx6402C

4 Limiting values

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(VBAT)}$	input voltage on pin VBAT		−0.3	-	+40	V
V_{REG_EN}	voltage on pin REG_EN		−0.3	-	min ($V_{i(VBAT)}$ + 0.5, +40)	V
$V_{O(VREG)}$	output voltage on pin VREG		−0.3	-	+5.8	V
$V_{I(VDDD)}$	input voltage on pin VDDD		−0.3	-	+5.8	V
$V_{I(VDDC)}$	input voltage on pin VDDC		−0.3	-	+5.8	V
$V_{I(VDDIO)}$	input voltage on pin VDDIO		−0.3	-	+5.8	V

Table 2. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{I(dig)}$	digital input voltage	GPIO0 to GPIO7, ID1 to ID3, CFG0, CFG1, SDAT_REQ_RXD, SDAT_RSP_TXD, CSN_RSP, CSN_REQ, SCLK_REQ, SCLK_RSP, STB_N_OUT, STB_OUT	−0.3	-	min (V_{VDDIO} + 0.5, 5.8)	V
$V_{I(dig)}$	digital input voltage	ID0_STB_OD for CAN FD	−0.3	-	min (V_{VDDIO} + 0.5, 5.8)	V
$V_{I(dig)}$	digital input voltage	ID0_STB_OD for SPI or UART	−0.3	-	+5.8	V
$V_{I(WAKE\_IN)}$	input voltage on pin WAKE_IN		−0.3	-	min ($V_{i(VBAT)}$ + 0.5, +40)	V
$V_{i(OSCP)}$	input voltage on pin OSCP		−0.3	-	+5.8	V
$V_{i(OSCN)}$	input voltage on pin OSCN		−0.3	-	+2.75	V
$V_{bus(TPL)}$	voltage on TPL communication bus pins	RXTX0N, RXTX0P, RXTX1N, RXTX1P; relative to pin VSSC	−10	-	+10	V
$V_{I(RESET)}$	input voltage on pin RESET	maximum limits	−0.3	-	+5.8	V
ESD maximum ratings						
V_{ESD1}	electrostatic discharge voltage 1	at any pin; human body model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)	−2	-	+2	kV
V_{ESD2}	electrostatic discharge voltage 2	at VSSIO, ID0_STB_OD, ID1, ID2, ID3, VSSC, RXTX1P, RXTX1N, GNDSUB, RXTX0P, RXTX0N, WAKE_IN, REG_EN, VBAT, VSSD, CFG1, CFG0; HBM: according to AEC-Q100-002 (100 pF, 1.5 kΩ)	−4	-	+4	kV
V_{ESD3}	electrostatic discharge voltage 3	at all pins; charged device model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF)	−500	-	+500	V
V_{ESD4}	electrostatic discharge voltage 4	at corner pins; CDM: according to AEC-Q100-011 (field induced charge; 4 pF)	−750	-	+750	V
Thermal maximum ratings						
T_j	junction temperature		−40	-	+165	°C
T_{stg}	storage temperature		−55	-	+150	°C

Table 2. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature	[1]	-	-	260	°C

[1] Pin soldering temperature limit is maximum 10 s duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

5 Revision history

Table 3. Revision history

Document ID	Release date	Description
BMA6402_BMI6402_SDS v.1.0	14 April 2025	initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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