A6G25H112WN

Airfast RF Power GaN Amplifier

Rev. 1 — 22 August 2025 Product data sheet

1 General description

This 16 W asymmetrical Doherty RF power GaN amplifier is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2300 MHz to 2690 MHz.

This part is characterized and performance is guaranteed for applications operating in the 2300 MHz to 2690 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2 Features and benefits

- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

3 Typical performance

Table 1. 2600 MHz — Typical Doherty single-carrier W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQA} = 70 mA, V_{GSB} = -4.6 Vdc, P_{out} = 16 W Avg., input signal PAR = 9.9 dB @ 0.01 % probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	16.8	62.2	8.1	-30.9
2593 MHz	16.7	61.0	8.1	-32.9
2690 MHz	16.5	60.0	7.9	-34.4

[1] All data measured with device soldered to NXP reference circuit.

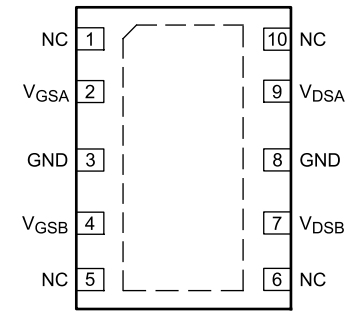
Table 2. 2400 MHz — Typical Doherty single-carrier W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQA} = 70 mA, V_{GSB} = -5.5 Vdc, P_{out} = 16 W Avg., input signal PAR = 9.9 dB @ 0.01 % probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	16.1	59.5	8.6	-32.9
2350 MHz	16.3	59.8	8.4	-34.1
2400 MHz	16.2	60.1	8.2	-33.9

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information



(Top view)

Note: Exposed backside of the package is the source terminal for the device.

Figure 1. Pin configuration

5 Ordering information

Table 3. Ordering information

Device	Tape and reel information	Package
A6G25H112WNT2	T2 suffix = 2,000 units, 24 mm tape width, 13-inch reel	DFN 7 × 10

6 Product marking

Figure 2. Product marking

Table 4. Product marking trace code

Identifier	Description
AA	Assembly location
WL	Wafer lot indicator
YYWW	Date code
ZZ	Assembly lot

7 Limiting values

Table 5. Limiting values

Symbol	Parameter	Conditions	Value	Unit
V_{DSS}	Drain-source voltage		125	Vdc
V_{GS}	Gate-source voltage		-8, 0	Vdc
V_{DD}	Operating voltage		55	Vdc
I_{GMAX}	Maximum forward gate current	$I_{G\ (A+B)}$, @ T_C = 25 °C	13	mA
T_{stg}	Storage temperature range		-65 to +150	°C
T_{CH}	Maximum channel temperature		225	°C

8 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Operating voltage		48	Vdc

9 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta SC}$ (IR)	Thermal resistance by infrared measurement, active die surface-to-case	Case temperature 107 °C, $P_{D\text{-}Global}$ = 13.6 W	2.4[1]	°C/W
$R_{\theta CHC}$ (FEA)	Thermal resistance by finite element analysis, channel-to-case	Carrier (case temperature 107 °C, P_D = 7.6 W)	7.5[1][2]	°C/W
		Peaking (case temperature 103 °C, P_D = 4.8 W)	5.4[1][2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to https://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A+B/(T+273)]}$, where T is the channel temperature in degrees Celsius, A = -12.47 and B = 9729.

10 ESD protection characteristics

Table 8. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	1A
Charge Device Model (per JS-002-2022)	C3

11 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

12 Electrical characteristics

12.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off characteristics[1]						
$I_{D(BR)}$	Off-state drain leakage	Carrier (V_{DS} = 150 Vdc, V_{GS} = -8 Vdc)	-	-	0.7	mAdc
		Peaking (V_{DS} = 150 Vdc, V_{GS} = -8 Vdc)	-	-	1.61	mAdc
I_{GLK}	Off-state gate leakage	Carrier (V_{DS} = 48 Vdc, V_{GS} = -8 Vdc)	-0.36	-	-	mAdc
		Peaking (V_{DS} = 48 Vdc, V_{GS} = -8 Vdc)	-0.84	-	-	mAdc

[1] Each side of device measured separately.

12.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On characteristics — Side A, Carrier						
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 10 Vdc, I_D = 4.1 mAdc	-4.6	-2.3	-1.85	Vdc
$V_{GSA(Q)}$	Gate quiescent voltage	V_{DD} = 48 Vdc, I_{DA} = 70 mAdc[1]	-3.3	-2.7	-2.1	Vdc
I_{GSS}	Gate-source leakage current	V_{DS} = 150 Vdc, V_{GS} = -8 Vdc	-0.7	-	-	mAdc
On characteristics — Side B, Peaking						
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 10 Vdc, I_D = 9.36 mAdc	-4.6	-2.4	-1.9	Vdc
I_{GSS}	Gate-source leakage current	V_{DS} = 150 Vdc, V_{GS} = -8 Vdc	-1.61	-	-	mAdc

[1] Measured in functional test.

12.3 Functional tests

Table 12. Functional tests

(In NXP Doherty production ATE[1] test fixture, T_A = 25 °C unless otherwise noted, 50 ohm system)[2] V_{DD} = 48 Vdc, I_{DQA} = 70 mA, V_{GSB} = (V_t - 1.4) Vdc, P_{out} = 16 W Avg., f = 2690 MHz, LTE-FDD 20 MHz, 7.5 dB PAR.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_{ps}	Power gain		13.3	14.8	18.0	dB
η_D	Drain efficiency		49.0	54.7	-	%
P_{sat}	Saturated power	Pulsed CW, 5 % duty cycle	48.9	53.0	-	dBm
ACPR	Adjacent channel power ratio		-	-29.5	-25.0	dBc

[1] ATE is a socketed test environment.
[2] Internally matched part.

12.4 Wideband ruggedness

Table 13. Wideband ruggedness

(In NXP Doherty reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1] I_{DQA} = 70 mA, V_{GSB} = -4.6 Vdc, f = 2500 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 46.9 W Avg. modulated output power (3 dB input overdrive from 16 W Avg. modulated output power)	No device degradation

[1] All data measured with device soldered to NXP reference circuit.

12.5 Typical performance

Table 14. Typical performance

(In NXP Doherty reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1] V_{DD} = 48 Vdc, I_{DQA} = 70 mA, V_{GSB} = -4.6 Vdc, 2496–2690 MHz bandwidth.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulsed CW, 10 % duty cycle						
P_{sat}	Saturated power		-	108	-	W
Φ	AM/PM (Phase deviation from rated power to saturated power. Maximum value measured across the 2496–2690 MHz bandwidth.)		-	-8	-	°
ΔG	Gain variation @ Avg. power over temperature	-40 °C to +85 °C	-	0.008	-	dB/°C
ΔP_{sat}	Output power variation @ saturated power over temperature	-40 °C to +85 °C	-	0.003	-	dB/°C
Single-carrier W-CDMA, unclipped						
G_F	Gain flatness	194 MHz bandwidth @ P_{out} = 16 W Avg.	-	0.2	-	dB
2-tone CW						
VBW_{res}	VBW resonance[2]		-	220	-	MHz

[1] All data measured with device soldered to NXP reference circuit.
[2] IMD third order inflection point.

Correct biasing sequence for GaN depletion mode amplifiers in a Doherty configuration

Bias ON the device

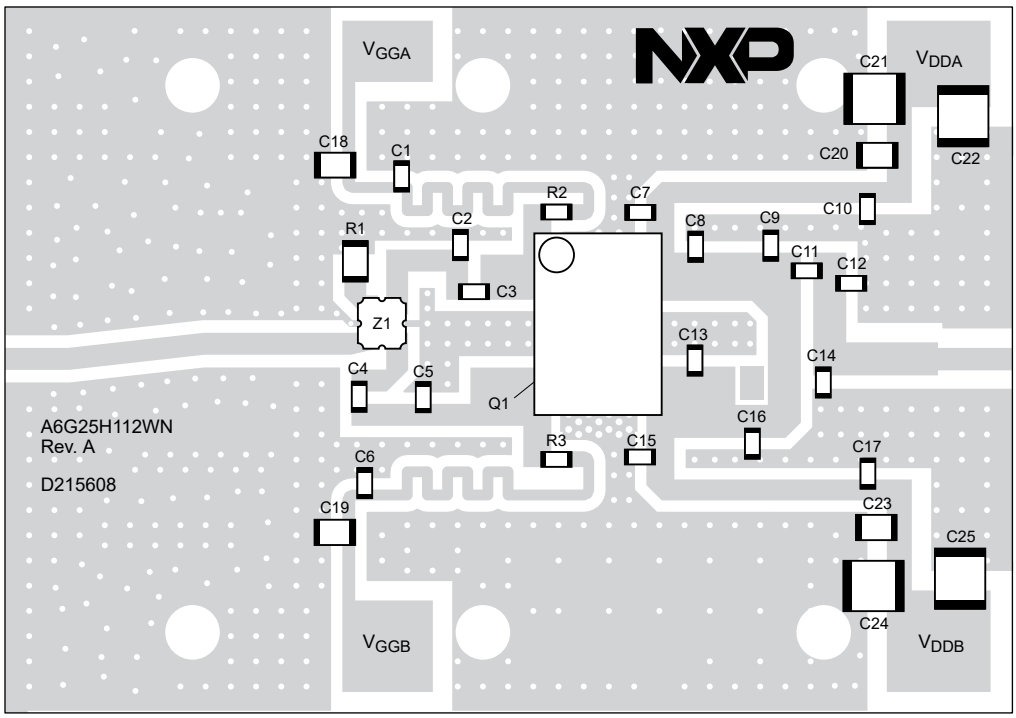
1. Set gate voltage V_{GSA} and V_{GSB} to -5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to -5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.

13 Component layout and parts list

13.1 Component layout



Note: All data measured in reference circuit with device soldered to heatsink. *aaa-062403*

Figure 3. A6G25H112WN reference circuit component layout

13.2 Component designations and values

Table 15. A6G25H112WN reference circuit component designations and values

Part	Description	Part Number	Manufacturer
C1, C6, C10, C11, C17	12 pF chip capacitor	600S12R0AW250XT	Kyocera AVX/ATC
C2	0.7 pF chip capacitor	600S0R7AW250XT	Kyocera AVX/ATC
C3	15 pF chip capacitor	600S15R0AW250XT	Kyocera AVX/ATC
C4	8.2 pF chip capacitor	600S8R2AW250XT	Kyocera AVX/ATC
C5	0.6 pF chip capacitor	600S0R6AW250XT	Kyocera AVX/ATC
C7	0.8 pF chip capacitor	600S0R8AW250XT	Kyocera AVX/ATC
C8, C9, C12, C16	0.3 pF chip capacitor	600S0R3AW250XT	Kyocera AVX/ATC
C13	1.3 pF chip capacitor	600S1R3AW250XT	Kyocera AVX/ATC
C14	0.5 pF chip capacitor	600S0R5AW250XT	Kyocera AVX/ATC
C15	1 pF chip capacitor	600S1R0AW250XT	Kyocera AVX/ATC
C18, C19, C20, C23	1 µF chip capacitor	C3216X7R2A105K160AA	TDK
C21, C22, C24, C25	10 µF chip capacitor	GRM32EC72A106KE05L	Murata
Q1	RF power GAN amplifier	A6G25H112WN	NXP
R1	50 Ω, 8 W termination chip resistor	C8A50Z4B	TTM/Anaren
R2, R3	10 Ω, 1/10 W chip resistor	RC0603FR-0710RL	Yageo
Z1	2200–2800 MHz, 90°, 3 dB hybrid coupler	X4C25J1-03G	TTM/Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D215608	MTL

14 Package information

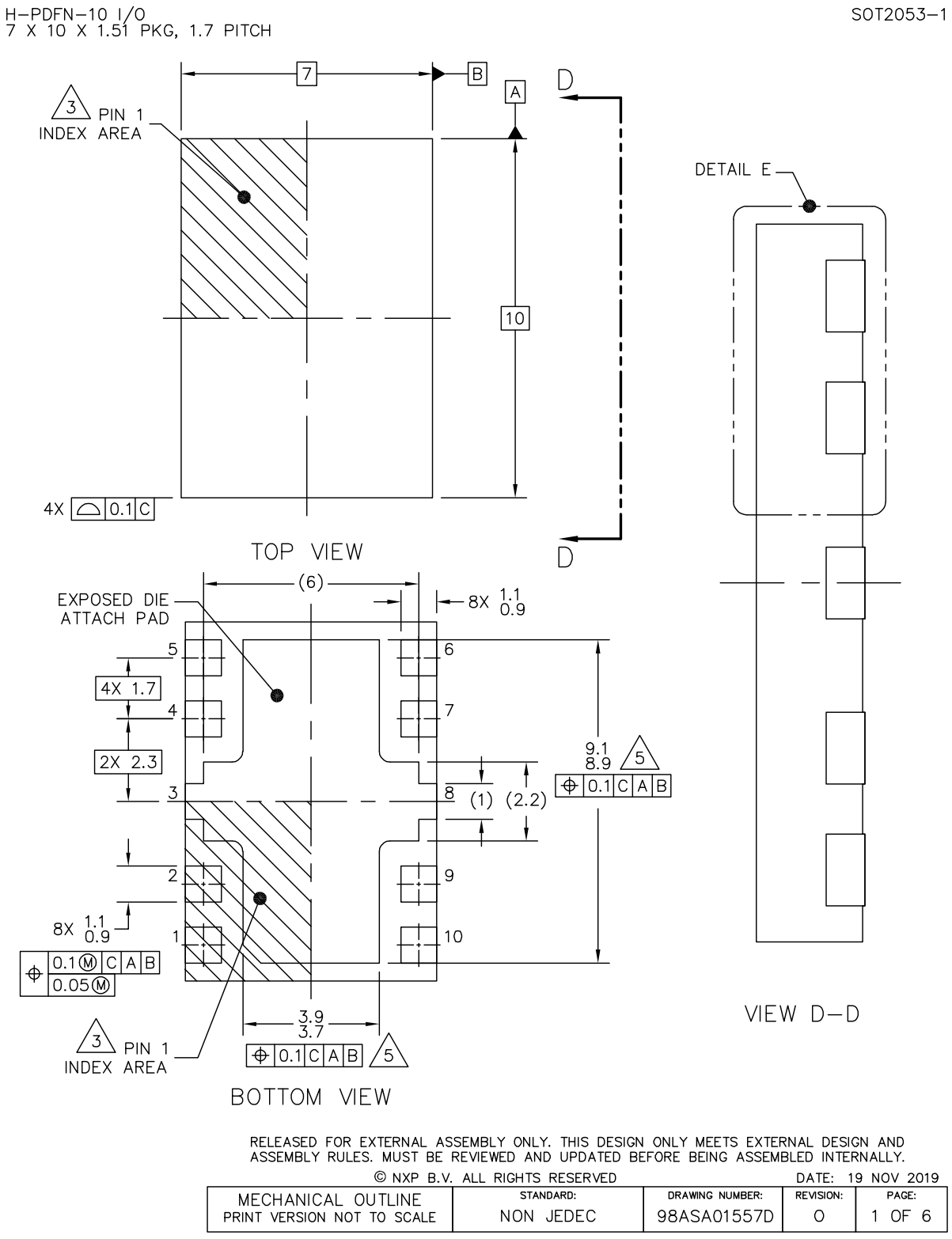


Figure 4. Package outline (DFN 7 mm × 10 mm) — top view, bottom view, detail E

H–PDFN–10 I/O
7 X 10 X 1.51 PKG, 1.7 PITCH

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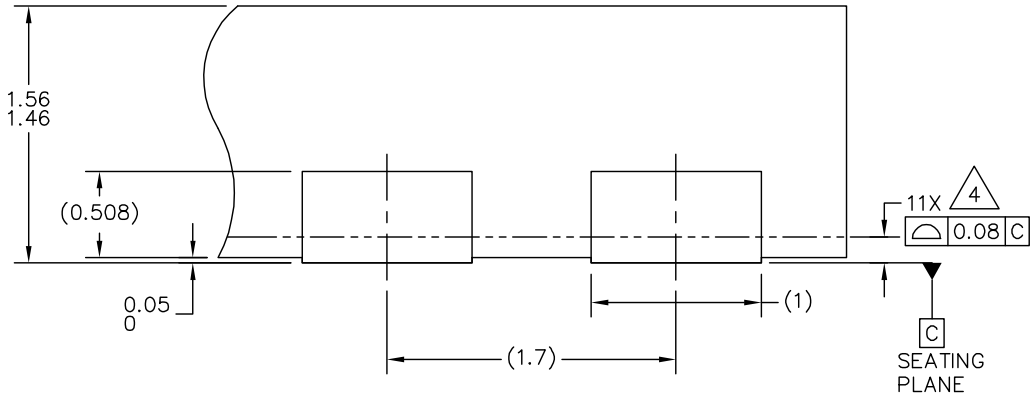

DETAIL E
VIEW ROTATED 90°CW

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

DATE: 19 NOV 2019

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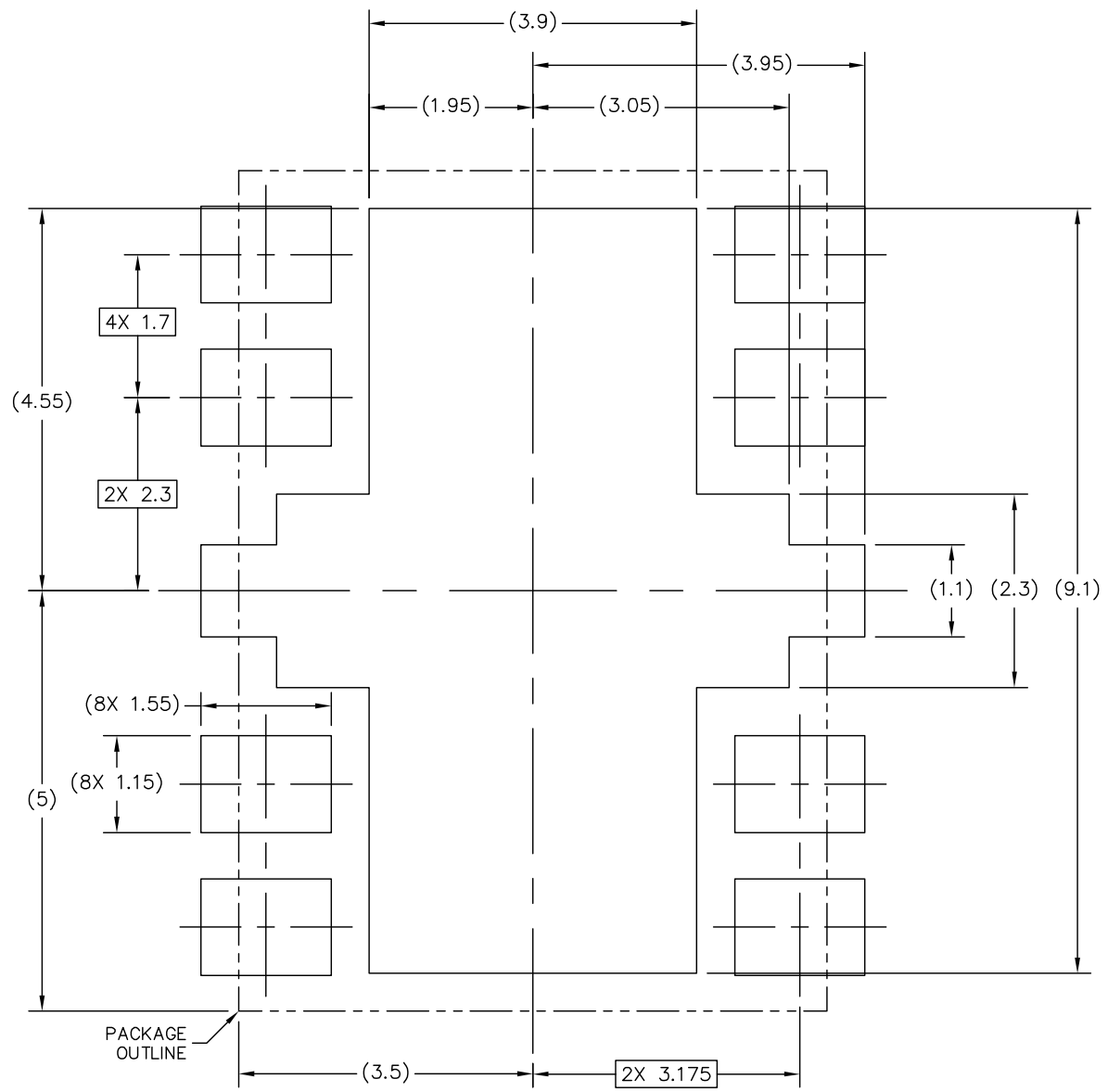
Figure 5. Package outline (DFN 7 mm × 10 mm) — detail E, rotated



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 19 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01557D	REVISION: O	PAGE: 3

Figure 6. Package outline (DFN 7 mm × 10 mm) — PCB design guidelines: solder mask opening pattern

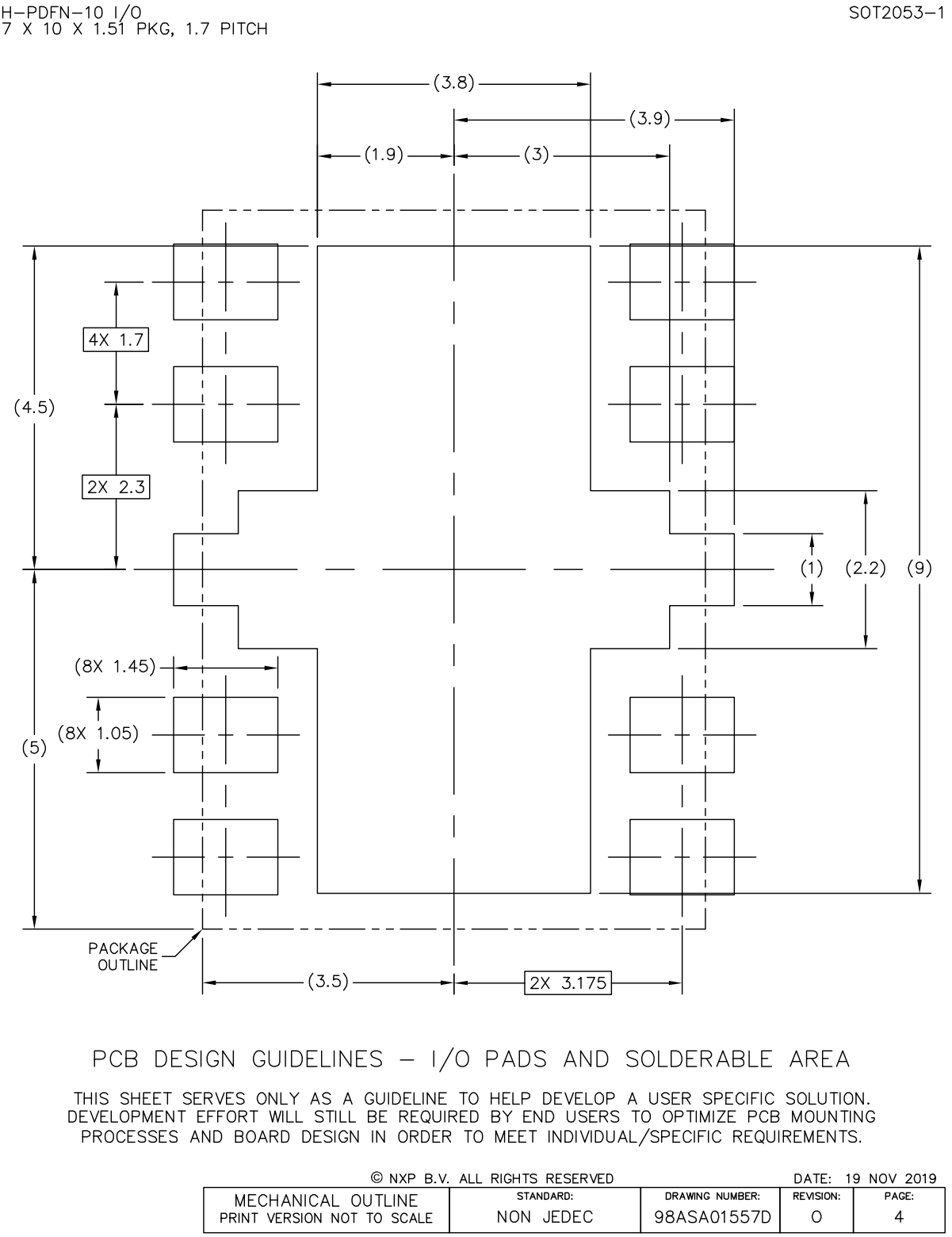


Figure 7. Package outline (DFN 7 mm × 10 mm) — PCB design guidelines: I/O pads and solderable area

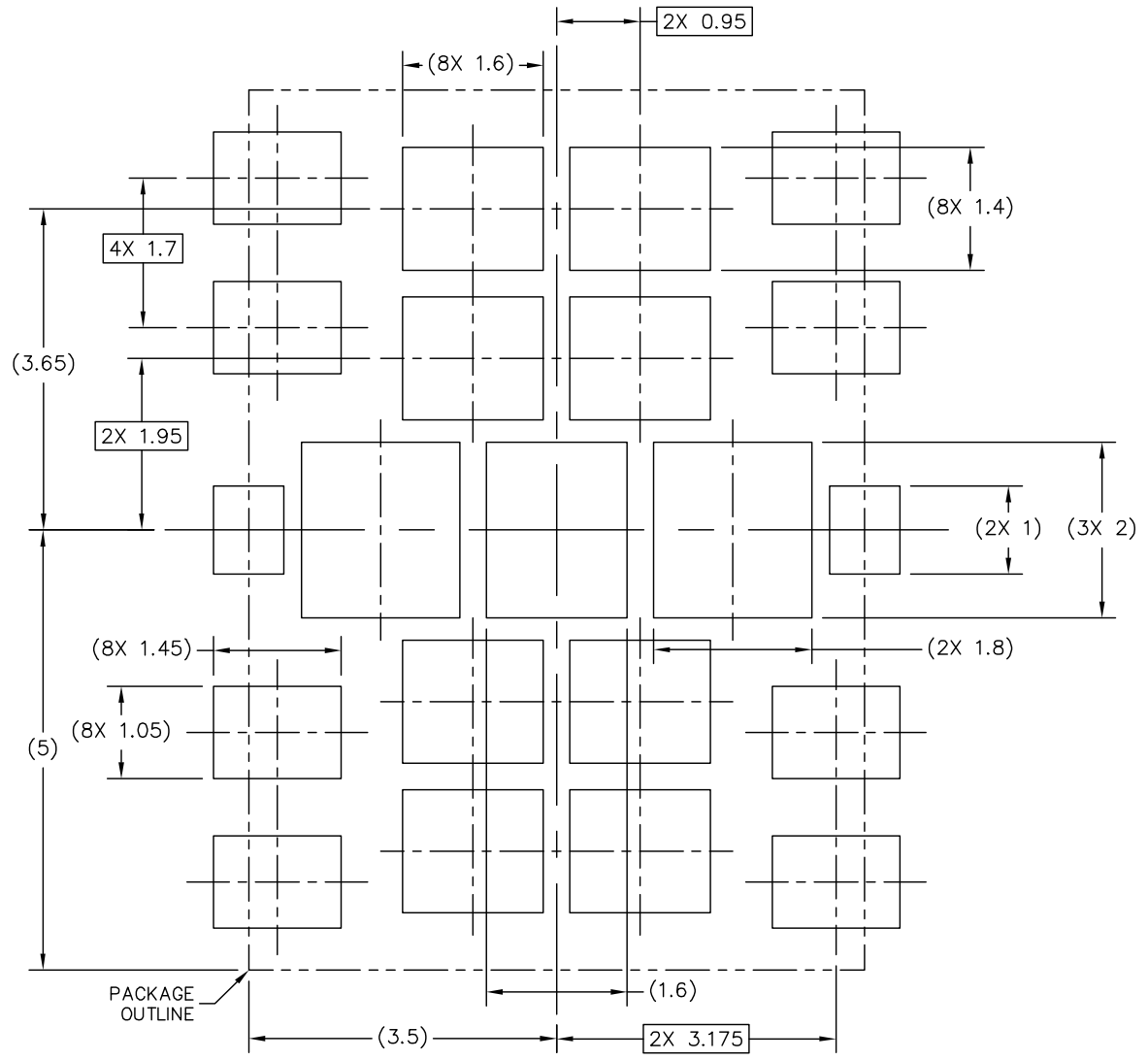


Figure 8. Package outline (DFN 7 mm × 10 mm) — PCB design guidelines: solder paste stencil

H–PDFN–10 I/O
7 X 10 X 1.51 PKG, 1.7 PITCH

SOT2053–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. RADIUS ON DIE ATTACH FLAG IS OPTIONAL.

DATE: 19 NOV 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01557D	REVISION: O	PAGE: 6

Figure 9. Package outline (DFN 7 mm × 10 mm) — notes

15 Product documentation, software and tools

Refer to the following resources to aid your design process.

Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p file

Development tools

- Printed circuit boards

16 Revision history

The following table summarizes revisions to this document.

Table 16. Revision history

Document ID	Release date	Description
A6G25H112WN v.1	22 August 2025	• Initial release of product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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